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HSPICE simulation and analysis of current reused operational transconductance amplifiers for biomedical applications

Udari Gnaneshwara Chary[1,2], Kakarla Hari Kishore[1]
[1]Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation, Guntur, India
[2]Department of Electronics and Communication Engineering, B V Raju Institute of Technology, Narsapur, India

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ABSTRACT

The proposed work focuses on the design of a current-reused biomedical amplifier; it is a microwatt-level electrocardiogram (ECG) analog circuit design that addresses low power consumption and noise efficiency. As implantable devices require unobtrusiveness and longevity, the current reuse technique in this circuit effectively enhances power and noise efficiencies. Using 90 nm technology enables efficient circuit implementation, yielding promising simulation results. At 100 Hz, the noise performance reaches 62.095 nV/√Hz, while the power consumption is only 8.3797 µW. These advancements are pivotal for next-generation implantable devices, ensuring reliable operation and reducing frequent battery replacements, improving patient convenience. Moreover, the high noise efficiency ensures that ECG signals are captured with high fidelity, crucial for accurate monitoring and diagnosis. This research addresses the challenges in implantable ECG analog circuit design and sets a benchmark for future developments. The techniques employed can be adapted for other bio signal monitoring devices, broadening the impact on healthcare technology. Ultimately, this advancement contributes to more efficient, reliable, and long-lasting medical devices, enhancing patient monitoring and healthcare on a broader scale.

Corresponding Author:

Kakarla Hari Kishore
Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation
Vaddeswaram, Guntur, Andhra Pradesh, India
Email: kakarla.harikishore@kluniversity.in

1. INTRODUCTION

The design and development of the current reused biomedical amplifiers pose significant engineering challenges, particularly in terms of achieving low power consumption and high noise efficiency. It must function consistently within the human body for extended periods of time in order to be used for continuous patient monitoring. Electrocardiogram (ECG) monitoring is a crucial application domain for these devices, as precise diagnosis and treatment depend on the high-fidelity acquisition and processing of cardiac signals.

Long operational lifetimes and minimal power consumption are requirements for implantable devices, which also call for superior signal integrity. However, creating such circuits requires balancing a difficult trade-off between noise reduction and power consumption. Effective noise reduction approaches can result in higher power consumption and circuit complexity, while traditional low-power strategies frequently sacrifice noise performance. The proposed work focuses on the operational transconductance amplifier (OTA), a three-input terminal device with high output resistance, in contrast to the op-amp, which has two input terminals and low output resistance. The OTA operates as a voltage-controlled current source, generating current as its output [1]–[3]. Compared to op-amps, OTAs exhibit superior high-frequency

capabilities. OTAs come in various types, including voltage-controlled OTA (VCO), current-controlled OTA (CCO), differential OTA, variable gain OTA, and switched-capacitor OTA [4]–[6]. In many applications, the OTA stands as the analog integrated circuit block with the highest power consumption. Designing low-power OTAs poses challenges, especially considering the increasing importance of low-power consumption in mobile devices. This is due to the trade-off between speed, power, and gain, as these parameters often conflict [7]–[10]. Various techniques are available to address power consumption concerns, and selecting the appropriate technology becomes crucial, especially for medical appliances. One such technique is the current reuse technique [11]–[13].

The current reuse technique in OTA designs enhances performance and reduces power consumption [14], [15]. It involves recycling the current that flows through the amplifier's load back to the input stage, accomplished through the introduction of a feedback loop [16]–[18]. By allowing the current to return to the input stage instead of dissipating heat, the OTA can achieve higher gain, improved linearity, and reduced power consumption [19], [20]. This technique is particularly beneficial in low-power applications where minimizing power consumption is critical [21]–[24]. Current reuse can be implemented in various ways, as explained below. The folded-cascode OTA is a widely used architecture that features two stages-a cascode stage and a common-source stage. It efficiently reuses the bias currents, thereby reducing power consumption. The cascode stage provides high gain, while the common-source stage serves as a current mirror, enabling current reuse [25], [26]. The folded-cascode OTA exhibits excellent linearity and high gain, making it suitable for a wide range of applications [27]. The bulk-driven OTA uses the bulk terminal of metal oxide semiconductor (MOS) transistors to generate bias currents, reducing the need for extra biasing circuitry. By doing so, it achieves power efficiency by reusing currents in the biasing network. This architecture is particularly advantageous for low-power applications, where minimizing power consumption is critical [28], [29]. The adaptive biasing OTA dynamically adjusts the bias currents based on the input signal amplitude. It employs a feedback mechanism to vary the bias currents, ensuring optimum power efficiency while maintaining linearity. This approach is particularly useful in applications with varying signal conditions, such as communication receivers, where power consumption can be reduced during low signal levels [30]–[32]. Operating in the subthreshold region allows the OTA to achieve ultra-low power consumption. By leveraging subthreshold operation, the OTA takes advantage of the exponential relationship between current and voltage in weak inversion, leading to reduced power dissipation [33]. Current reuse is crucial in subthreshold OTAs to maintain reasonable performance levels while minimizing power consumption [34]. The cascode OTA uses a cascode configuration to achieve high gain and reduce power dissipation. By reusing bias currents between the cascode stages, this architecture efficiently utilizes power resources [35], [36]. The cascode current-reused OTA is well-suited for high-gain applications, such as filters and instrumentation amplifiers [37].

The switched-current OTA employs charge transfer techniques to achieve current reuse. It utilizes clocked switches to transfer charges between different stages, enabling efficient current recycling. This architecture is commonly used in applications requiring high-speed analog signal processing, such as switched-capacitor filters and data converters [38]. This OTA combines the advantages of adaptive biasing and bulk-driven techniques. Using the bulk-driven approach for biasing and integrating an adaptive biasing mechanism achieves high power efficiency and adaptability to varying signal conditions [39]. This architecture finds applications in low-power sensor interfaces and battery-powered systems. The source-degenerated OTA introduces a resistor in the source branch of the transconductance stage, enhancing the linearity and power efficiency. It enables better control over the gain and facilitates current reuse, making it suitable for applications where high linearity and power efficiency are essential, such as wireless communication systems. As explained above, each method offers its own advantages and disadvantages, depending on the specific requirements of the OTA application [40]–[42]. As explained above, the previous research has explored several approaches to address these challenges. Low-power design techniques such as duty cycling, sub-threshold operation, and energy harvesting have been employed to extend battery life.

However, these methods often compromise noise performance or add complexity to the circuit design. Noise reduction techniques like chopper stabilization correlated double sampling, and filtering has also been utilized to enhance signal integrity. While effective in certain contexts, these approaches can increase power consumption or require more complex circuitry, making them less suitable for power-constrained implantable devices. In some cases, the concept of current reuse has been investigated in analog circuits to improve efficiency. Current reuse involves recycling the current within the circuit to reduce overall power consumption. Although promising, its application in the specific domain of ECG analogue circuits for implantable devices remains underexplored, presenting an opportunity for innovation. Current reused operational transconductance amplifiers (CR-OTAs) also play a significant role in the realm of quantum computing and quantum electronics due to their ability to efficiently manage power consumption while maintaining high performance [43]–[45]. These amplifiers are particularly valuable in quantum systems where the precision and stability of signal amplification are crucial. CR-OTAs operate by reusing the current

in multiple stages of the amplifier, reducing the overall power consumption and enhancing the linearity and bandwidth of the device. This efficiency is vital in quantum applications [46]–[51], where maintaining low temperatures is critical to minimize thermal noise and decoherence. The improved performance of CR-OTAs ensures that quantum signals can be amplified with minimal distortion, preserving the integrity of quantum information. Furthermore, their compact design and reduced power requirements make them suitable for integration into the highly sensitive and space-constrained environments typical of quantum computing hardware [52]–[55]. As a result, CR-OTAs are essential components in advancing the development of scalable and efficient quantum systems.

The organization of the remaining paper is as follows: section 2 delves into the proposed current reuse technique, explaining its principles and variations. Section 3 presents the results obtained through simulations, validating the effectiveness of the proposed technique. Section 4 provides an in-depth analysis and interpretation of the results with a detailed discussion. Finally, the paper is concluded in section 5. Through the exploration of current reuse in OTAs, this paper contributes to the advancement of low-power analog circuit designs, particularly in the context of medical appliances.

2. PROPOSED CURRENT REUSE ARCHITECTURE

Current reuse is a beneficial technique employed in operational transconductance amplifiers (OTAs) to enhance efficiency and reduce power consumption. OTAs typically consume a significant amount of power, especially in the transconductance stage. By implementing current reuse, the OTA can recycle a portion of the current flowing through this stage instead of dissipating it as heat [29]–[32]. However, one drawback of OTA design is the increase in current consumption. To address this, current reuse architecture has been introduced to optimize power utilization. By employing shared bias devices to preserve headroom, orthogonal current reuse enhances the trade-off between noise and power. In a two-channel design, orthogonal current reuse requires splitting the input of the second channel into two identical, half-sized differential pairs that utilize the drain currents from the first channel as tail currents [33]. This design can accommodate multiple signal channels, each with the same amplifier transconductance, by stacking additional differential pairs, further improving the amplifier's efficiency. Moreover, it allows for ultra-low power operation under very low voltage supplies without compromising noise performance.

The proposed OTA design shown in Figure 1 incorporates a current mirror to facilitate efficient current reuse. The use of current reuse techniques is widespread in analog circuit design as it minimizes power consumption and reduces chip area. This technique involves reusing an already generated current in one part of the circuit rather than generating a new current from scratch in another part. The complementary metal oxide semiconductor (CMOS) current mirror, a vital component in current reuse techniques, is employed to achieve this goal. In a current reuse circuit, the output current from one stage is fed back to serve as the input current for another stage. This enables subsequent stages to utilize the same current source as the previous stages, effectively reducing the overall power consumption of the circuit. The core principle of the current reuse technique with CMOS current mirrors is to generate a reference current by biasing a reference transistor in the saturation region and then reusing this current in multiple circuit blocks. This reference current can be replicated by employing a series of mirror transistors connected in parallel, with each supplying the required current to the load transistors in each block. In the CMOS current mirror concept, two matched transistors, typically a p-channel and an n-channel metal–oxide–semiconductor field-effect transistor (MOSFET), are utilized to create a "mirror" current that is proportional to the reference current. The reference current flows through the source of the reference transistor and is mirrored through the drain of the mirror transistor.

The CMOS current mirror circuit consists of two transistors connected in a common source configuration, with their gates and drains connected in series. The reference transistor is typically biased in the saturation region, while the mirror transistor operates in the triode region. By carefully selecting the aspect ratio of the transistors, the mirrored current can closely approximate the reference current. One of the primary advantages of CMOS current mirrors is their low power consumption, making them highly suitable for low-power applications. Additionally, using complementary MOSFETs in the circuit ensures minimal voltage drop across the mirror transistor, thereby minimizing power dissipation. The output current (I_{OUT}) of the differential pair can be expressed as:

$$I_{OUT} = I_{D1} - I_{D2} = g_m * ((V_{G1} - V_T) - (V_{G2} - V_T)) = g_m * (V_{G1} - V_{G2})$$

The output voltage (V_{OUT}) of the differential pair can be expressed as:

$$V_{OUT} = -g_{m3} * ((V_{DD} - I_{OUT} * R_D) - V_{SS})$$
$$= -g_{m3} * (V_{DD} - (g_m * (V_{G1} - V_{G2})) * R_D - V_{SS})$$

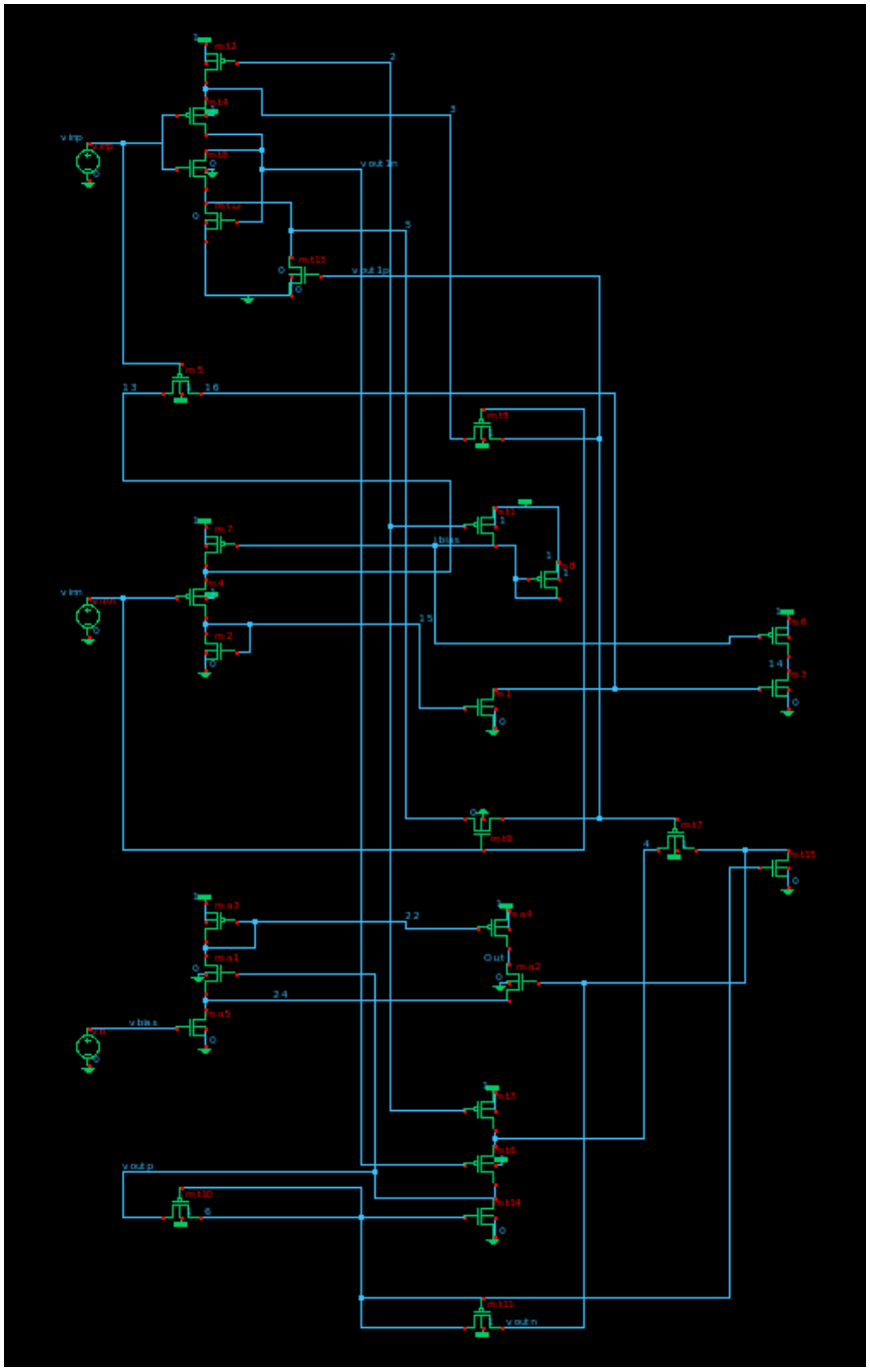

Figure 1. Current reuse amplifier circuit

3. SIMULATION RESULTS AND ANALYSIS

The proposed circuit was designed and simulated using the HSPICE simulator, a widely recognized and trusted tool in the industry for CMOS circuit design and analysis. HSPICE is renowned for its accuracy and reliability in modeling complex electronic circuits, making it an ideal choice for our work. The simulation process involved developing a detailed HSPICE code tailored specifically for our circuit, ensuring that all aspects of its performance were thoroughly examined. This included the implementation of our current reuse technique and the evaluation of critical parameters such as noise performance and power consumption. The

comprehensive HSPICE code provided a precise representation of the circuit's behavior, enabling us to verify and optimize its design effectively.

3.1. Input netlist file (HSPICE code)

HSPICE code is a powerful analog and mixed-signal circuit simulator used to design and verify integrated circuits (ICs) at various stages of the design process. It is widely used in the electronics industry to simulate complex circuits, including analog, digital, and mixed-signal systems. Developed by Synopsys, HSPICE offers precise, reliable simulation results, making it a standard tool for circuit designers. The developed HSPICE code for the proposed circuit is as detailed as follows.

```
.option post nomod
.op
.temp 30
.option Use_AGAUSS_Format=yes
.option PARHIER = LOCAL
.option MODMONTE = 0
.option MONTECON = 1
.option PORT_VOLTAGE_SCALE_TO_2X = 1
.variation
Option OUTPUT_SIGMA_VALUE=1
.end_variation vdd 1 0 dc 0.4
mt1 ibias 2 1 1 p12 l=0.56u w=0.5u
mt2 3 2 1 1 p12 l=0.56u w=0.5u
mt3 4 2 1 1 p12 l=0.56u w=0.5u
mt4 vout1n vinp 3 1 p12 l=0.56u w=0.5u
mt5 vout1p vinn 3 1 p12 l=0.56u w=0.5u
mt6 voutp vout1n 4 1 p12 l=0.56u w=0.5u
mt7 voutn vout1p 4 1 p12 l=0.56u w=0.5u
mt8 vout1n vinp 5 0 n12 l=0.56u w=0.5u
mt9 vout1p vinn 5 0 n12 l=0.56u w=0.5u
mt10 6 6 voutp 1 p12 l=0.56u w=0.5u
mt11 6 6 voutn 1 p12 l=0.56u w=0.5u
mt12 5 vout1n 0 0 n12 l=0.56u w=0.5u
mt13 5 vout1p 0 0 n12 l=0.56u w=0.5u
mt14 voutp 6 0 0 n12 l=0.56u w=0.5u
mt15 voutn 6 0 0 n12 l=0.56u w=0.5u
mt16 16 15 0 0 n12 l=0.56u w=0.5u
mt17 15 15 0 0 n12 l=0.56u w=0.5u
mt18 14 16 0 0 n12 l=0.56u w=0.5u
mt19 15 vinn 13 1 p12 l=0.56u w=0.5u
mt20 16 vinp 13 1 p12 l=0.56u w=0.5u
m21 14 ibias 1 1 p12 l=0.56u w=0.5u
mt22 13 ibias 1 1 p12 l=0.56u w=0.5u
mt23 ibias ibias 1 1 p12 l=0.56u w=0.5u
mt24 22 voutp 24 0 n12 l=0.3u w=0.29u
mt25 Out voutn 24 0 n12 l=0.3u w=0.29u
mt26 22 22 1 1 p12 l=0.3u w=0.29u
mt27 Out 22 1 1 p12 l=0.3u w=0.29u
mt28 24 vbias 0 0 n12 l=0.3u w=0.29u
vb vbias 0 dc 0.4
.tran 1n 450n start=10n sweep monte=10
.measure tran vdd_rms_pwr rms p(vdd)
.print tran v(out)
.ac dec 10 10meg 700meg
.measure tran RMS_ckt_pwr rms power
.print ac isub(out)
.noise v(out) vinp
.print noise onoise inoise
.variation
.global_variation Temp temp='30'
.end_global_variation
.end_variation
.end
```

After running the above code in the HSPICE simulator, the retrieved results are analyzed in terms of transient analysis, power, AC, noise and Monte Carlo analysis, which are detailed as follows.

3.2. Transient analysis

Transient analysis is a vital technique employed in analog circuit design to examine the dynamic behavior of a circuit over time. Its primary objective is to simulate the circuit's response to a specific input

signal and analyze the resulting output waveform. During transient analysis, a time-varying input signal is applied to the circuit, and the circuit's response is observed as the signal changes over time. The behavior of the circuit, including voltage and current waveforms, is recorded and analyzed to extract crucial characteristics such as rise time (the time taken for a signal to transition from a low to a high level), fall time (the time taken for a signal to transition from a high to a low level), settling time (the time required for the output to stabilize within a specified tolerance), and overshoot (the extent to which the output exceeds the final desired value before settling) as shown in Figure 2. By performing transient analysis, designers can evaluate the circuit's performance and ensure it meets the desired specifications. This analysis aids in identifying and addressing potential issues such as signal distortion, instability, or excessive response times, allowing for fine-tuning and optimization of the circuit's behavior.

Figure 2. Transient analysis of current reuse technique

3.3. Power analysis

Power analysis is used to assess the power consumption of a design. It involves examining the power consumed by a device when it is powered up but no signals are changing value, indicating that the transistors are not switching. In CMOS devices, this power consumption is referred to as static power and is primarily caused by leakage. Sub-threshold leakage occurs when a CMOS gate is not completely turned off. The power analysis of the proposed architecture is depicted in Figure 3.

The equation for calculating the root mean square (RMS) power, denoted as P_{vp}, in a direct current (DC) circuit is given by (1):

$$P_{vp} = \frac{{V_{vp}}^2}{R} \quad (1)$$

where P_{vp} represents the power in watts (W). V_{vp} is the voltage in volts (V) across the load or resistor. R is the resistance in ohms (ω) of the load or resistor. The measured values for power consumption are as in (2) and (3):

$$V\ dd\ rms\ power\ = 7.9748e^{-06} \quad (2)$$

$$Rms\_ckt\ power\ =\ 8.3797e^{-06} \quad (3)$$

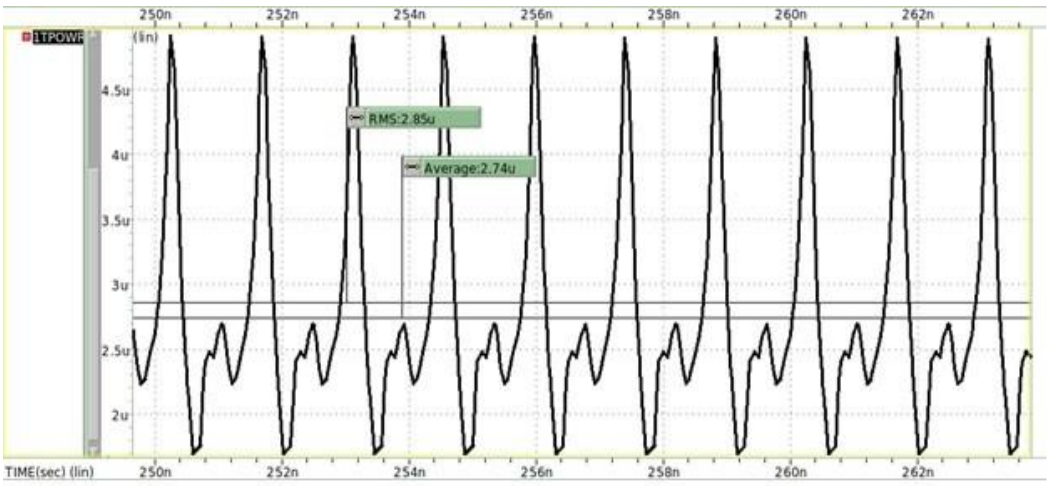

Figure 3. Power analysis of OTA

3.4. AC analysis

AC analysis is a crucial tool in electronics, enabling engineers to understand how circuits respond to various input signal frequencies. This analysis is vital for designing and optimizing filters, amplifiers, and other circuits that must function accurately at specific frequencies. By evaluating the frequency response, AC analysis helps in identifying how circuits behave under different conditions, ensuring they meet the required performance standards. Additionally, AC analysis is instrumental in determining an amplifier's gain, which is the ratio of the output voltage to the input voltage. Since an amplifier's gain can vary across different frequencies, AC analysis allows engineers to pinpoint the frequency range where the amplifier maintains its desired gain, ensuring efficient and reliable operation within the specified parameters. This comprehensive understanding is essential for developing high-performance electronic devices and systems. AC Analysis of the proposed architecture is outlined in Figure 4.

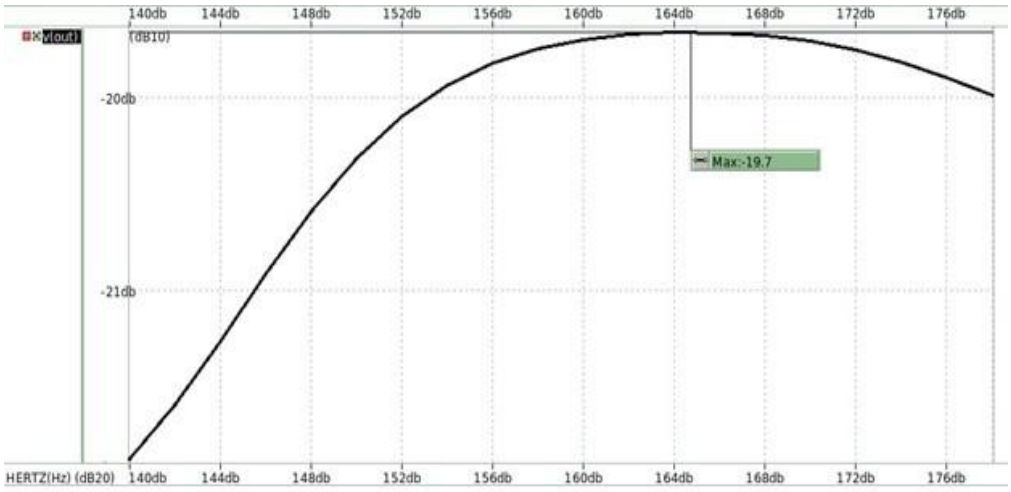

Figure 4. AC analysis of OTA

3.5. Noise analysis

Operational transconductance noise analysis (OTNA) is a technique used in electronic circuit signs to evaluate and characterize the impact of transconductance noise in operational amplifiers and other

transconductance-based circuits. Transconductance noise refers to the random fluctuations in the output current of a device caused by the thermal agitation of charge carriers. OTNA aims to predict the effects of this noise on circuit performance, such as voltage gain, signal-to-noise ratio, and distortion. Noise analysis of the proposed architecture is represented in Figure 5. The analysis begins by modelling the noise sources within the transconductance devices, considering factors like channel length modulation, flicker noise, and thermal noise. These noise sources are then expressed as spectral densities, which provide a measure of noise power over a range of frequencies. By calculating the spectral densities of the circuit's input and output currents, OTNA enables the estimation of the noise contribution at different stages. OTNA involves the application of noise modeling techniques such as the equivalent input noise model and the equivalent input noise resistance model. These models approximate the effect of transconductance noise in terms of equivalent input voltage and equivalent input resistance, respectively. By incorporating these models into the overall circuit analysis, engineers can evaluate the noise performance of the circuit and make informed design decisions.

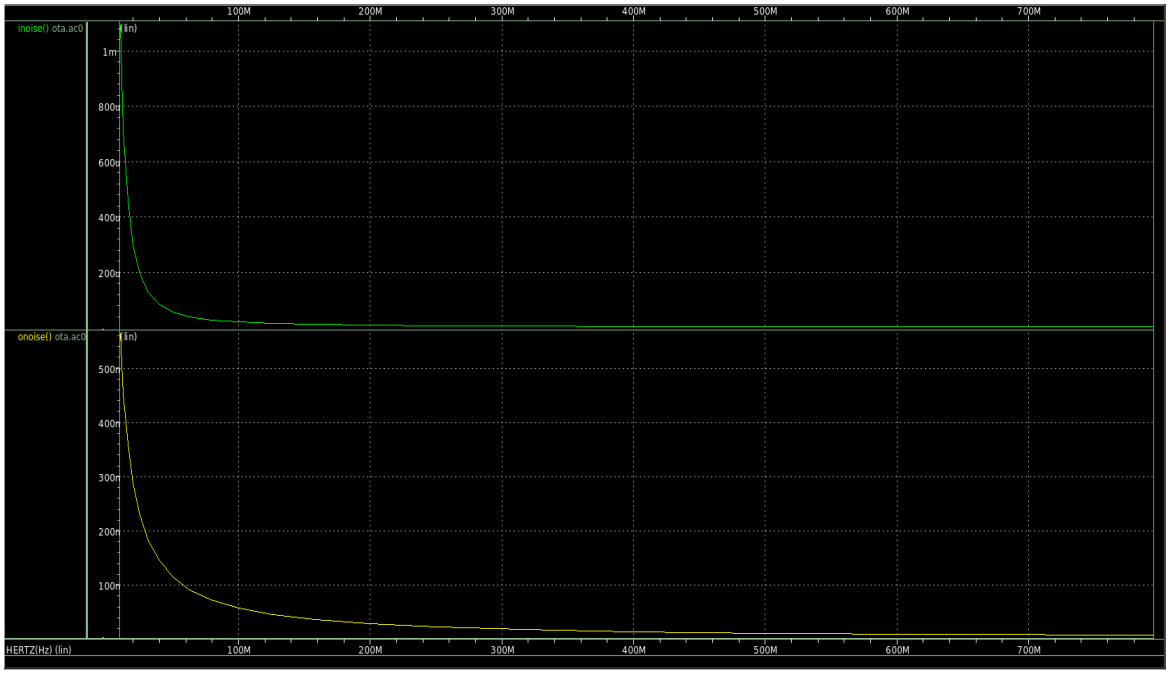

Figure 5. Noise analysis of OTA

The ultimate goal of OTNA is to assess the impact of transconductance noise on the signal integrity and overall performance of the circuit. It helps designers optimize key parameters such as bias currents, transistor sizes, and feedback configurations to minimize the impact of noise on the desired signal. By utilizing OTNA, engineers can achieve lower noise figures, improved linearity, and enhanced overall circuit performance, leading to better system design and functionality in a wide range of applications, including audio amplifiers, communication systems, and sensor interfaces.

3.6. Monte Carlo analysis

The Monte Carlo simulation is a modeling technique used to assess the probability of different outcomes in situations where accurate predictions are challenging due to the involvement of random variables. This method provides insights into the impact of risk and uncertainty. Often referred to as a multiple probability simulation, the Monte Carlo approach addresses an inherent challenge in simulation techniques. It recognizes that the precise probabilities of various outcomes cannot be determined definitively due to the influence of random variables. Therefore, the focus is on repeatedly generating random samples. In a Monte Carlo simulation, an uncertain variable is assigned a random value, and the model is executed to produce a result. This process is repeated numerous times, each time assigning different values to the variable under consideration. Once the simulation is finished, the results are averaged to obtain an estimate. The proposed work Monte Carlo simulation and histogram output are illustrated in Figures 6 and 7.

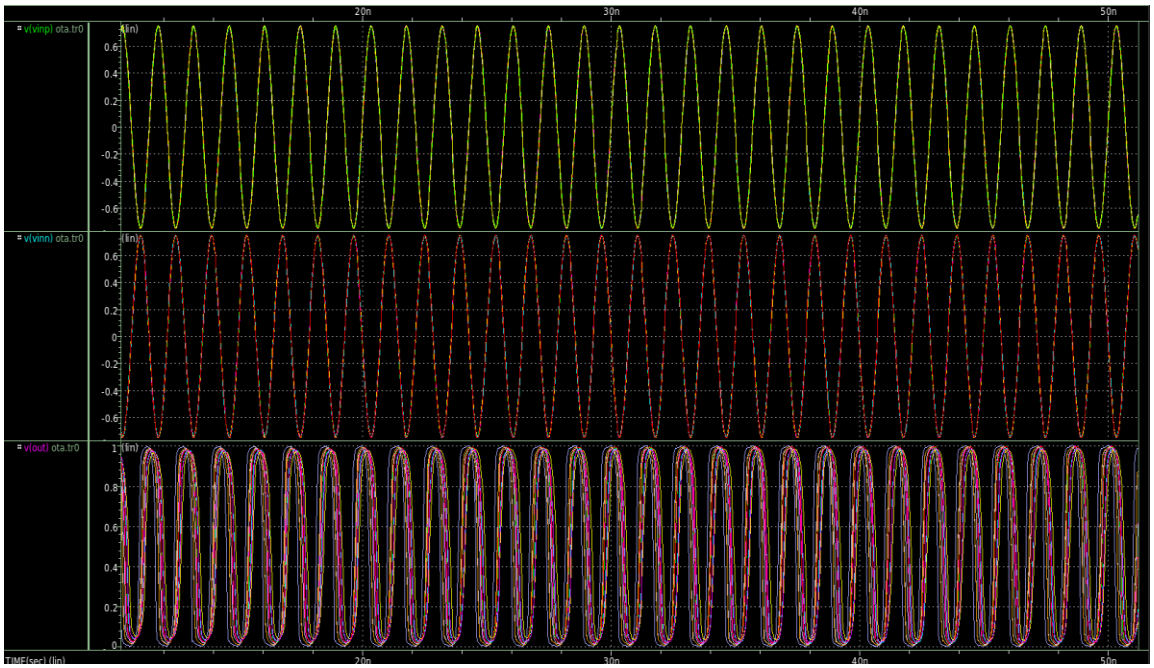

Figure 6. Monte Carlo simulation

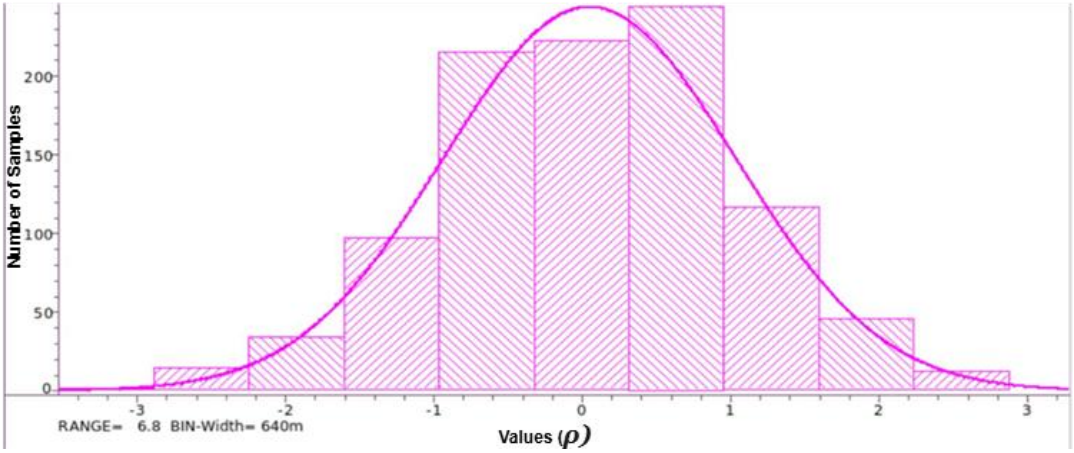

Figure 7. Histogram output

4. DISCUSSION AND RESULT ANALYSIS WITH EXISTING STATE-OF-THE-ART

The development of implantable medical devices demands a rigorous approach to circuit design, primarily focusing on minimizing power consumption and optimizing noise efficiency. This paper thoroughly explores an innovative microwatt-level ECG analog circuit designed to address these critical challenges. The core challenge in designing implantable medical devices is ensuring unobtrusiveness and longevity, necessitating circuits with exceptionally low power consumption and high noise efficiency. Traditional designs often face trade-offs between these two parameters, but the proposed circuit leverages the current reuse technique to effectively balance and enhance both aspects. Recycling the current within the circuit reduces the overall power consumption without compromising performance, a crucial advancement for extending the operational life of implantable devices.

The choice of 90 nm CMOS technology plays a pivotal role in the circuit's implementation. This technology node offers several advantages, including reduced leakage current and improved scaling, which are essential for achieving low power consumption. The circuit's design process involved extensive simulations to validate its performance, with a specific focus on noise and power metrics. Simulation results demonstrate that at 100 Hz frequency pertinent to ECG signals, the noise performance of the circuit reaches an impressive

62.095 nV/√*Hz*. This low noise is crucial for maintaining signal integrity and ensuring accurate ECG readings, which are vital for patient monitoring. The power consumption is also measured at a mere 8.3797 µW, a significant reduction compared to existing designs. This ultralow power consumption ensures that the implantable device can operate for extended periods without frequent battery replacements, thereby enhancing patient convenience and device reliability. The result analysis of the proposed method with the existing state-of-the-art methods in terms of supply voltage, current, noise, gain, power, and technology are represented in Table 1.

Table 1. Result analysis

Parameters	Proposed	[7]	[22]	[28]
Supply voltage(V)	0.4	0.9	1	0.7
Noise	0.6860	1.46	1.22	4.11
Gain(db)	51.2	47.66	40.74	38.9
Power(W)	2.85u	3.7u	11.9u	4.32u
Technology	0.90um	0.35um	0.35um	0.5um

5. CONCLUSION

The research presented in this paper marks a significant advancement in the design of implantable medical devices, particularly through the development of a microwatt-level ECG analog circuit that excels in both low power consumption and noise efficiency. By leveraging the current reuse technique and implementing the circuit using 90 nm CMOS technology, we have demonstrated that achieving substantial improvements in these critical parameters is possible, addressing longstanding challenges in the field. The proposed work introduces a novel capacitive feedback amplifier that addresses the specific needs of ECG recordings by achieving low noise and low power consumption. The amplifier design is based on a current-reused OTA. To optimize power-to-noise efficiency, the OTA incorporates inverter-based differential pairs in its first stage. This choice improves the trade-off between power consumption and noise performance, which is crucial for accurate ECG signal acquisition. Furthermore, a class-AB output stage is employed to enhance the amplifier's gm/I (transconductance per unit current) efficiency. The OTA is implemented using advanced 90 nm CMOS technology, leveraging the benefits of scaled-down transistor dimensions. Through extensive measurement and evaluation, the research team demonstrates that the proposed amplifier exhibits exceptional performance in terms of power consumption and noise characteristics. The amplifier effectively meets the requirements for capturing high-quality ECG signals. By presenting this low noise and low power capacitive feedback amplifier, the paper contributes to the advancement of ECG recording technology. The amplifier's ability to achieve good performance in terms of power efficiency, noise reduction, and accurate ECG signal recording highlights its potential for various healthcare and biomedical applications.

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BIOGRAPHIES OF AUTHORS

Udari Gnaneshwara Chary received his master's degree in 2009 in VLSI systems design from Jawaharlal Nehru Technological University Hyderabad. He works as an assistant professor at the B.V. Raju Institute of Technology. Pursuing Ph.D. at Koneru Lakshmaiah University (KLEF). He had 14 years of teaching experience. His research interests include CMOS analog design, VLSI system design, and quantum computing. He can be contacted at email: gnaneshwarchary@gmail.com.

Kakarla Hari Kishore born in Vijayawada, Andhra Pradesh, India. He received B.Tech. (ECE) from JN-TUH, M.Tech. from SK University, Andhra Pradesh, India. He received his Ph.D. in VLSI from Koneru Lakshmaiah Education Foundation. He received his Postdoctoral Fellowship (PDF) in Malaysia. At present, he is working as professor in ECE. He has published 3 IEEE Transactions and more than 121 research articles published in international journals/conferences with an H-index of 33. He has filled and published 07 patents and 03 Textbooks published. He is editorial board member/reviewer for several international journals/conferences. His research interests include VLSI design, fault tolerance and digital testing, IoT, communications, and signal processing. He is a life member of ISTE and IE. He can be contacted at email: kakarla.harikishore@kluniversity.in.