Five-level three phase cascaded H-bridge inverter using digital signal processor control for renewable energy applications

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Article Info

Article history:

Received Apr 13, 2024
Revised Oct 25, 2024
Accepted Nov 20, 2024

Keywords:

Cascaded H-bridge
Five level three phase inverters
Multilevel inverter
Renewable energy
Total harmonic distortion

ABSTRACT

This article presents a five-level three-phase cascaded H-bridge inverter for renewable energy applications, aimed at reducing total harmonic distortion (THD) and enhancing efficiency. The inverter uses a digital signal processing board, TMS320F28335, to generate pulse-width modulation signals through MATLAB/Simulink, ensuring precise control. The experimental setup includes an 84 VDC input voltage and a 300-watt load. Simulation and experimental results closely align, validating the accuracy of the simulation model. The output voltage shows a stepped pattern characteristic of multilevel inverters, significantly reducing harmonic distortion. THD analysis reveals a substantial reduction at higher modulation indices, with particularly low THD at a modulation index of 0.95. Consistent THD levels across modulation indices of 0.5, 0.8, and 0.95 demonstrate robust performance under varying conditions. Comparative analysis indicates that the proposed inverter achieves lower THD levels than traditional inverters, enhancing power quality and system efficiency. The five-level three-phase cascaded H-bridge inverter offers a promising solution for renewable energy applications by significantly reducing THD and improving power quality. Its robust performance and scalability potential contribute valuable advancements to renewable energy systems.

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1. INTRODUCTION

The global adoption of renewable energy sources has gained substantial traction in recent years due to escalating environmental concerns and the recognition of the finite nature of traditional energy reservoirs. Governments, industries, and academic institutions worldwide are increasingly prioritizing the transition to renewable energy to mitigate the adverse impacts of climate change and ensure a sustainable energy future. Solar, wind, and other renewable energy sources are being integrated into the power grid, but their effective utilization presents significant challenges, particularly in power conversion and grid integration. These challenges arise from the intermittent nature of renewable energy sources, variations in power output, and the need for efficient and reliable power electronic circuits [1], [2].

In response to these challenges, there is a critical need for developing advanced power electronic circuits that can harness renewable energy inputs with precision and efficiency. Power inverters, which convert direct current (DC) from renewable sources into alternating current (AC) for grid use, play a pivotal role in this process. Traditional inverters, commonly used in renewable energy systems, often struggle with constraints such as voltage regulation, harmonic distortion, and energy losses. These issues impede the performance and reliability of renewable energy systems, necessitating improvements in inverter technology [3].

Previous studies have explored various multilevel inverter topologies and their advantages [4]–[7]. For instance, Vemuganti *et al.* [8] conducted a survey on reduced switch count multilevel inverters, highlighting their efficiency and reduced complexity. Their research underscored the potential of multilevel inverters to provide superior performance in renewable energy systems. Kadhim and Hasan [9] examined the enhancement of power stability and efficiency using multilevel inverter technology based on renewable energy sources. Their findings indicated that multilevel inverters, such as the five-level H-bridge architecture, offer enhanced output waveform fidelity, reduced switching losses, and increased efficiency, making them suitable for modern renewable energy applications.

Despite these advancements, there remain unresolved issues in achieving optimal voltage regulation and minimizing harmonic distortion in renewable energy applications. Traditional inverters often exhibit significant total harmonic distortion (THD), which can adversely affect the quality of power delivered to the grid and reduce the lifespan of electrical components [10], [11]. This paper addresses these challenges by presenting a five-level three-phase cascaded H-bridge inverter design that focuses on reducing THD and improving power conversion efficiency, thereby advancing the reliability and quality of renewable energy systems. The proposed circuit employs two sets of H-bridge inverters connected in series, each with separate power sources. The control circuitry utilizes phase disposition-pulse width modulation (PD-PWM) techniques for switching, employing a TMS320F28335 digital signal processor (DSP) board in conjunction with MATLAB/Simulink software to generate PWM signals. This configuration aims to enhance power conversion efficiency, reduce harmonic distortion, and facilitate seamless integration with existing grid infrastructures. The five-level structure of the inverter is particularly advantageous as it provides higher voltage levels, improved output waveform quality, and reduced electromagnetic interference compared to conventional two-level inverters.

This research presents several new contributions: a novel five-level three-phase H-bridge inverter circuit configuration for improved power conversion efficiency; implementation of a PD-PWM technique using a DSP board and MATLAB/Simulink for precise control; and comprehensive analysis of the THD levels to validate the performance improvements. The innovative aspects of this study include the use of separate power sources for each H-bridge set, which enhances the modularity and scalability of the inverter system, and the employment of advanced control algorithms to optimize the switching sequences and minimize power losses. The subsequent sections of this manuscript will elaborate on the design, implementation, and evaluation of the proposed inverter circuit, demonstrating its potential to enhance the performance and reliability of renewable energy systems. By addressing the critical challenges of power conversion and grid integration, this research aims to contribute to the broader adoption of renewable energy technologies and support the global transition towards a more sustainable energy future.

2. METHOD

This study presents a 5-level three-phase H-bridge inverter of the cascaded-cell type for renewable energy sources. The methodology encompasses a detailed analysis of the power circuit and modulation techniques, focusing on PWM control. Additionally, harmonic distortion analysis is conducted to assess the waveform quality. The experimental setup employs a THD board and MATLAB/Simulink software for signal generation and analysis.

2.1. Cascaded H-bridge five-level inverter

Multilevel inverters (MLIs) are widely used in current applications, primarily consisting of three main types: i) Neutral point clamped multilevel inverters (NPCMLI), also known as the diode clamped multilevel inverters (DCMLI), produces multiple voltage steps by using diodes to clamp voltages at specific levels; ii) Flying capacitor multilevel inverters (FCMLI) uses capacitors to produce a range of voltage levels, improving the quality of the waveform; and iii) Cascaded H-bridge multilevel inverters (CHBMLI) for multi-level voltage output [4], [12]–[16]. Additionally, there are several other types of multilevel inverters, such as the generalized multilevel inverter [17]–[19], mixed-level hybrid multilevel inverter [20], and back-to-back diode-clamp multilevel inverter [21], among others.

In this article, we choose a cascaded H-bridge multilevel inverter [22]–[25]. The single-phase five-level CHBMLI, composed of two H-bridges, utilizes a cascaded inverter with separate DC sources (SDCSs) to synthesize voltage from multiple DC voltage sources. Figure 1 illustrates the Two H-bridge consisting of 8 MOSFET switches, with each H-bridge comprising 4 MOSFET switches. The operational principle of

CHBMLI entails three output voltage levels: +Vdc, 0, and -Vdc, which are connected to the DC power supply to convert into AC electricity through the independent circuit connection of switches. When switches S_{11} and S_{14} are in the on state, switches S_{12} and S_{13} will receive a voltage of +Vdc, conversely, when switches S_{12} and S_{13} are on, switches S_{11} and S_{14} will receive a voltage of -Vdc. However, if switches S_{11} and S_{13} or S_{12} and S_{14} are simultaneously on, the output voltage will be 0. The output voltage is a cumulative effect of the voltage generated in each cell. The number of output voltage levels is 2*(m+1), where m is the number of cells. The output voltage of the CHB inverter leg is increased by the addition of the output voltage of the H-bridge [6], [26], [27].

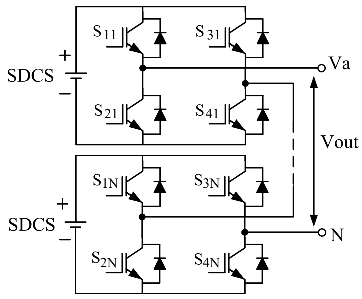


Figure 1. Single phase N-level CHBMLI topology [6]

The number of levels in cascaded H-bridge multilevel inverters is related to the input DC voltage source or the number of cells in an H-bridge inverter, which can be expressed as (1).

$$m = 2s + 1 \quad (1)$$

The number of switch devices in cascaded H-bridge multilevel inverters is related to the number of voltage levels of the output AC voltage, given by (2).

$$n = 2 \times (m - 1) \quad (2)$$

For the number of levels of the output phase voltage, it can be determined by (3).

$$m_P = 2s + 1 \quad (3)$$

The number of levels of the output line-to-line voltage can be found from (4).

$$m_L = 4s - 1 \quad (4)$$

Calculating the output phase voltage magnitude of the inverter can be achieved by (5).

$$V_{AN} = V_{dc1} + V_{dc2} + \ldots + V_{dc(S-1)} + V_{dcs} \quad (5)$$

where m_P is the number of levels of the output phase voltage of the inverter. m_L is the number of levels of the output line-to-line voltage of the inverter, and s is the number of input DC voltage sources.

2.2. Power circuit and modulation techniques of multilevel inverters

2.2.1. Power circuit

In this research, a five-level three-phase H-bridge inverter of the cascaded-cell type, which offers advantages such as a simple circuit structure, ease of design, high-quality output voltage, and low harmonic distortion, is selected. It is suitable for driving electric motors with high power ratings. Figure 2 illustrates the circuit topology proposed in this study, comprising two independent DC power sources, each rated at 84 VDC. Each set of these power sources feeds into the power circuit of the five-level three-phase H-bridge inverter, with each cell of the H-bridge comprising two sets. This configuration results in an output voltage waveform resembling a step ladder, facilitating its compatibility with AC load applications. The control circuit employs a TMS320F28335 DSP board in conjunction with MATLAB/Simulink software to generate

12 sets of PWM signals, which are then fed into the inverter circuit through the gate drive circuit, dead-time circuit, and ground separation circuit. This ensures signal integrity and safeguards against potential damage to components within the circuit.

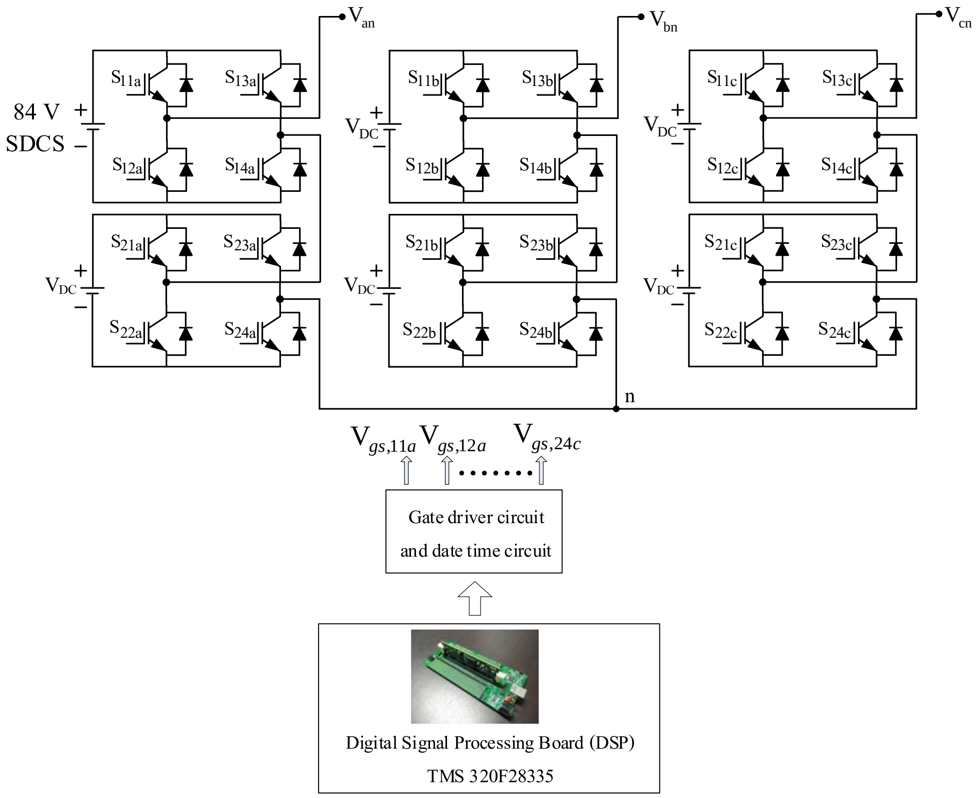


Figure 2. Power circuit of the five-level three-phase H-bridge cascaded-cell inverter used in the research article

2.2.2. Modulation techniques of multilevel inverters

The PWM technique used to control the power circuit of multilevel inverters employs modulation between a reference signal and a triangular carrier wave. The width of the PWM signal depends on the amplitude of the reference signal compared to the amplitude of the carrier wave. Figure 3 illustrates the modulation techniques used in the inverter design, with Figure 3(a) showing the PWM signal modulation process using a reference signal and triangular carrier wave, and Figure 3(b) depicting the three-phase carrier-based POD PWM technique for minimizing harmonic distortion, expressed by (6).

$$\frac{T_P}{T_C} = A \,;\, 0 \leq A \leq 1 \tag{6}$$

where T_P is the pulse width of the output signal. T_C is the period of the carrier wave. A is the amplitude of the reference signal.

The output phase voltage of the five-level three-phase H-bridge cascaded-cell inverter circuit correlates with the modulation index (m) and the V_{dc}, as defined by (7).

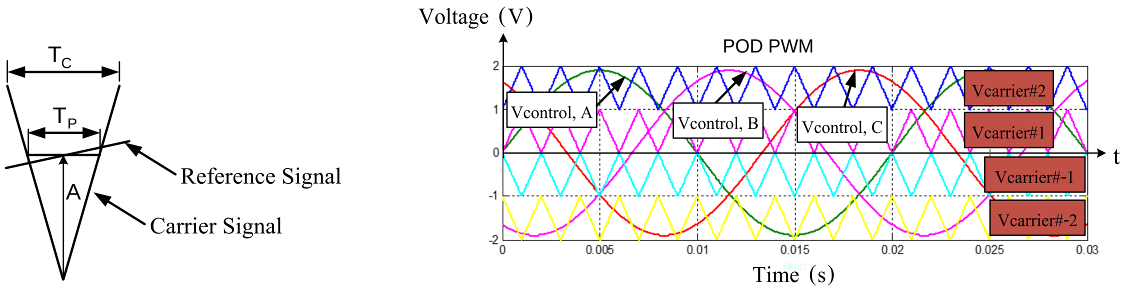
$$V_{1,Peak} = m_a \cdot V_{dc} \,;\, (m_a \leq 1) \tag{7}$$

$$V_{dc} = sE \tag{8}$$

where E is the sub-inverter voltage level. s is the number of input DC voltage sources per phase. The number of carrier waves can be obtained from (9).

$$n_c = n - 1 \tag{9}$$

where n_c is the number of carrier waves. n is the number of levels of the output phase voltage. The circuit generates double-edge PWM signals using a digital signal processor board TMS320F28335 in conjunction with MATLAB/Simulink software, as depicted in Figure 4.



(a) (b)

Figure 3. The modulation techniques used in the inverter design (a) relationship between reference signal and carrier signal (b) three-phase carrier-based POD PWM techniques

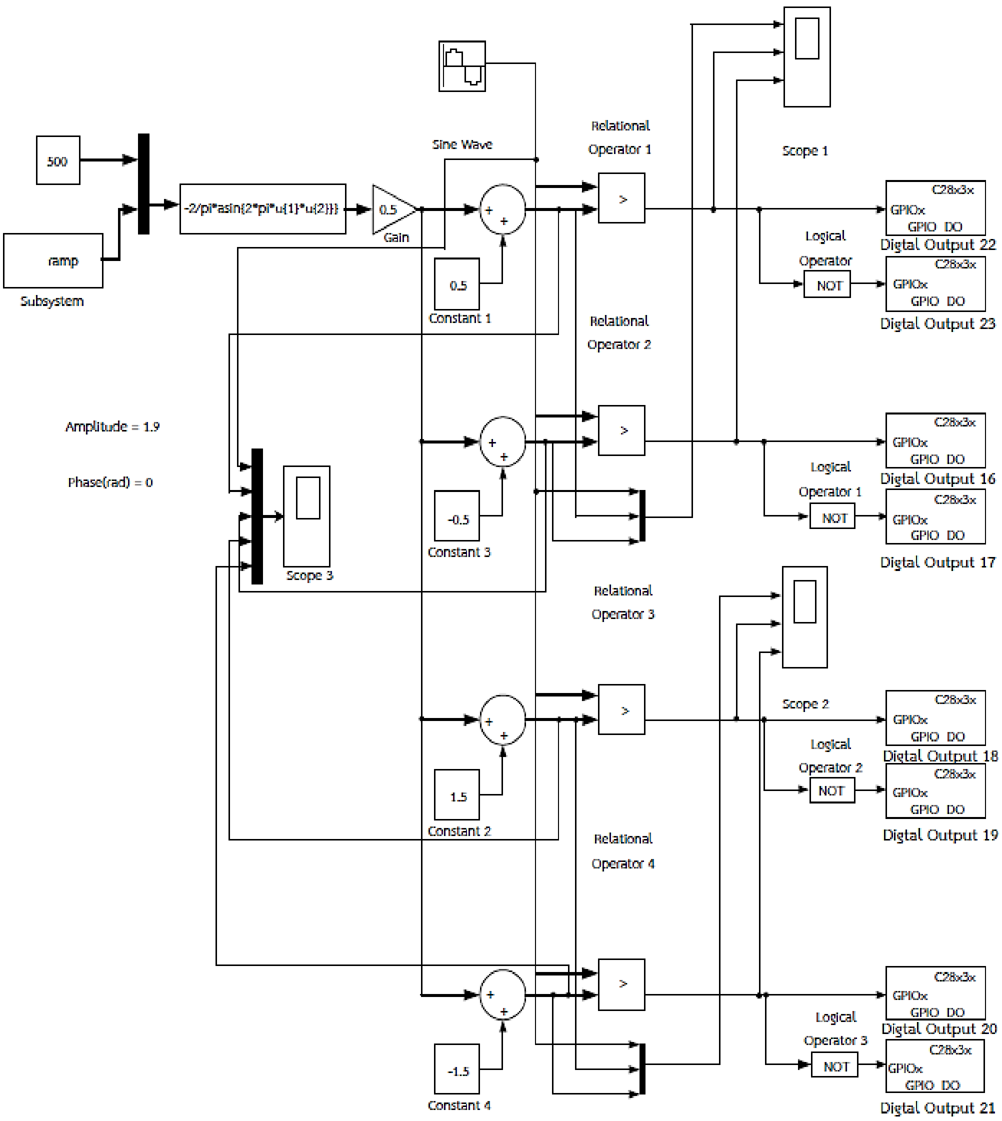


Figure 4. Generation of sinusoidal PWM signals using a DSP board with MATLAB/Simulink

2.2.3. Harmonic distortion analysis

Multilevel inverter circuits produce output voltages that closely resemble sinusoidal waveforms but may contain harmonic distortions. Therefore, the waveform with such distortions can be analyzed using Fourier series analysis theory. The analysis of non-sinusoidal waveforms and periodic signals with a fundamental frequency can be defined by the Fourier series as (10):

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty}(a_n \cos n\,\omega t + b_n \sin n\,\omega t) \quad (10)$$

When the Fourier coefficient is:

$$a_n = \frac{1}{\pi}\int_0^{2\pi} f(t)\cos(n\omega t)\, d(\omega t), n = 0,1,2,\dots,\infty \quad (11)$$

$$b_n = \frac{1}{\pi}\int_0^{2\pi} f(t)\sin(n\omega t)\, d(\omega t), n = 0,1,2,\dots,\infty \quad (12)$$

Alternatively, we can express it as (13):

$$f(t) = C_o + \sum_{n=1}^{\infty} C_n \cos(n\omega t + \theta_n) \quad (13)$$

where:

$$\left.\begin{aligned} C_0 &= a_0 \\ C_n &= \sqrt{a_n^2 + b_n^2} \\ \theta_n &= \tan^{-1}\frac{b_n}{a_n} \end{aligned}\right\} \quad (14)$$

Finally, we obtain the Fourier coefficients in (14), which can be used to determine the total harmonic distortion of the current and output voltage, given by (15).

$$\left.\begin{aligned} \mathrm{THD}_I &= \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \\ \mathrm{THD}_V &= \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \end{aligned}\right\} \quad (15)$$

where I_1 is the amplitude of the current harmonic order 1. V_1 is the amplitude of the voltage harmonic order 1. I_n is the amplitude of the current harmonic order n. V_n is the amplitude of the voltage harmonic order n.

Based on the voltage waveform illustrated in Figure 5, we apply (10)-(14) to perform a detailed Fourier series analysis, which helps in breaking down the waveform into its fundamental and harmonic components. By calculating the Fourier coefficients from these equations, we can precisely quantify the individual harmonic contributions present in the waveform.

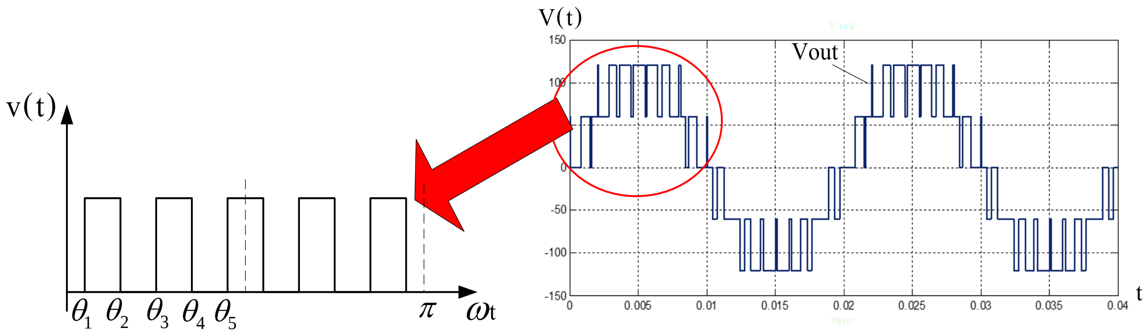


Figure 5. Analysis of the total harmonic distortion of the output voltage waveform

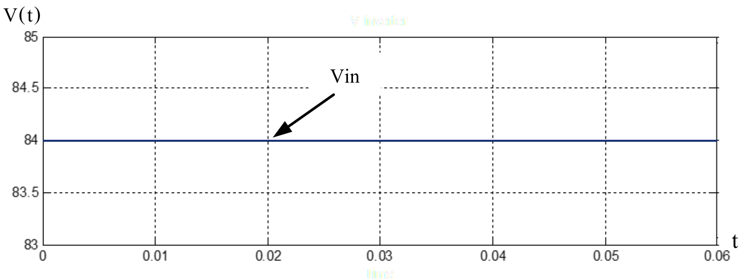
3. RESULTS AND DISCUSSION

The experimental setup of the five-level three-phase H-bridge inverter circuit involves the integration of various components. These components include the power circuit section, control circuit section, direct current power supply, a 300-watt load (light bulb), and measuring instruments. The prototype setup, as depicted in Figure 6, incorporates a circuit that generates PWM signals utilizing a digital signal processing board, TMS320F28335, through MATLAB/Simulink software. These PWM signals are then outputted through the digital output port of the board.

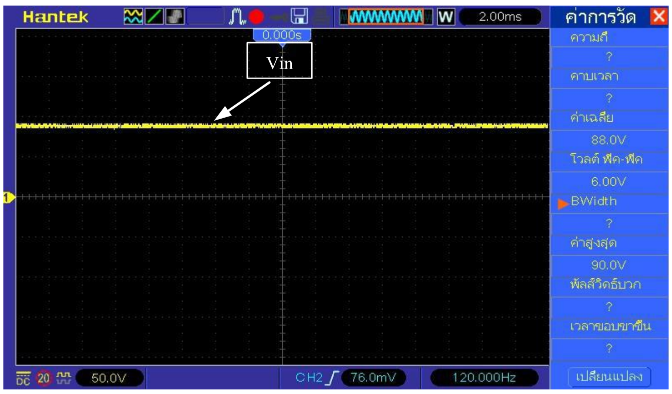
Figure 6. The prototype circuit constructed for this experiment

3.1. Input voltage analysis

The circuit is supplied with an 84 VDC input voltage from a battery consisting of seven 12 VDC cells. Figure 7 shows the DC voltage at the input, comparing simulation in Figure 7(a) and experimental results in Figure 7(b). The close match between the simulated and experimental data confirms the accuracy of the simulation model in replicating real-world conditions. This consistency is crucial as it validates the reliability of our experimental setup.



(a)

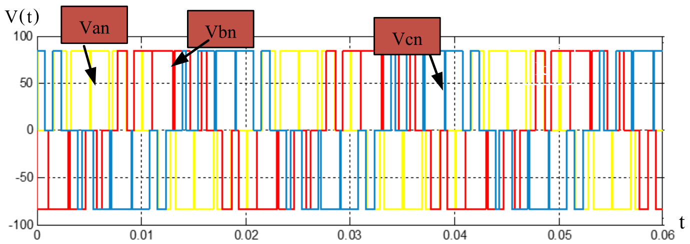


(b)

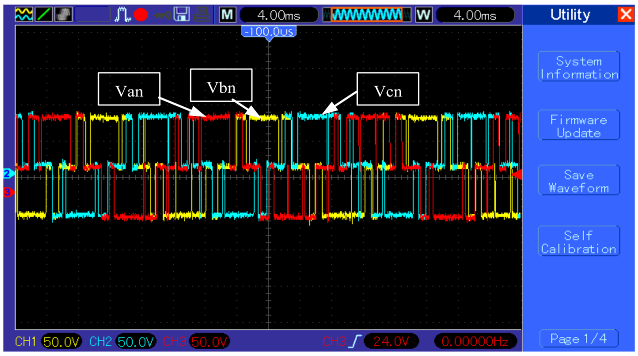
Figure 7. Input voltage (a) simulation and (b) experimental results

3.2. Output voltage

Figure 8 presents the output voltage for both simulation in Figure 8(a) and experimental results in Figure 8(b). The waveforms illustrate a stepped voltage pattern characteristic of multilevel inverters, which helps in reducing harmonic distortion. Figure 9 shows the output phase voltage and current at a load of 300 Watts, comparing simulation in Figure 9(a) with experimental results in Figure 9(b). The agreement between these results further substantiates the model's reliability and the efficiency of the PWM control strategy employed.

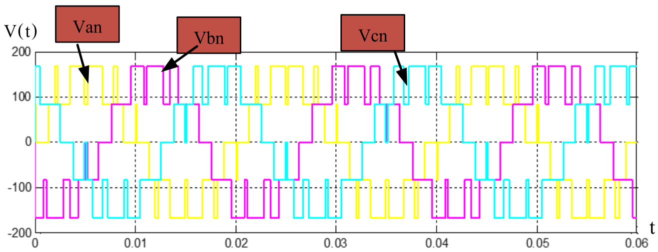


(a)

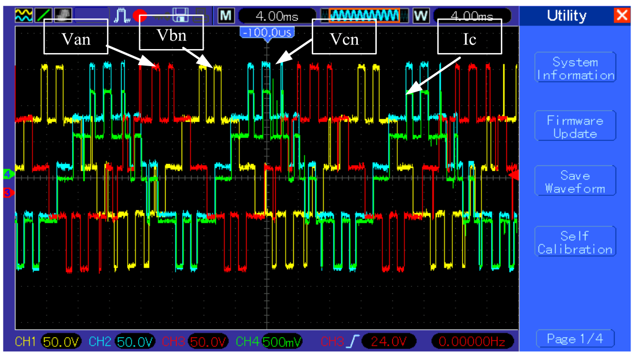


(b)

Figure 8. Output phase voltage operating at three-level (a) simulation and (b) experimental results



(a)



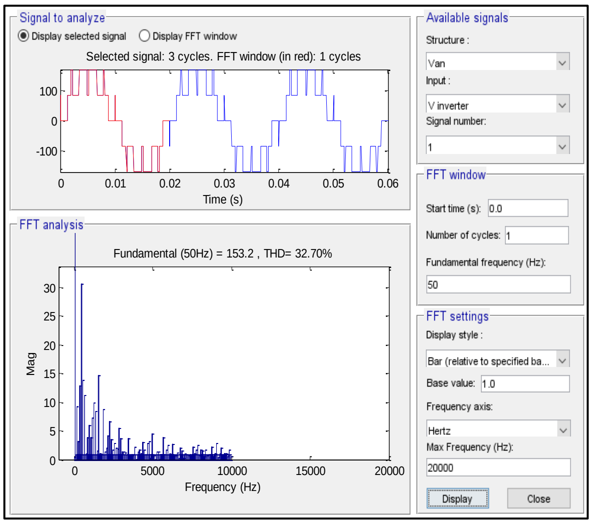
(b)

Figure 9. Output phase voltage operating at five-level (a) simulation and (b) experimental results

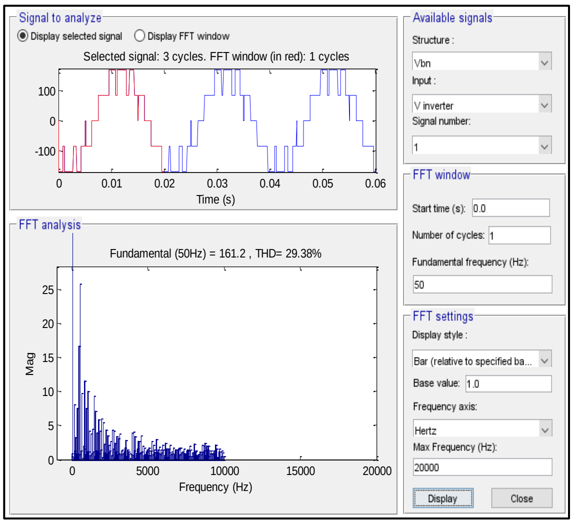
3.3. Harmonic distortion analysis

Total harmonic distortion of the output voltage is a critical parameter in assessing inverter performance. Figure 10 illustrates the output voltage and THD from the simulation at a modulation index (m) of 0.95, with Figure 10(a) showing the phase voltage V_{AN}, Figure 10(b) displaying the phase voltage V_{BN}, and Figure 10(c) depicting the phase voltage V_{CN}. The observed THD levels in the simulation indicate a significant reduction compared to conventional inverter designs. Figures 11(a) and 11(b) show the line voltage from the simulation at modulation indices of 0.5 and 0.8, respectively, providing insights into the performance across different operating conditions. This reduction in THD is pivotal for enhancing the quality of power delivered to the grid, reducing potential disturbances.

Table 1 shows the correlation between the modulation index and the total harmonic distortion for phases V_{AN}, V_{BN}, and V_{CN} obtained from the simulation. As the modulation index increases, the THD decreases significantly, especially in the linear modulation range. For instance, at a modulation index of 0.10, the THD values for phases V_{AN}, V_{BN}, and V_{CN} are extremely high, approximately 240%. However, as the modulation index increases to 1.00, the THD values drop to 30.52%, 23.63%, and 23.86%, respectively. This trend continues in the over modulation range, with the THD values slightly increasing at higher modulation indices but remaining significantly lower than the initial values.



(a)



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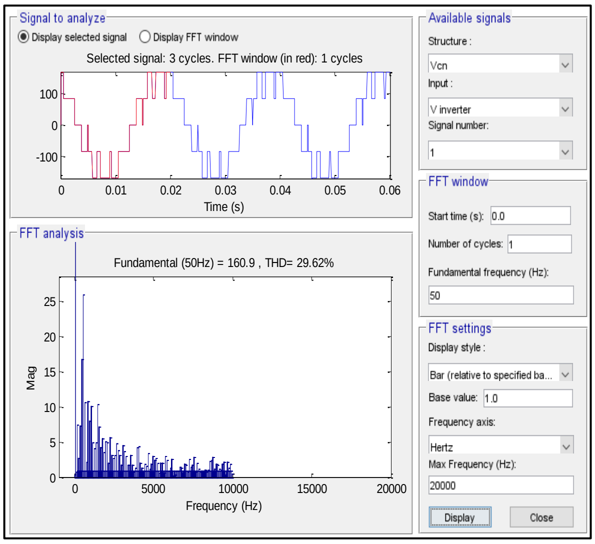
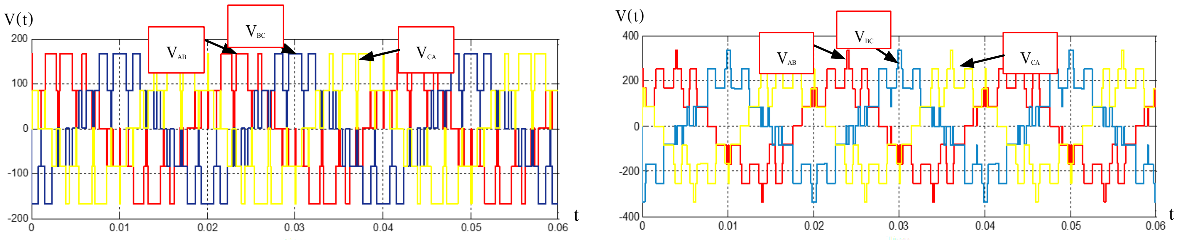


(c)

Figure 10. Output phase voltage and total harmonic distortion from the simulation at $m_a = 0.95$ (a) phase voltage V_{AN} (b) phase voltage V_{BN} and (c) phase voltage V_{CN}



(a) (b)

Figure 11. Output line-to-line voltage from the simulation using MATLAB/Simulink (a) $m_a = 0.5$ and (b) $m_a = 0.8$

Table 1. The correlation between the modulation index and the total harmonic distortion obtained from the simulation

Modulation Index (m_a)	(THD%) PhaseV_{AN}	(THD%) PhaseV_{BN}	(THD%) Phase V_{CN}	Operating status of the H-bridge cells	The modulation index range
0.10	240.99	242.36	242.47	Cells 1 active Cell 2 inactive	Linear modulation
0.25	126.62	128.20	128.23		
0.50	50.24	53.84	54.99		
0.75	36.35	41.75	41.77		
1.00	30.52	23.63	23.86		
1.50	23.60	23.82	23.86	Cells 1 and 2 are active	Over modulation
3.24	31.99	35.57	35.57		
3.50	33.92	35.72	36.18		

3.4. Discussion

When comparing our results with previous studies, we observe a marked improvement in the harmonic performance of our proposed inverter design [28]–[30]. The proposed technique, leveraging the capabilities of the TMS320F28335 DSP board for precise PWM control, achieves lower THD, thus enhancing overall system performance. This finding aligns with recent literature, where advanced control algorithms have shown promise in improving inverter outputs. However, our study uniquely combines these algorithms with a cascaded H-Bridge topology, presenting a novel approach to THD reduction.

The proposed five-level three-phase cascaded H-bridge inverter has been tested under a 300 W load, but its performance at higher power levels is important to consider for broader applications. Based on the design and the modular nature of the inverter, it is expected to scale effectively to handle higher loads while maintaining its benefits, such as reduced THD and improved power conversion efficiency. At higher loads, the inverter is still expected to produce a stepped output waveform, characteristic of multilevel inverters, which helps maintain low THD levels. However, as the current increases with larger loads, there may be a slight increase in harmonic content, although the THD is expected to remain significantly lower than traditional two-level inverters. For instance, at a modulation index of 1.0, the inverter achieved a THD of 23.63% at 300 W, and similar levels are anticipated at higher loads due to the multilevel output design.

In terms of efficiency, the inverter's performance is strongly tied to switching frequency and load. At higher loads, efficiency may decrease slightly due to increased switching losses and thermal stress on the components. However, the cascaded H-bridge configuration helps to distribute thermal stress across multiple cells, which reduces the likelihood of efficiency loss. To ensure continued high efficiency and long-term reliability at higher power levels, advanced thermal management solutions, such as heat sinks or active cooling, should be considered, especially when scaling the inverter for larger renewable energy systems.

4. CONCLUSION

This study introduces a five-level three-phase cascaded H-bridge inverter specifically designed for renewable energy applications. The primary focus was on reducing THD and improving power conversion efficiency. The results demonstrate that the proposed inverter achieves a significant reduction in THD, particularly with a THD level of 23.63% at a modulation index of 1.0. Additionally, the experimental results closely match the simulation data, confirming the accuracy and reliability of the design. The modular architecture of the inverter allows for easy scalability, making it suitable for small- and large-scale renewable energy systems, thereby improving power quality and system reliability.

The significance of this study lies in its contribution to the field of renewable energy systems, where traditional inverters often face challenges related to high THD and limited efficiency. The proposed inverter, with its cascaded H-bridge design, offers a practical solution to these problems by producing a higher quality output waveform, reducing switching losses, and improving energy conversion efficiency. This makes the inverter highly adaptable for various renewable energy applications, from small-scale residential systems to larger commercial grid-connected systems.

However, this study does have certain limitations. The inverter's performance was experimentally validated at a 300 W load, and its behavior under higher loads was not tested in practice. While the results indicate that the inverter can scale to larger loads, future experiments are necessary to verify this. Additionally, the control algorithms used in this study, though effective, could be further optimized to enhance performance under dynamic and variable load conditions. The study also does not address long-term reliability and the overall cost of implementation, which are critical considerations for large-scale deployment.

For future research, it is recommended to explore the optimization of control algorithms to improve the inverter's performance under more dynamic load conditions and varying renewable energy sources. Further testing of the inverter under higher power levels and different types of renewable energy, such as wind and hydroelectric, would provide additional insights into its broader applications. It would also be beneficial to investigate advanced thermal management techniques and fault-tolerant designs to ensure the reliability of the inverter in large-scale renewable energy systems. Moreover, integrating the inverter with energy storage systems could enhance energy management and grid stability.

ACKNOWLEDGEMENTS

This research was made possible by the kind support of the Research and Development Institute of Nakhon Pathom Rajabhat University, and Creating Innovation for Sustainable Development Research Center, Nakhon Pathom Rajabhat University, Nakhon Pathom, Thailand

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