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Improvement of Philips MOS model 9 radio frequency performance with circuit level parasitic compensation

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ABSTRACT

The two circuit-level parasitic compensation techniques for the Philips metal oxide semiconductor (MOS) model 9 metal oxide semiconductor field effect transistor (MOSFET) at high frequencies (in the GHz range) are presented in this paper. The first method involves connecting the series resonant LC circuit in parallel to the drain and grounded source/bulk of the MM9; the second method involves connecting two of these MM9s in parallel to increase the drain current at higher frequencies along with parasitic compensation. Using these compensatory techniques, it is possible to reduce the impact of drain-source parasitic capacitance on MOS model 9 by preventing the short circuit of MOSFET terminals at high frequencies. After adjustment, improvements were seen in a number of metrics, including output impedance, S-parameters, output power and stability. Finally, using a 10 dBm source power, these parasitic compensation techniques are applied to a single and two stage basic class-E power amplifier and simulated at 1.7 and 1.1 GHz, respectively. Improvements are noted in multiple performance parameters, including power Gain (16.5 dB), drain Efficiency (83%), power added efficiency (85.82%), output power (26 dBm), good Stability (K=2.23, B>0), and S-parameters (S11=-9.22 dB, S12=-39.78 dB, S21=16.38 dB, and S22=1.41 dB) in two-stage cascade power amplifier.

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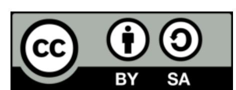

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1. INTRODUCTION

High frequency applications are needed these days to get the fastest data rates possible while using tiny antennas. However, the design of the metal oxide semiconductor field effect transistor (MOSFET) circuits for the transmitter and receiver presents a high frequency challenge. The main factor that degrades the MOSFET's overall performance at giga hertz (GHz) range is parasitic components [1]. Rather than limiting the influence of parasitic elements, a great deal of effort has been done on the extraction/modeling of parasitic components [2]–[6] and the impact of parasitic elements [7]–[9] on MOSFET operation. Typically, device level modeling or circuit level modeling can be used to compensate for parasitic elements at high frequencies in MOSFET.

When it comes to device level modeling, the impact of parasitic elements can be minimized with i) gate all around field effect transistor (GAAFET) technology [10]; ii) A tall gate stem for a Gallium Nitride high electron mobility transistor (GaN HEMT) [11]; iii) Sidewall spacers have an insulator layer made of a low k dielectric material covering them, and they have an optimum cross-sectional form [12], [13]; and iv) a silicon carbide (SiC) MOSFET with a recessed source trench and an integrated metal oxide semiconductor

(MOS)-channel diode [14]. However, the influence of parasitic elements can be mitigated in circuit level modeling through the following methods: i) Using the low gate turn off impedance driver methodology to reduce the MOSFET's common source parasitic inductor [15]; ii) Using a cross-coupled arrangement, input matching with a three-coil transformer compensates for the parasitic capacitance of the gate to the source [16]; and iii) A large number of stacked complementary metal oxide semiconductor field effect transistors (CMOS FETs) can prevent body effect transconductance degradation and reduce parasitic capacitances influence on overall operation [17]. The preceding circuit-level modeling research focuses on either parasitic capacitance or parasitic inductance minimization, but rarely at once.

A novel approach to circuit-level modeling is presented in this study to compensate for the parasitic inductance, parasitic capacitance, conduction loss, power dissipation, junction temperature and also helps to operate the MOSFET at high frequencies. The parasitic drain-source capacitance is compensated with a series resonant inductor-capacitor (LC) circuit connected in parallel to the metal oxide semiconductor model (MM9), as shown in Figure 1(a). Additionally, the parasitic capacitance and inductance in the gate/drain-source loops are minimized with parallel connected parasitic compensated MOSFETs, as shown in Figure 1(b). The compensation is validated through simulation reports and mathematical analysis. Paralleling field effect transistor (FETs), M1 and M2 provide the following advantages: i) The current handling capacity increases to meet the electric current requirements of high-power applications; ii) Reduces the conduction losses; iii) Power dissipation over multiple devices is spread to limit the maximum junction temperature; iv) Equalizing the parasitic inductance in the critical gate to the source and drain to the source loop; v) The switching speed increases and helps to achieve high operating frequencies; vi) The transconductance increases because of the same gate to source voltage; vii) The power loss associated with the parallel combination reduces because of the lower ON state resistance; and viii) Improved thermal stability. Ultimately, from an application standpoint, the two parasitic compensation techniques are applied to a two-stage cascade power amplifier and a simple class-E power amplifier to achieve a good improvement in several parameters, including linearity, S-parameters, stability, power dissipation, gain, input/output impedance, and power added efficiency (PAE) and drain efficiency (DE).

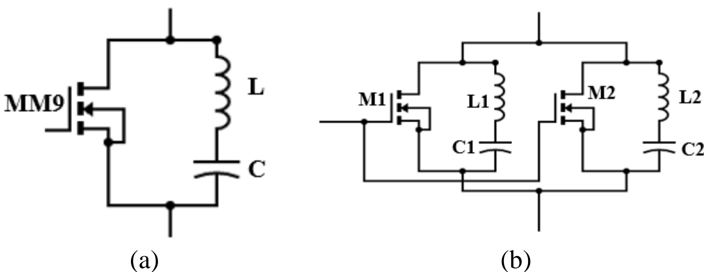

Figure 1. Proposed (a) series resonant LC compensation and (b) parallel MOSFETs LC compensation

2. METHOD

An analytical model for simulating electrical circuits based on physics, the Philips MOS model 9 (MM9) is well-suited for both analog and digital applications. It explains the electrical properties in all pertinent transistor operating regions, including the output conductance, substrate current, and sub-threshold current. In addition to providing superior performance over the more intricate Berkeley Short-channel Insulated gate FET model (BSIM), The first MOS model that is compact and passes the benchmark tests for analog models is MM9. MM9 covers every possible geometry that can be used in an integrated circuit (IC) process [18]. The complete model of MM9 and its related parasitic at radio frequency (RF) is represented by the combination of conventional MOSFET (Mi) and parasitic elements in Figure 2 [19]. Figure 3 display the alternating current (AC) small signal equivalent model of a complete millimeter wave (MMW) MOSFET for high-frequency applications [20].

As shown in Figure 4, the output impedance of the MM9 is regulated by connecting a series resonant LC circuit in parallel to the drain and grounded bulk of the simplified small signal equivalent model of the MM9 [21] in order to compensate for parasitic elements. The main obstacles to working with millimeter wave and radio frequency circuits are parasites. Figure 5 shows the schematic of MM9 (MOSFET1) with proposed parasitic compensation technique i.e., series LC circuit. The following mathematical analysis and simulation reports demonstrate how series LC can be used to compensate for the parasitic effect on high frequency circuit performance.

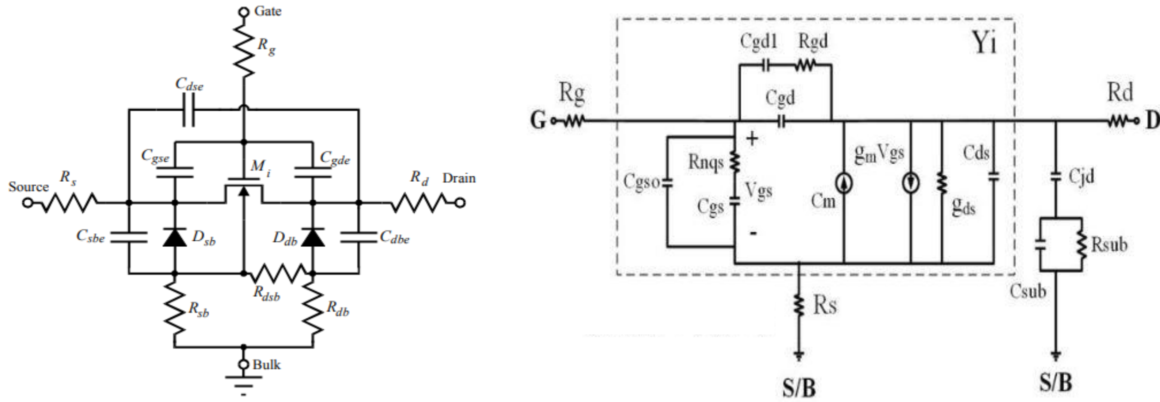

Figure 2. MM9 with parasitic capacitors

Figure 3. MM9 MMW equivalent model

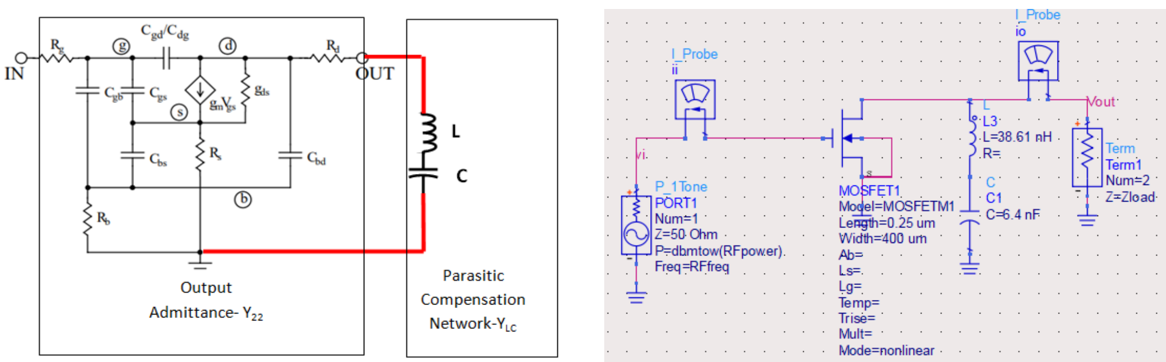

Figure 4. MM9 equivalent model with proposed series resonant LC circuit

Figure 5. Schematic of MM9 MOSFET with proposed series resonant LC circuit

The MM9's output admittance or admittance at MOSFET's drain of the Figure 5 [21] is

$$Y_{22} \approx \frac{1}{\frac{1}{\frac{\omega^2 c_{db}^2}{\frac{1}{R_b}+j\omega\left(c_{gb}+c_{sb}+c_{db}\right)}+g_{ds}+j\omega\left(c_{dg}+c_{db}\right)}+R_s+R_d}$$

According to the aforementioned formula, output admittance increases as source signal frequency (ω) increases. Because of the lowest impedance of drain-bulk (c_{db}) and drain-gate (c_{dg}) parasitic capacitances, it is clear that parasitic capacitances cause MOSFETs to exhibit reduced output impedance at high frequencies (in the GHz region). This causes the gate, drain, and source terminals to short circuit, which ultimately results in a large amount of power dissipation and a reduction in power gain.

The admittance of series resonant LC circuit (Y_{LC}) is

$$Y_{LC} = \frac{1}{j\omega L + \frac{1}{j\omega C}}$$

$$Y_{LC} = \frac{1}{j\omega L - \frac{j}{\omega C}}$$

$$Y_{LC} = -\frac{j}{\omega L - \frac{1}{\omega C}}$$

$$|Y_{LC}| = -\frac{1}{\omega L - \frac{1}{\omega C}}$$

Finally, the magnitude of admittance of Figure 5 can be given as (1).

$$|Y_{PCM}| = |Y_{22}| + |Y_{LC}|$$

$$|Y_{PCM}| = |Y_{22}| - \frac{1}{\omega L - \frac{1}{\omega C}} \quad (1)$$

If $\omega L \gg 1/\omega C$, then from (1),

$$|Y_{PCM}| = |Y_{22}| - (1/\omega L) \quad (2)$$

If $\omega L \ll 1/\omega C$, then from (1),

$$|Y_{PCM}| = |Y_{22}| + \omega C \quad (3)$$

As per the (2) and (3), it can be clearly understood that the output impedance of MM9 MOSFET at higher frequencies can be increased or decreased with the proposed series LC parasitic compensation method by varying the inductor (L) and capacitor (C) magnitudes. If $\omega L \gg \frac{1}{\omega C}$, then the output impedance of series LC compensated MM9 MOSFET at higher frequencies can be increased as per the (2). Hence, the compensation of drain-bulk parasitic capacitance i.e., C_{bd} can be done with a series LC compensated network.

3. RESULTS AND DISCUSSION

The Philips MM9 MOSFET dimension considered here is 0.25×400 µm. The validity of proposed parasitic compensation techniques is verified and simulated with Keysight advanced design system. The output (mag(Zin2)) and input impedance (mag(Zin1)) magnitude of MM9 are 78.27 Ω and 25.19 Ω respectively, as shown in Figure 6(a) at the operating frequency of 3 GHz. According to (2), the output admittance of Figure 5 with L=38.61 nH and C=6.4 nF satisfies the requirement that $\omega L \gg 1/\omega C$, can be given as:

$$Y_{PCM} = (1/78.27) - (1/727.41) = 11.4 \text{ mS}$$

$$\text{mag(Zin2)} = 1/Y_{PCM} = 1/11.4 \text{ mS} = 87.7\ \Omega$$

where, mag(Zin2) is the output impedance magnitude of Figure 5 and its simulated graph is shown in Figure 6(b) along with input impedance magnitude mag(Zin1) of Figure 5. As demonstrated in Figure 1(b) for two parallel parasitic compensated MM9s, Figure 6(c) illustrates the increased output impedance magnitude to 328.84 Ω. Therefore, when compared to series LC MM9s, the two parallel MM9s with series LC compensation offer superior performance and parasitic compensation. In other case, according to (3), the output admittance of Figure 5 with L=1 nH and C=1 nF satisfies the requirement that $\omega L \ll 1/\omega C$, can be given as

$$Y_{PCM} = (1/78.27) + (1/34.23) = 40 \text{ mS}$$

$$\text{mag(Zin2)} = 1/Y_{PCM} = 1/40 \text{ mS} = 23.81\ \Omega$$

The simulated graph of mag(Zin2) i.e., 23.81 is shown in Figure 7(a) at the operating frequency of 3 GHz. With the same L(nH)=C(nF)=1, the output impedance is still reduced to 15.87 ohms in the case of parallel MOSFETs LC compensation, as shown in Figure 7(b) at 3 GHz. It is evident from this mathematical analysis that the two parasitic compensation approaches that are suggested can be used to vary the output impedance of MM9 by selecting different values for the inductor and capacitor. Operating the MM9 even at high frequencies is made possible by this change in output impedance.

According to the aforementioned analysis, the MM9's output impedance can be decreased at low frequencies to provide good current/power amplification or raised at high frequencies to prevent output terminals short circuit. The simulated parameters of MM9, MM9 with series resonant LC compensation, and MM9 with parallel LC compensation at 3 GHz are displayed in Table 1. The following observations have been made based on this table. i) Decrease in input impedance Mag(Zin) contributes to the low power signals' amplification; ii) As output impedance Mag(Zout) rises, power dissipation at high frequencies is lessened; iii) Forward transmission (S21), output reflection coefficient (S22), and input reflection coefficient (S11) all improved, but reverse transmission (S12) barely degraded at all; iv) The stability measurement (B=1+|S11|2-|S22|2-|S11*S22-S12*S21|2) and the Rollette Stability factor (K={1-|S11|2-|S22|2+|S11*S22-S12*S21|2}/{2*|S12*S21|}) remain the same, and the stability criteria (K>1, B>0) is satisfied; and vi) The power output is rising.

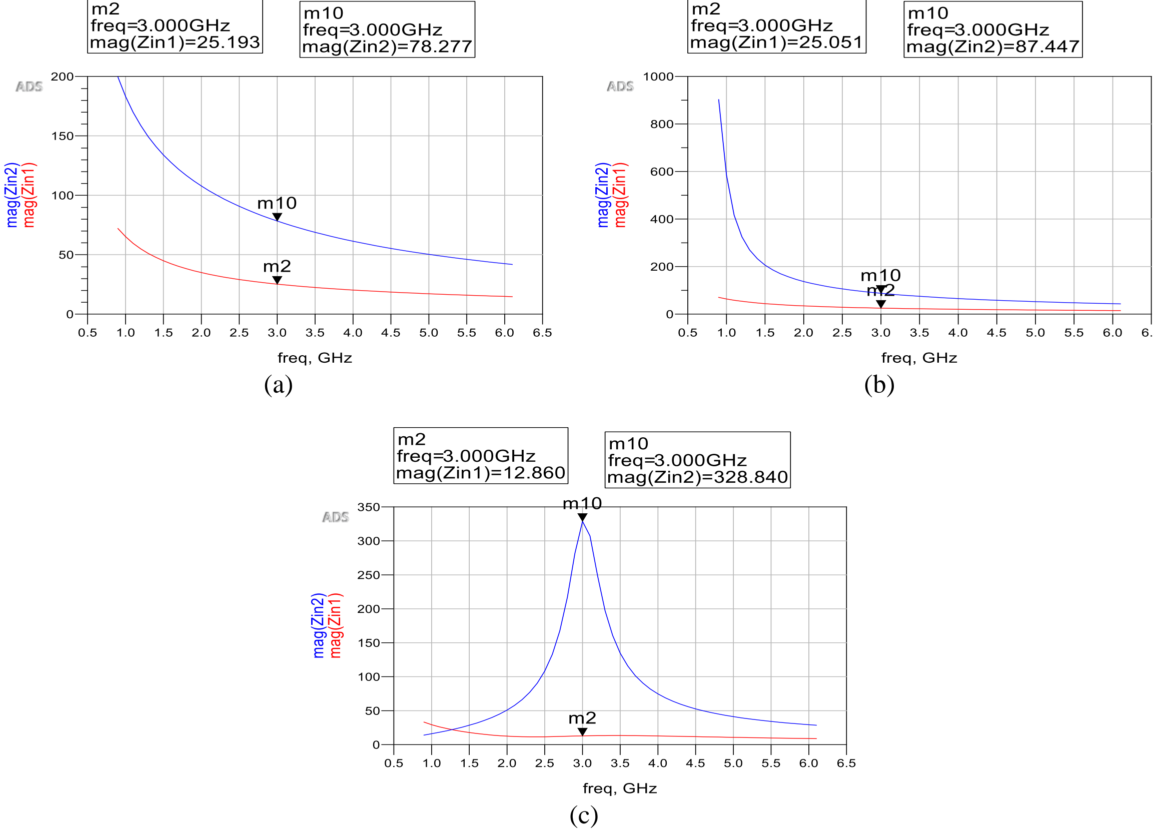

Figure 6. Input (mag(Zin1)) and output impedance (mag(Zin2)) of (a) MM9, (b) series resonant LC compensated MM9, and (c) parallel MM9s LC compensation

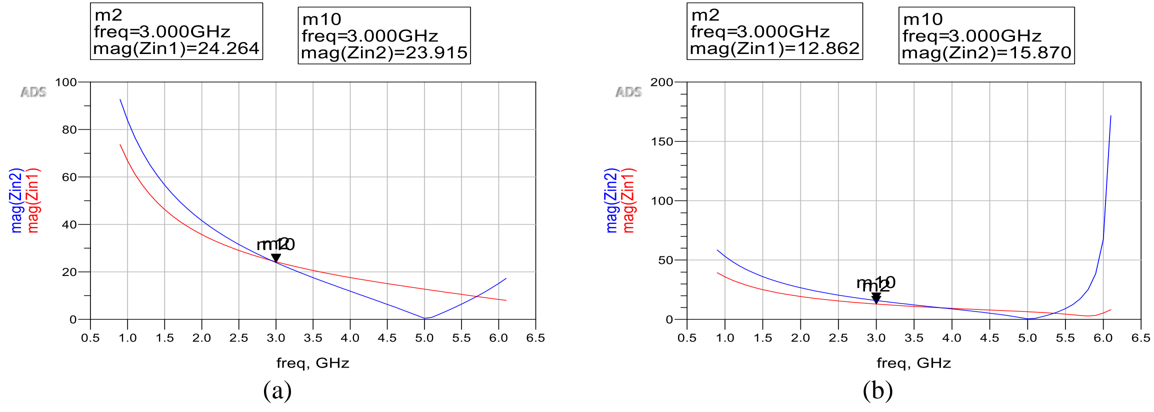

Figure 7. Input (mag(Zin1)) and Output impedance (mag(Zin2)) (a) series resonant LC compensated MM9 and (b) parallel MM9s LC compensation

Table 1. Parameter's comparison

Parameter	MM9	Series resonant LC compensated MM9	Parallel MM9s LC compensation
Mag(Zin)	25.19	25.05	12.86
Mag(Zout)	78.27	87.44	328.84
S11 (dB)	-1.67	-1.78	-2.64
S12 (dB)	-4.90	-4.73	-3.40
S21 (dB)	-4.94	-4.73	-3.40
S22 (dB)	-1.67	-1.78	-2.64
K	1	1	1
B	>0	>0	>0
Pout(dBm)	4.81	5.03	6.29

From an application perspective, the two parasitic compensation methods that have been proposed are employed in the design of a basic class-E power amplifier, as depicted in Figure 8. This allows us to examine the effects of the proposed methods on various performance parameters, including input/output impedances, S parameters, gain, power added efficiency, drain efficiency, direct current (DC) power dissipation, and stability factor. To provide the greatest power to the load, the Parallel MM9s LC compensation technique at 1.7 GHz, is helpful in matching the input impedance and output impedance of the power amplifier as illustrated in Figure 9. It also helps correct the parasitic of the MM9 and to boost up the drain current. Table 2 shows the performance metrics of a basic class-E power amplifier with a 10 dBm source power at 1.7 GHz. The following conclusions have been drawn from this table: i) The output impedance (Zout) can be adjusted with proposed compensation techniques depending on the intended load and amplification; ii) To provide the greatest power to the load, Parallel MM9s LC compensation technique provides the same input and output impedance; iii) Achieved improvements in forward transmission (S21), output reflection coefficient (S22), and input reflection coefficient (S11); iv) The stability measurement (B) is improving beautifully from an unstable to a stable system, while the Rollette stability factor (K) stays the same; and v) When power dissipation (Pdiss) is compromised, output power (Pout), gain, and PAE increase.

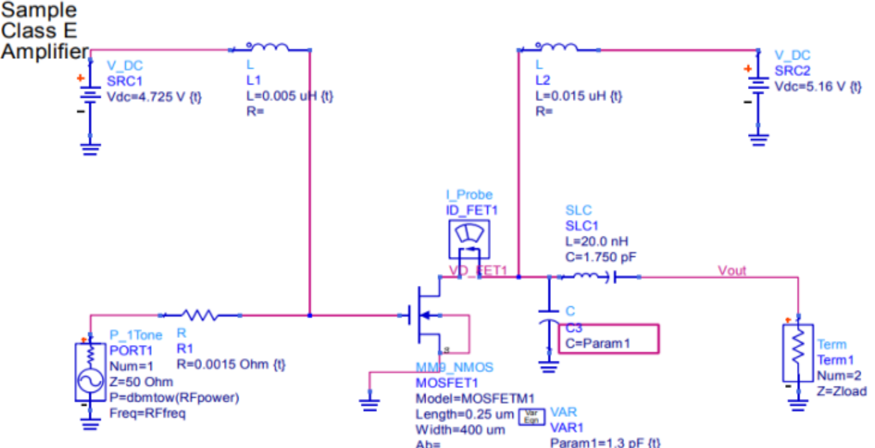

Figure 8. Simple class-E power amplifier

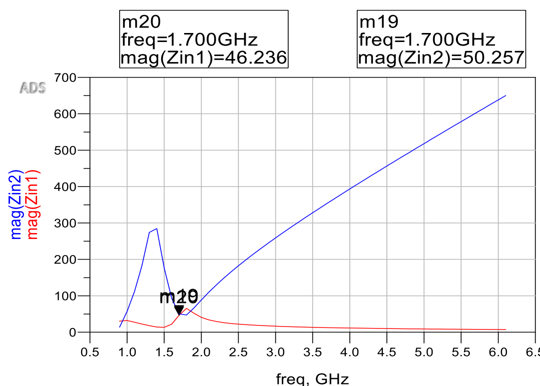

Figure 9. Input (mag(Zin1)) and Output (mag(Zin2)) impedance magnitude of basic class-E power amplifier with Parallel MM9s LC compensation

Table 3 shows the simulated parameters of two stage Cascade power amplifier designed with Parallel MM9s LC compensation technique with 10 dBm source power at operating frequency 1.1 GHz, as shown in Figure 10 and comparison has been done with previous work. The simulated parameters are power gain (Gain_dB) of 16.5 dB, drain efficiency (DE) of 83%, power added efficiency (PAE) of 85.82%, output power (Pout_dBm) of 26 dBm, good stability (StabFact1(K)=2.23, StabMeas1(B)>0) and S-parameters (S11= -9.22 dB, S12= -39.78 dB, S21=16.38 dB, S22=1.41 dB) as shown in Figures 11(a)-11(f) respectively.

The output spectrum of the two-stage cascade proposed power amplifier is shown in Figure 12, where the maximum output power can be observed at 1.1 GHz with harmonic suppression at other frequencies. Figure 13 shows the variation of output power and PAE with respect to the load resistor. Here the output power remained constant till 100 Ω load and peak PAE obtained at 55 Ω.

Table 2. Performance metrics of basic class-E power amplifier with proposed parasitic compensation techniques

Parameter	MM9	Series resonant LC compensated MM9	Parallel MM9s LC compensation
Zin (dB)	29.99	33.28	33.47
Zout (dB)	39.39	34.80	33.56
S11 (dB)	-8.66	-24.71	-28.33
S12 (dB)	-5.99	-0.99	-1.04
S21 (dB)	-4.06	0.94	0.98
S22 (dB)	-1.63	-24.62	-29.95
K	1	1	1
B	<0	>0	0.08
Pout (dBm)	10.25	10.62	11
PAE (%)	3.93	5.69	8.05
DE (%)	40.06	42.91	40.07
Pdc (mW)	26	27	31
Pdiss (mW)	24	24	28
Gain (dB)	0.24	0.68	0.98

Table 3. CMOS process performance comparison

	CMOS process (nm)	Frequency (GHz)	Pout (dBm)	PAE (%)
[22]	180	2.4	26	24
[23]	130	1.7-2.7	25	38
[24]	90	2.4	9	30
[25]	130	1.1-2.9	27.6	49.4
[26]	180	2.4	7.6	36
[27]	130	2.5	19	32
[28]	65	1.8	14.12	38.4
[29]	180	2.45	20	43.6
[30]	180	2.1-4.8	22	43.7
[31]	40	<1	20	43
[32]	22	2.4	30.7	42.5
[33]	65	1	21.5	52.4
This Work	**180**	**1.1**	**26**	**85.8**

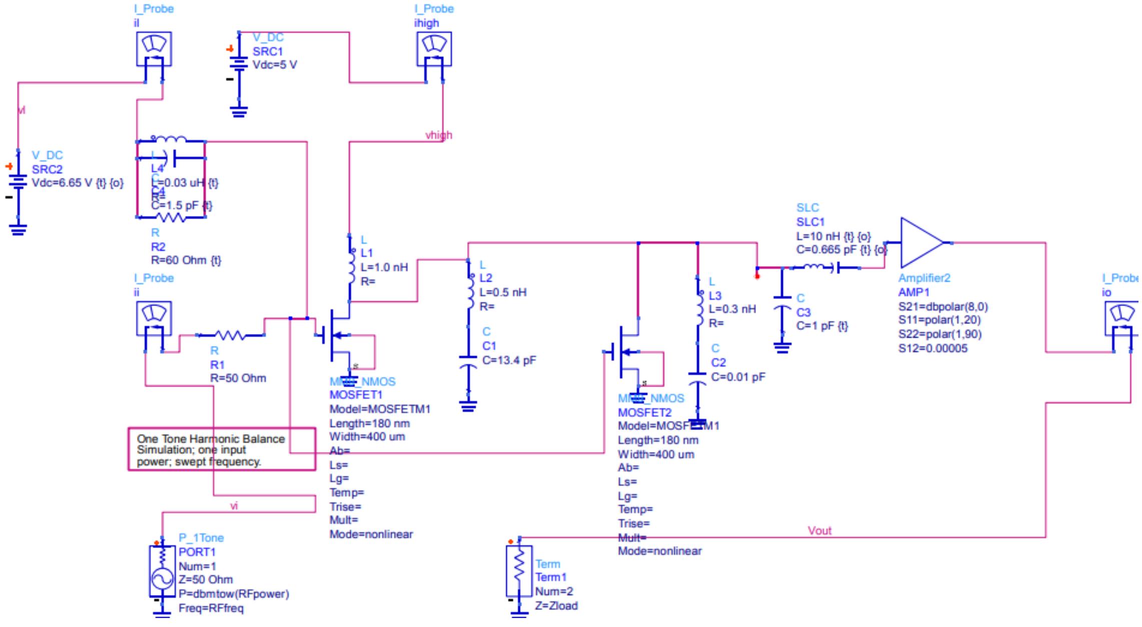

Figure 10. Two stage Cascade power amplifier at 1.1 GHz with Parallel MM9s LC compensation

(a) (b)

(c) (d)

(e) (f)

Figure 11. Parasitic compensated two stage cascade power amplifier at 1.1 GHz with (a) Gain, (b) DE, (c) PAE, (d) Output power, (e) Stability factor (K) and Stability measurement (B), and (f) S parameters

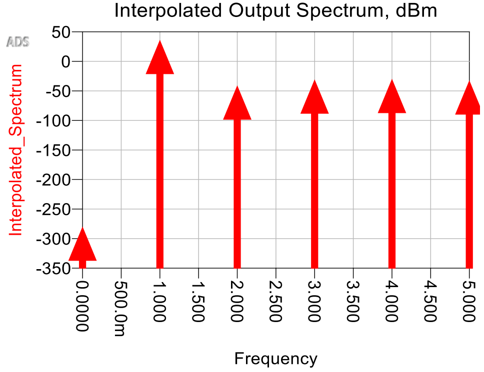

Figure 12. Interpolated output spectrum

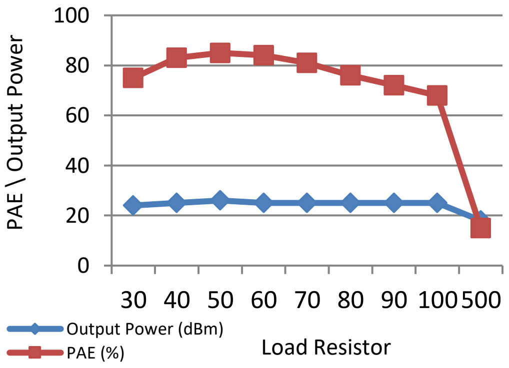

Figure 13. Variation of output power and PAE with respect to load resistor

4. CONCLUSION

This paper presents the simulation reports and mathematical analysis of proposed two circuit level parasitic compensation techniques to the Philips MM9 MOSFET at high frequencies (GHz). The suggested methods are based on series resonant LC circuit and paralleling the two parasitic compensated MOSFETs. These innovative techniques successfully reduce the influence of MOSFET parasitic elements at high frequencies, as evidenced by the 2-stage cascaded basic class-E power amplifier that has the maximum power added efficiency of 85.82%, high drain efficiency of 88.03%, power gain of 16.5 dB, good stability (K=2.23, B>0), reflection coefficient of -39.78 dB, transmission coefficient of 16.38 dB and an output power of 26 dBm at the operating frequency of 1.1 GHz with 10 dBm source power. Further improvement in performance metrics can be seen at higher operating frequencies by using the Doherty concept and Wilkinson power combining technique to the suggested power amplifier design.

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REFERENCES

[1] Q. Li and Y. P. Zhang, "CMOS T/R switch design: towards ultra-wideband and higher frequency," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 3, pp. 563–570, Mar. 2007, doi: 10.1109/JSSC.2006.891442.

[2] A. Singh, O. Maheshwari, and N. R. Mohapatra, "Parasitic capacitance in nanosheet FETs: extraction of different components and their analytical modeling," *IEEE Transactions on Electron Devices*, vol. 71, no. 5, pp. 2894–2900, May 2024, doi: 10.1109/TED.2024.3382216.

[3] S. Sharma, S. Sahay, and R. Dey, "Parasitic gate capacitance model for N-stack forksheet FETs," *IEEE Transactions on Electron Devices*, vol. 71, no. 3, pp. 1728–1736, Mar. 2024, doi: 10.1109/TED.2023.3335031.

[4] D. Navarro, C. Tanaka, K. Adachi, T. Naito, K. Tada, and A. Hokazono, "Technology-dependent modeling of MOSFET parasitic capacitances for circuit simulation," in *2023 35th International Conference on Microelectronic Test Structure (ICMTS)*, Mar. 2023, pp. 1–4, doi: 10.1109/ICMTS55420.2023.10094071.

[5] W. Chakraborty *et al.*, "Characterization and modeling of 22 nm FDSOI cryogenic RF CMOS," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 7, no. 2, pp. 184–192, Dec. 2021, doi: 10.1109/JXCDC.2021.3131144.

[6] S. H.-M. Jen, C. C. Enz, D. R. Pehlke, M. Schroter, and B. J. Sheu, "Accurate modeling and parameter extraction for MOS transistors valid up to 10 GHz," *IEEE Transactions on Electron Devices*, vol. 46, no. 11, pp. 2217–2227, 1999, doi: 10.1109/16.796299.

[7] D. N. Dalal *et al.*, "Impact of power module parasitic capacitances on medium-voltage SiC MOSFETs switching transients," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 298–310, Mar. 2020, doi: 10.1109/JESTPE.2019.2939644.

[8] X. Zhang, H. Fu, K. Ma, N. Yan, Y. Liu, and Y. Mu, "Investigation of channel parasitic effect of CMOS transistor for high responsivity 2.58 THz detector array with patch antennas in chip," *IEEE Transactions on Terahertz Science and Technology*, vol. 13, no. 5, pp. 464–475, Sep. 2023, doi: 10.1109/TTHZ.2023.3286654.

[9] P. Cadareanu, J. Romero-Gonzalez, and P.-E. Gaillardon, "Parasitic capacitance analysis of three-independent-gate field-effect transistors," *IEEE Journal of the Electron Devices Society*, vol. 9, pp. 400–408, 2021, doi: 10.1109/JEDS.2021.3070475.

[10] S. Sharma, S. Sahay, and R. Dey, "Parasitic capacitance model for stacked gate-all-around nanosheet FETs," *IEEE Transactions on Electron Devices*, vol. 71, no. 1, pp. 37–45, Jan. 2024, doi: 10.1109/TED.2023.3281530.

[11] P.-H. Lee *et al.*, "A tall gate stem GaN HEMT with improved power density and efficiency at Ka-Band," *IEEE Journal of the Electron Devices Society*, vol. 11, pp. 36–42, 2023, doi: 10.1109/JEDS.2023.3236304.

[12] E. Gili *et al.*, "Single, double and surround gate vertical MOSFETs with reduced parasitic capacitance," *Solid-State Electronics*, vol. 48, no. 4, pp. 511–519, Apr. 2004, doi: 10.1016/j.sse.2003.09.019.

[13] V. D. Kunz *et al.*, "Reduction of parasitic capacitance in vertical MOSFETs by spacer local oxidation," *IEEE Transactions on Electron Devices*, vol. 50, no. 6, pp. 1487–1493, Jun. 2003, doi: 10.1109/TED.2003.813334.

[14] J. Guo *et al.*, "A new 4H-SiC trench MOSFET with improved reverse conduction, breakdown, and switching characteristics," *IEEE Transactions on Electron Devices*, vol. 70, no. 1, pp. 172–177, Jan. 2023, doi: 10.1109/TED.2022.3225121.

[15] Y. Li, M. Liang, J. Chen, T. Q. Zheng, and H. Guo, "A low gate turn-off impedance driver for suppressing crosstalk of SiC MOSFET based on different discrete packages," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 1, pp. 353–365, Mar. 2019, doi: 10.1109/JESTPE.2018.2877968.

[16] D. Wei *et al.*, "A 140 GHz, 4 dB noise-figure low-noise amplifier design with the compensation of parasitic capacitance CGS," in *2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2019, pp. 299–302, doi: 10.1109/MWSCAS.2019.8884937.

[17] J. Zhang, D. Wang, W. Zhu, M. Zhai, X. Yi, and Y. Wang, "A Ka-Band mutual coupling resilient stacked-FET power amplifier with 21.2 dBm OP1dB and 27.6% PAE1dB in 45-nm CMOS SOI," *IEEE Solid-State Circuits Letters*, vol. 7, pp. 147–150, 2024, doi: 10.1109/LSSC.2024.3386676.

[18] R. M. D. A. Velghe, D. B. M. Klaassen, and F. M. Klaassen, "Compact MOS modeling for analog circuit simulation," in *Proceedings of IEEE International Electron Devices Meeting*, pp. 485–488, doi: 10.1109/IEDM.1993.347305.

[19] C. R. Iversen, "A MOS model 9 extension for GHz CMOS RF circuit design," in *2001 31st European Microwave Conference*, Sep. 2001, pp. 1–4, doi: 10.1109/EUMA.2001.339129.

[20] Y. Cao, W. Zhang, J. Fu, Q. Wang, L. Liu, and A. Guo, "A complete small-signal MOSFET model and parameter extraction technique for millimeter wave applications," *IEEE Journal of the Electron Devices Society*, vol. 7, pp. 398–403, 2019, doi: 10.1109/JEDS.2019.2900202.

[21] J. Saijets, M. Andersson, and M. Åberg, "A comparative study of various MOSFET models at radio frequencies," *Analog Integrated Circuits and Signal Processing*, vol. 33, pp. 5–17, 2022.

[22] J. Ho and H.-W. Tsao, “CMOS power amplifier with novel transformer power combiner,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 7, pp. 2365–2369, Jul. 2023, doi: 10.1109/TCSII.2023.3238509.

[23] S. Mariappan, J. Rajendran, Y. Chen, P.-I. Mak, and R. P. Martins, “A 1.7-to-2.7GHz 35–38% PAE multiband CMOS power amplifier employing a digitally-assisted analog pre-distorter (DAAPD) reconfigurable linearization technique,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 11, pp. 3381–3385, Nov. 2021, doi: 10.1109/TCSII.2021.3080831.

[24] V. Chironi, B. Debaillie, S. D’Amico, A. Baschirotto, J. Craninckx, and M. Ingels, “A digitally modulated class-E polar amplifier in 90 nm CMOS,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 4, pp. 918–925, Apr. 2013, doi: 10.1109/TCSI.2012.2215398.

[25] T. Shen, Y. Zhang, X. Tang, J. Li, F. Huang, and N. Jiang, “A 1.1 ~ 2.9 GHz high efficiency CMOS power amplifier,” in *2020 IEEE 5th International Conference on Integrated Circuits and Microsystems (ICICM)*, Oct. 2020, pp. 109–112, doi: 10.1109/ICICM50929.2020.9292176.

[26] M. M. El-Desouki, M. J. Deen, Y. M. Haddara, and O. Marinov, “A fully integrated CMOS power amplifier using superharmonic injection-locking for short-range applications,” *IEEE Sensors Journal*, vol. 11, no. 9, pp. 2149–2158, Sep. 2011, doi: 10.1109/JSEN.2011.2109708.

[27] H. Madureira *et al.*, “Design and measurement of a 2.5 GHz switched-mode CMOS power amplifier with reliability enhancement,” in *2016 IEEE MTT-S International Wireless Symposium (IWS)*, Mar. 2016, pp. 1–4, doi: 10.1109/IEEE-IWS.2016.7585406.

[28] J.-C. Du, Z.-G. Wang, J. Xu, and Y.-F. Yang, “A current-injection class-E power amplifier,” *IEEE Microwave and Wireless Components Letters*, vol. 30, no. 8, pp. 775–778, Aug. 2020, doi: 10.1109/LMWC.2020.3000994.

[29] Z. Li *et al.*, “A 2.45-GHz + 20-dBm fast switching class-E power amplifier with 43% PAE and a 18-dB-Wide power range in 0.18- µm CMOS,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 4, pp. 224–228, Apr. 2012, doi: 10.1109/TCSII.2012.2186363.

[30] Y. Dong, L. Mao, and S. Xie, “Fully integrated class-J power amplifier in standard CMOS technology,” *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 1, pp. 64–66, Jan. 2017, doi: 10.1109/LMWC.2016.2630920.

[31] M. Mizokami, T. Uozumi, Y. Yamashita, K. Shibata, and H. Sato, “A 43%-efficiency 20dBm sub-GHz transmitter employing rise-edge-synchronized harmonic calibration with 33.3% duty cycle,” in *2017 Symposium on VLSI Circuits*, Jun. 2017, pp. C304–C305, doi: 10.23919/VLSIC.2017.8008518.

[32] J. Du, Z. Li, and Z. Li, “A 2.4 GHz doherty power amplifier based on voltage combining in 22 nm CMOS,” in *2023 12th International Conference on Modern Circuits and Systems Technologies (MOCAST)*, Jun. 2023, pp. 1–4, doi: 10.1109/MOCAST57943.2023.10176649.

[33] N. Ginzberg and E. Cohen, “A wideband CMOS power amplifier with 52% Peak PAE employing resistive shunt feedback for sub-6 GHz 5G applications,” *IEEE Microwave and Wireless Technology Letters*, vol. 33, no. 2, pp. 192–195, Feb. 2023, doi: 10.1109/LMWC.2022.3209822.

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