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Low-power body-coupled transceiver for miniaturized body area networks

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ABSTRACT

As wearable devices continue to proliferate, seamlessly integrating them into wireless body-area networks (WBANs) becomes increasingly crucial. Body-coupled communication (BCC) emerges as a promising WBAN technology, utilizing the human body itself as a transmission channel. This paper presents a novel BCC transceiver designed for efficiency and miniaturization. The proposed transceiver prioritizes reliable data transmission with a convolutional encoder. It leverages a simple direct digital synthesizer (DDS) for frequency shift keying (FSK) modulation, minimizing chip area. At the receiver, a Viterbi decoder (VD) ensures accurate data recovery. This design shines in its resource efficiency. It occupies less than 1% of an Artix-7 FPGA, operates at 268.77 MHz with a mere 111 mW power consumption, and achieves a remarkable data rate of 13.78 Mbps. This translates to a hardware efficiency of 44.46 Kbps/slice, surpassing existing transceivers. Moreover, the BCC transceiver exhibits a stellar bit error rate (BER) of over 10^{-7} under realistic body channel conditions. Overall, this work presents a highly efficient BCC transceiver with significant improvements in chip area, power consumption, and data rate compared to existing designs. This paves the way for practical and miniaturized WBAN solutions for future wearable applications.

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1. INTRODUCTION

A body-area network (BAN) is relatively new in linking portable electronic and network gadgets close to a person's body. The several nodes located on and close to the human body in a BAN may interact wirelessly with one another. Various radio frequency (RF) wireless approaches have been established to support these connections, also known as personal area networks. Consumer electronic interconnection is one area where these BANs could be helpful [1]. Developing a dependable, quick, and accurate interface to enable active welfare management and achieve early identification, avoidance of illness, and even therapies is one of the main aims of implantable medical devices (IMDs). Body-coupled communication (BCC), or intra-body communication (IBC), is a possible innovation that envisions a network of sensors and actuators inside a human body. It takes advantage of the body's conducting qualities and comes under the general

heading of the IEEE 802.15.06 protocol. IBC connections are often created via the human body, although signaling pathways can change according to how the electrodes are set up and the various signal connection techniques [2], [3].

Wireless BANs (WBANs) are mainly used in medical and well-being gadgets, which must be connected to share information like health data. Several of these gadgets use short-range transmission technologies. Examples of short-range communications are ZigBee and Bluetooth devices, which both work at 2.4 GHz. One of the ways for WBAN data transmission, known as human body communication (HBC), also known as IBC or BCC, has drawn much attention. It uses a portion of an individual's body as a transmission medium [4]. For communication between implants or between implants and relays, the most popular type of BCC link uses traditional RF signals in the narrowband (NB) or ultra-wideband (UWB) range. But there are also unusual wireless communication methods with unique qualities that might be better suited for IBC. Humans communicate on the transmitter and receiver sides using galvanic, capacitive, and resonant coupling techniques. People send signals into tissue from other people using galvanic coupling (GC), which uses a weak current of about 0.5 mA. These signals can be used to connect devices. By allowing nearby electric fields to go within and around the tissues of humans, capacitive coupling (CC) makes linkages that extend across the entire medium possible. Like inductive coupling approaches, magnetic resonance coupling (RC) uses weakly linked coils placed over body parts to send and receive magnetic energy [5], [6].

The WBAN applications address various topics to enhance the user's quality of life. Applications like these are divided into two categories based on their intended use: medical or non-medical. Applications for immersive gaming and wellness tracking, intellectual and emotional assessment for helping with driving or social relationships, and medical assistance during disasters, including terrorist attacks, quakes, and wildfires, are examples of non-medical applications. Healthcare applications mainly consist of healthcare options for sick and older people. Early identification, avoidance, and tracking of illnesses are common, as are home care for older people, recovery following operations, neurofeedback programs that regulate feelings, and residential care programs that enhance the standard of living for those with impairments [7]. With the help of these recently developed wearable sensors, individuals can track their long-term wellness in open spaces without limiting their regular activities. The sensors enable activities such as supported living for those with persistent medical conditions in this manner. The delivery of medical care can now be more individualized, scientific and data-based, economical, user-friendly, and staff-friendly. The heartbeat and frequency response of the human body are realized using BCC for WBAN applications [8], [9].

The BAN with a RF based wireless system provides reasonable data rates but lags with security, electromagnetic issues, low battery life, and power consumption problems. The alternate non-RF wireless technology is IBC or BCC, which connects the human body as a channel or medium for electrical signal transmission and resolves most RF-based wireless system problems. The BCC is another option for short-range transmission by offering a better data rate and less power utilization in the human body.

An efficient BCC transceiver architecture and its performance metrics are discussed in this manuscript. The contribution of the proposed work is as follows: The proposed work uses a simple encoding and decoding mechanism using convolutional codes to reduce the bit error rate (BER). The frequency shift keying (FSK) approach with a direct digital synthesizer (DDS) is used for modulation and demodulation to improve the data rate of the BCC transceiver. Most existing approaches use voltage controller oscillators (VCOs) or local oscillators (LOs) to generate the sine wave, which utilizes more chip area and degrades the system's overall performance. So, DDS is used with the FSK approach to generate the sine waveform and improve the chip area.

The manuscript's organization is as follows: The background of the proposed work is discussed concerning recent works in section 1. The related works is discussed in section 2. The BCC transceiver architecture is explained in detail in section 3. The results of the BCC transceiver and its sub-modules are discussed in detail in section 4. Section 5 concludes the overall work with improvements and suggests a futuristic scope.

2. RELATED WORKS

This section discusses recent works on BCC, or IBC, systems and their approaches and performance metrics. Seyedi and Lai [10] present the IBC system design for WBAN applications using a digital baseband approach. The high-frequency pulse wave is transmitted via humans at different frequency rates. The work analyses the signal attenuation of the human arm at specific frequencies. Using a galvanic coupling approach, the IBC works at a data rate of 1.56 Mbps by consuming 3.94 mW of power and a bit error rate (BER) of 10-7. Vijayalakshmi and Nagarajan [11] describe the body-channel communication-based transceiver as designed with low-power and high-efficiency features. The hamming encoding digital transmitter (HEDT) with the FSK approach is used in this work to improve the data rate and power. The transceiver works at a

data rate of 60 Mbps by consuming 2.65 mW of power on 65 nm complementary metal oxide semiconductor (CMOS) technology. However, the transceiver utilizes more chip area using the FSK approach. Chen *et al.* [12] present the GC based IBC transceiver using direct sequence spread spectrum (DSSS) and differential phase shift keying (DPSK) approaches. The DSSS-DPSK improves symbol recovery and BER. The IBC transceiver achieves a data rate of 50 Kbps with a BER of 10-5 for the 2 MHz carrier frequency and 0.392 mA of coupling amplitude. The GC-based IBC transceiver operates at a lower data rate, and the complexity is higher at the receiver side due to the symbol recovery operation.

Vizziello *et al.* [13] describe the physical layer (PHY) design of the GC-Testbed for IBC links. The work offers higher flexibility, physiological data transmission, and error-free communication in the PHY layer. The Wiener filter compensates for the frequency offset during binary phase-shift keying (BPSK) modulation. The signal-to-noise ratio (SNR) of 20 dB is obtained with a 4 cm distance between the transmitter and receiver. However, the energy consumption is higher during data transmission between IBC links. Wei *et al.* [14] describe the GC-IBC transceiver using a differential phase shift keying (DPSK) approach. The DPSK modulation with coherent demodulation approaches is used in the IBC design to improve the data rate and BER. The IBC design achieves a data rate of 1 Mbps with a BER of 10-5 using a carrier frequency of 2 MHz and a coupling amplitude of 0.6 mA. However, the GC-IBC transceiver using DPSK operates at a lower data rate due to filtering. Nath *et al.* [15] present the electro-quasistatic-based human-body communication (EQ-HBC) system. EQ-HBC uses inter-body communication with a capacitive coupling approach to strengthen the SNR. The BER of 10-4 is achieved using quadrature PSK and quadrature amplitude modulation (QAM) at 7.1 and 13.2 SNR, respectively. Pitou *et al.* [16] describe the GC-IBC transceiver with the fully miniaturized feature. The DDS is used for analogue sine wave generation on both the transmitter and receiver sides. The work analyses the receiver gain and output signal concerning the different frequencies. However, the system model supports a data rate of up to 800 Kbps. Vizziello *et al.* [17] present HBC-based channel characterization using measured impulse response (IR). For implanted GC, the cross-correlation amplitude and frequency parameters are used to look at the channel impulse response (CIR) and channel frequency response (CFR).

Kim *et al.* [18] talk about a small, dual-band, near-field antenna that is placed on the body and has a reflector for using electromagnetic radiometers to get a full picture of the internal temperature. It successfully obtained the spectrum and volume loss level appropriate for measuring the deep core temperature of electromagnetic radiometers. Rangeaiah *et al.* [19] describe fat-intrabody communication (FIBC) as studying a wireless interface system centered on the human body. The BER tests show that the Fat-IBC link is straight and can handle modulations as complicated as 512-QAM without any noticeable BER loss. The only thing that was not used was two on-body antennas with extended phantoms. Musa *et al.* [20] present the creation and evaluation of a small, dual-band handheld antenna for WBAN applications. An inverted U-shaped notch is added to the alteration to increase its resonance frequency to 2.4 GHz. The proposed antenna's on-body tests and twisting conditions demonstrate that its effectiveness remains unaltered. As a result, it is shown that the antenna may be used in WBAN situations. Demrozi *et al.* [21] describe building a low-cost WBAN. It is predicated on readily available gadgets and an Android application. After that, they offer an analytical evaluation that considers resource utilization. Finally, it provides accuracy and adaptability in clinical and medical operations scenarios. Focusing on energy efficiency in IoT, a study published in [22] investigates energy-aware protocols for both MAC and routing mechanisms. This research introduces a classification system for routing protocols, followed by an in-depth analysis of their strengths and weaknesses. Chen *et al.* [23] examine human body shadow properties in the sub-6 GHz frequency range, used in most widely used wireless systems. Even though the frequencies fluctuated, the attenuating assessment for the human body shifted when the RXs and the body's position towards others changed.

3. BCC TRANSCEIVER ARCHITECTURE

The BCC transceiver (TR) is designed using convolution codes and the FSK modulation approach. The hardware architecture of the BCC transceiver is illustrated in Figure 1. The BCC TR has a BCC transmitter (TX), a channel like the human body, and a BCC receiver (RX). The BCC-TR has 1-bit data input and 1-bit data output. A preamble and start of the frame (SOF) generator, a convolutional encoder (CE), a parallel to serial (P2S) converter, FSK modulation with DDS for data generation, and a multiplexor (MUX) are all part of the BCC-TX. The BCC-RX contains a demultiplexer (DEMUX), FSK demultiplexer, serial-to-parallel (S2P) converter, Viterbi demultiplexer, and header recovery unit. The 32-bit Preamble and 8-bit SOF generate the 40-bit header for BCC. The data generation unit provides 12-bit FSK modulation. So, BCC transmits 52 bits in a sequence to the human body. The BCC frame format is shown in Figure 2.

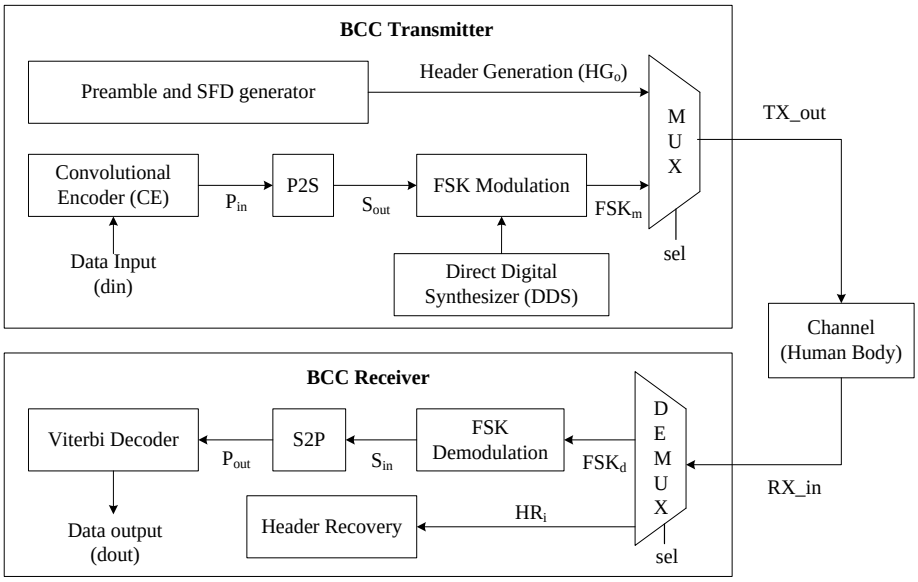

Figure 1. Hardware architecture of BCC transceiver

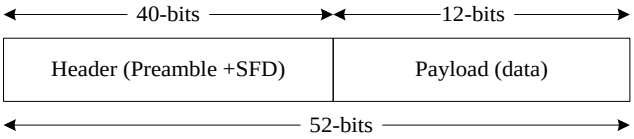

Figure 2. BCC frame format

3.1. BCC Transmitter

The BCC-TX sends the 1-bit data input in a sequence to the CE unit, which encodes and provides a 3-bit encoded output. The P2S converter receives the 3-bit encoded data in parallel to generate the 1-bit serial data. The FSK modulation with DDS provides two different frequency outputs, either 500 KHz or 1 MHz, based on the 1-bit serial data. The MUX unit receives header data; modulated data provides the transmitted output based on a selected line. The 32-bit preamble (PG) and 8-bit SOF (SG) values are predefined and stored in the read-only memory (ROM) unit. The 32-bit Preamble and 8-bit SOF are predefined values and are 'C55555CC' and 'A5', respectively. The BCC-TX sub-module's architecture is shown in Figure 3. The CE architecture and FSK modulation operation are illustrated in Figures 3(a) and 3(b), respectively. The BCC-TX sub-modules are explained as:

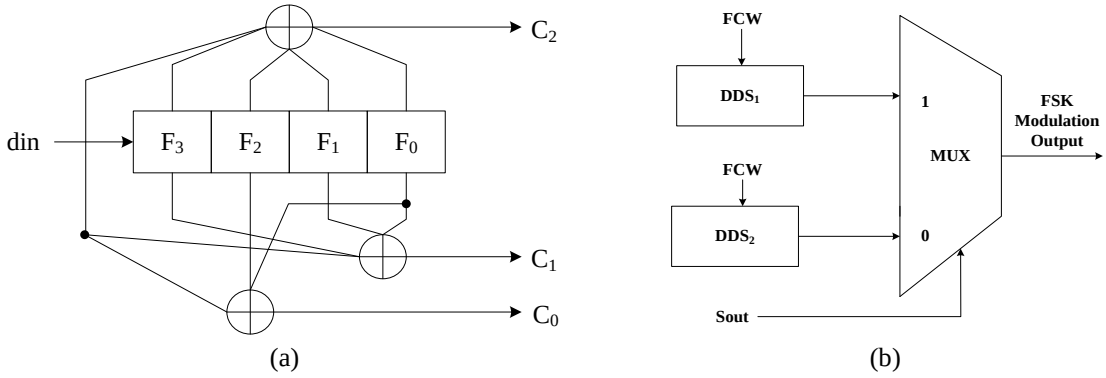

Figure 3. BCC-TX sub-module architectures, including (a) convolutional encoder and (b) FSK modulation

The CE unit uses the state machine method with a memory unit and combinational circuit. The state machine has 1-bit shift registers (F) and n modulo-2 adders. The state machine contains the adders, which decide the length of the codewords. The CE is framed using three parameters ($n, m,$ and K). Where $'n'$ is the length of the codewords, $'m'$ is the number of data bits, and $'K'$ is the constraint length of the CE. In this work, the CE is designed based on the format of (3, 1, 4). where the number of input bits $(m) = 1$, the codeword length $(n) = 3$, and the constraint length $(K) = 4$. The code rate (m/n) of the convolutional encoder is 1/3. It contains 1-bit input (inp), four shift registers (F), and three modulo-2 adders (XOR) that produce three-bit output code words ($n = 3$). The four shift registers are connected to the three modulo adders based on the definition of the three generator polynomials $G_0, G_1,$ and G_2. The generator polynomials $G_0, G_1,$ and G are defined as: $G_0 = [0101], G_1 = [1011]$, and $G_2 = [1111]$. The length of the codewords or the output of the CE is calculated using (1).

$$C_0 = din \oplus F_2 \oplus F_0$$

$$C_1 = din \oplus F_3 \oplus F_1 \oplus F_0$$

$$C_2 = din \oplus F_3 \oplus F_2 \oplus F_1 \oplus F_0 \quad (1)$$

The P2S converter is modelled using the parallel in serial out (PISO) register, and it mainly contains 3-bit parallel inputs, 3-data flip-flops (D-FF), and 1-bit serial output (S_{out}). The 2-bit counter is used to count the P2S conversion operation. The FSK modulation (FSKm) is designed using two DDS and control logic units. The data input is 1-bit, providing the logic '1' or logic '0'. The control logic unit acts as MUX functionality. The two DDS modules provide the waveforms (sinusoidal) and inputs to the MUX. The first DDS frequency control word (FCW) is set to 10,485 for generating a 1 MHz waveform output. Similarly, the second DDS FCW is set to 5,243 for generating 500 KHz waveform output. The received serial data input (S_{out}) acts as the select line for the MUX and provides '0' or '1' logic. If the data input is 1, the MUX selects the first DDS output as an FSK-modulated output. Similarly, if the data input is 0, the MUX selects the second DDS output as modulated output (FSK_m). The BCC TX output (TX_{out}) considers either header or data (payload) output as the final TX output. The Algorithm 1 of the BCC-TX is represented as Algorithm 1.

Algorithm 1. BCC transmitter

```
Input: data input (din), select line (sel);
Output: Transmitter output (TX_out)
    1.  Header Generation:
            a.  Preamble generation:
                  • Predefine 32-bit preamble data (PG) and set it to: "C55555CC";
            b.  SFD Generation:
                  • Predefine 8-bit SOF data (SG) and set it to: "A5";
            c.  Concatenate Preamble and SOF data:
                  • Header Generation: HGo={SG, PG};
    2.  Data or Payload Formation:
            a.  Convolutional Encoder:
                  • Pin ={0, C3, C2, C1}= CE (din);
            b.  P2S Converter:
                  • Sout=P2S(Pin);
            c.  FSK Modulation:
                  • If (Sout=1)
                       FSKm=DDS1 Output; // at 1 MHz
                    else
                       FSKm=DDS2 Output; // at 500 KHz
                    end if
            d.  TX Output generation:
                  • If (sel=1)
                       TX_out=FSKm; // data information
                    else
                      TX_out=HGo; // header information
                    end if
```

The DDS is used to produce the sinusoidal wave for the given FCW. The DDS contains a phase accumulator (PA), complementor, MUX tree, adder, and format converter. The DDS architecture is illustrated in Figure 4. Three components comprise the PA: a phase register, an adder, and a frequency register.

Figure 4. DDS architecture

A phase-to-amplitude converter converts every value at the PA's output to an approximation of sine amplitude. The output of the PA is a ramp-based signal. For angles in quadrants 2 and 4, the complementor is used to invert the last few bits of the phase accumulator. As a result, a triangle wave with the same frequency and double the amplitude is created from the ramp output of the PA. The smoothed half-sine wave is generated by the MUX tree employing shifting and ROM operations on linear segments. The format converter generates the final sine waveform based on the output of the MSB bit and adder from the PA. The DDS output signal's frequency (F_{out}) is represented using (2):

$$F_{out} = F_{clk} * \left(\frac{FCW}{2^A}\right) \quad (2)$$

where F_{clk} denotes system clock frequency, the length of the PA is denoted by 'A'. The channel contains an additive Gaussian white noise (AWGN) generator and scaling factor. The AWGN generator generates random data based on the linear feedback shift register (LFSR), and the scaling factor is fixed to 4. The 8-bit noise data is generated by dividing the AWGN generator data by the scaling factor. The channel receives the BCC-TX output (TX_{out}) and corrupts it by performing the OR operation with noise data.

3.2. BCC receiver

The BCC receiver (RX_{in}) receives the corrupted data from the channel or human body to perform the demodulation, followed by a decoding operation to return the original data and header recovery. The DEMUX receives the corrupted data; the data and header values are separated based on the select line. The FSK demodulator (FSK_d) receives and matches the data values with DDS values. If it matches, then FSK demodulated output (S_{in}) is one else zero. The serial-to-parallel (S2P) converter converts the 1-bit serial to 3-bit parallel data (P_{out}) in a serial-in-parallel-out (SIPO) manner. The Viterbi decoder (VD) decodes and generates the final corrected output (d_{out}). Algorithm 2 of the BCC-RX is represented as Algorithm 1:

Algorithm 2. BCC receiver

```
Input: Receiver input (RX_in), select line (sel);
Output: Receiver output (dout)
    a. Decompose using DEMUX:
        • If (sel=1)
            FSKd=RX_in;
              else
            HRi=RX_in;
             end if
    b. FSK Demodulation:
        • If (FSKd=DDS1)
            Sin=1;
              else if (FSKd=DDS2)
            Sin=0;
               end if
    c. S2P Converter:
        • Pout=S2P(Sin);
    d. Viterbi Decoder:
        • dout=VD(Pout);
```

Figure 5 shows the architecture of a VD. The VD unit has a data shift register, counter, add-compare-select (ACS) module, and traceback module (TBM). The hard decision-based VD is employed to generate the decoded bits. The path metric module (PMM) is another name for the ACS module. The ACS module adds, compares, and selects actions to calculate the path metric. The decision bits are located in eight ACS modules. Each ACS module generates the 2-bit decision bits. As a result, the TBM of the trellis state uses 16 decision bits. Once the trace path was reconfigured, the data shift register received the TBM data and was shifted right to create the correct 1-bit output ($dout$).

The detailed hardware architecture of the VD is illustrated in Figure 6. This work uses eight ACS modules (ACS-0 to ACS-7). The lower data bits ($m0, m1, m2, m3, m4, m5, m6$, and $m7$) and upper data bits ($m8, m9, m10, m11, m12, m13, m14$, and $m15$) are inputs to the ACS module. Each ACS unit has two 6-bit

lower and upper data bits along with 3-bit received input data as input. The decision bits in the VD design are located using 8 add-compare-select unit (ACSUs). The received data are combined with fresh path metric data to determine the lower and upper data. The lower data bits are compared to the upper ones to see the new path metric data and determine the decision. Each ACSU generates the 2-bit decision bit (t). Hence, eight ACS modules produce the 16-bit decision bits. So, the TBM of the trellis state continues to employ 16 decision bits.

The 16-bit choice values are sent to the TBM along with a counter, which it uses to determine the optimum route. The memory unit for keeping the history of the decision bit from the ACSU is in the TBM. Based on the counter values, a memory unit stores the decision bits. The 16 values in memory serve as decision vectors for every trellis state at every clock cycle. The optimum trellis path can then be recreated using the decision vector. TBM produces 20-bit data to shift the register to generate the decoded data. To generate an appropriate 1-bit output, the shift registers finally got the TBM data and shifted right.

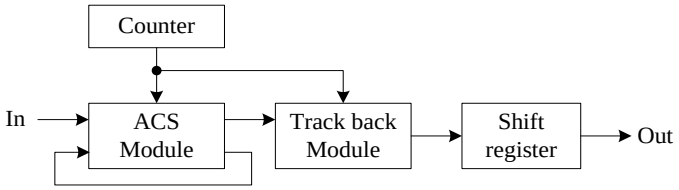

Figure 5. Hardware architecture of Viterbi decoder

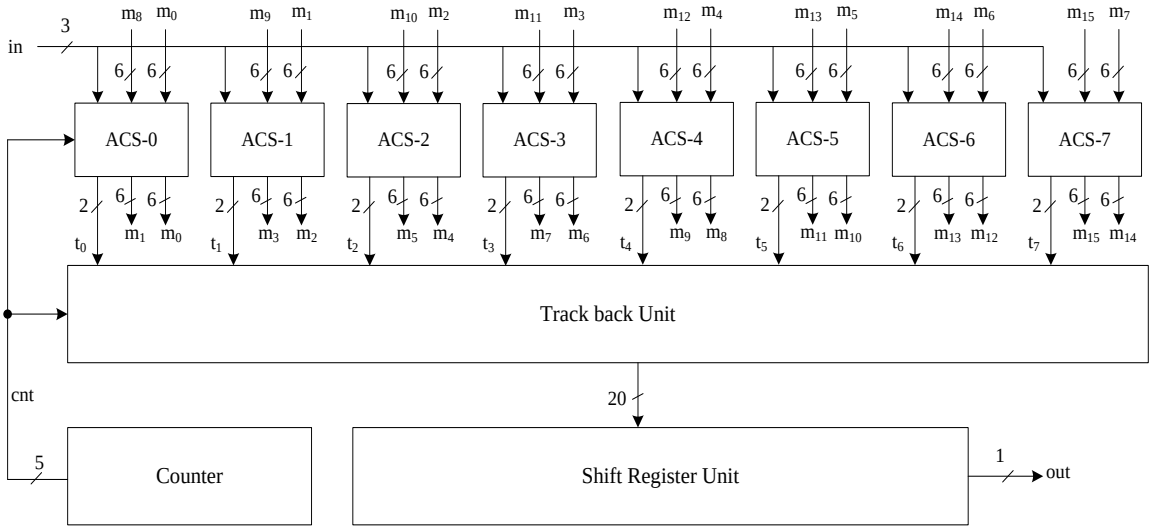

Figure 6. Detailed hardware architecture of Viterbi decoder

4. RESULTS AND DISCUSSION

The synthesized results of the BCC transceiver are discussed in this section. The BCC transceiver (TR) is designed and implemented on the Artix-7 FPGA using Verilog-HDL in the Xilinx ISE environment. The implementation results like chip area (Slices, Look-Up Tables (LUTs), and LUT-flip-flops (FFs)), maximum operating frequency, and power of the BCC-TR and its sub-modules are realized after place and route operation in Xilinx Tool. The resource utilization of BCC-TR and its sub-modules on the Artix-7 FPGA is tabulated in Table 1. The graphical representation of the BCC-TR system's resource utilization is shown in Figure 7.

The BCC transmitter (TX) utilizes the slices of 77 and LUTs of 198 with a maximum frequency of 267.236 MHz. Similarly, the BCC receiver (RX) utilizes the slices of 253 and the LUTs of 651 with a maximum frequency of 268.9 MHz. The BCC-TR obtains the slices 310 and 778 with a maximum frequency of 268.7 MHz. The power is calculated using the Xilinx power analyzer (XPA) tool after place and route operations. The BCC-TX, BCC-RX, and BCC-TR consume a total power of 102 mW, 98 mW, and 111 mW,

including dynamic power of 19 mW, 16 mW, and 29 mW, respectively. The BCC-TX consumes more dynamic power than the BCC-RX due to internal input-output (IO) port usage. The IO ports consume a dynamic power of 14 mW out of 19 mW in BCC-TX. The overall chip area utilization of the BCC-TR and its sub-modules is < 1% on the Artix-7 FPGA.

Table 1. Resource utilization of BCC-TR and its sub-modules on artix-7 FPGA

Resources	BCC TX	BCC RX	BCC TR
Slices	77	253	310
LUTs	198	651	778
LUT-FF pairs	72	190	244
Max frequency (MHz)	267.236	268.9	268.77
Dynamic power (mW)	19	16	29
Total power (mW)	102	98	111

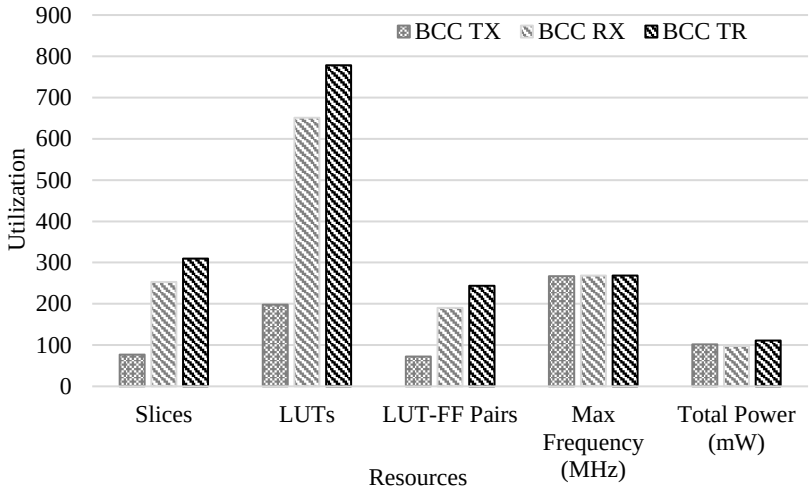

Figure 7. Graphical representation of BCC-TR system's resource utilization

The performance results of the BCC-TR system are tabulated in Table 2. The performance metrics like Latency, throughput, and efficiency are realized for the BCC-TR system. The Latency is calculated in terms of clock cycles (CC). The throughput or data rate for Megabits per second (Mbps) is determined using Latency, data size, and obtained frequency on an FPGA device. The BCC-TR obtains a Latency of 19.5 CC with a throughput of 13.78 Mbps and an efficiency of 44.46 Kbps/slice. The operating frequency of 100 MHz is considered in most BCC transceivers for WBAN applications. So, the proposed BCC-TR obtains a throughput of 5.13 Mbps with an efficiency of 16.54 Kbps/Slice at 100 MHz frequency. The BCC-TR system achieves the BER of $>10^{-7}$ under channel (human body) conditions.

Table 2. Performance results of BCC-TR system

Performance metrics	BCC-TR results
Latency (CC)	19.5
Throughput (Mbps)	13.78
*Throughput (Mbps) at 100 MHz	5.13
Efficiency (Kbps/Slices)	44.46
*Efficiency (Kbps/Slices) at 100 MHz	16.54
BER	10^{-7}

The performance comparison of the proposed BCC-TR with existing FSK approaches is tabulated in Table 3. The design approach, CMOS technology, frequency band, core voltage used, obtained data rate, and BER are considered performance parameters for comparison. The BCC-TR is designed using the FSK approach [24] using 65 nm CMOS technology. The BCC-TR [24] operates in a 1 to 30 MHz frequency band with a core voltage of 1.1 V and obtains a 1 Mbps data rate with a BER of 10^{-7}. The BCC-TR with FSK approach [25] using 65 nm technology is designed. The BCC-TR [25] operates in a frequency band of

30 MHz with a core voltage of 1.1 V and obtains a 2 Mbps data rate with a BER of 10^{-6}. The BCC-TR with FSK approach [26] obtains a data rate of 1 Mbps with a BER of 10-6. The narrowband (NB)-based BCC is designed using the FSK approach [26] on 90 nm CMOS technology. The NB-BCC-TR [27] operates in a frequency band of 50 MHz with a core voltage of 5 V and obtains a 0.14 Mbps data rate with a BER of 10^{-4}. The HBC-TR is designed using the FSK approach [28] on 90 nm CMOS technology. The HBC-TR [27] operates in a frequency band of 50–60 MHz with a core voltage of 1.2 V and obtains a 2 Mbps data rate with a BER of 10^{-6}. The proposed BCC-TR uses the FSK and convolutional code (CC) approaches on 28 nm technology (FPGA). The proposed BCC-TR operates in the 1 to 100 MHz frequency band with a core voltage of 1 V and obtains a 5.13 Mbps data rate with a BER of 10^{-7}. The proposed BCC-TR obtains a better data rate with a lower BER than other BCC-TR systems using the FSK approach. The resource comparison of the proposed BCC-TR system with similar transceivers on the FPGA platform is tabulated in Table 4. The design approach, FPGA used, chip area (slices and LUTs), obtained maximum frequency on the device, total power, BER, and obtained data rate are considered resource parameters for comparative study.

Table 3. Performance comparison of proposed BCC-TR with existing approaches

Parameters	Ref [24]	Ref [25]	Ref [26]	Ref [27]	Ref [28]	Proposed work
System	BCC	BCC	BCC	NB-IBC	HBC	BCC
Approach	FSK	FSK	FSK	FSK	FSK	FSK + CC
CMOS technology	65	65	65	90	90	28
Frequency band (MHz)	1 to 30	30	30	50	50-60	1-100
Core voltage (V)	1.1	1.1	1.1	5	1.2	1
Data rate (Mbps)	1	2	1	0.14	2	5.13
BER	10^{-7}	10^{-6}	10^{-6}	10^{-4}	10^{-6}	10^{-7}

Table 4. Resource comparison of proposed work with existing transceivers on the FPGA platform

Parameters	Ref [29]	Ref [30]	Ref [31]	Ref [32]	Proposed work
Transceiver	HBC	BCC	PHY-BCC	HBC	BCC
Approach	FSDT	WBS+ CC	MC	FSDT	FSK + CC
FPGA used	Artix-7	Virtex-2	Artix-7	Artix-7	Artix-7
Slices	NA	6649	1646	196	310
LUTs	5231	5272	2517	1137	778
Frequency (MHz)	32	100	231.28	255.31	268.77
Power (mW)	113	158	113	101	111
BER	10^{-6}	$< 10^{-8}$	NA	$< 10^{-4}$	10^{-7}
Data rate (Mbps)	6	3.125	7.7	9.52	13.78

The HBC-TR with frequency-selective digital transmission (FSDT) approach [29] is designed on an Artix-7 FPGA. The proposed BCC-TR reduces the area overhead by 85.2% for LUTs, frequency by 88%, power by 1.8%, and data rate by 56.45% compared to HBC-TR [29]. The BCC-TR with wideband signaling (WBS) with convolutional codes (CC) approach [30] is designed on a Virtex-2 FPGA. The proposed BCC-TR reduces the area overhead of 95.3% for slices, 85.2% for LUTs, frequency of 62.7%, power of 42.4%, and data rate of 77.3% compared to BCC-TR [30]. The PHY-based BCC-TR with Manchester coding (MC) approach [31] is designed on an Artix-7 FPGA. The proposed BCC-TR reduces the area overhead of 81.3% for slices, 69% for LUTs, frequency of 13.5%, power of 1.8%, and data rate of 44.12% compared to the PHY-based BCC-TR [31]. The HBC-TR with FSDT approach [32] is designed on the Artix-7 FPGA. The proposed BCC-TR reduces the area overhead by 31.5% for LUTs, the frequency by 4.8%, and the data rate by 39.9% compared to HBC-TR [32]. Most of the existing TR system uses a voltage-controlled oscillator (VCO) for sine wave generation in FSK modulation and demodulation, which utilizes most of the chip area and power in the transceiver system. The proposed BCC-TR using FSK uses simple DSS for sine wave generation, improving performance with less chip area and power.

5. CONCLUSION

In wireless body-area networks, this research presents a unique BCC transceiver that is optimized for efficiency and compactness (WBANs). Our novel architecture paves the way for wearable applications of the future by outperforming current approaches in key areas. The suggested transceiver is incredibly resource-efficient; it takes up very little space on an Artix-7 FPGA chip (less than 1 percent). It is remarkably efficient, using only 111 mW at 268.77 MHz, making it perfect for wearables that run on batteries. It also has a 13.78 Mbps data throughput, which is outstanding and faster than similar designs. Additionally, it allows

real-time communication for crucial applications with a low latency of 19.5 clock cycles. Its remarkable BER of more than 10^{-7} under genuine body channel conditions, however, which guarantees extremely dependable data transfer, is what really makes it stand out. In conclusion, a novel BCC transceiver with notable gains in important performance parameters is presented in this work. Future studies will concentrate on incorporating security features and investigating alternative implementation platforms for even wider applicability. We feel it offers enormous potential for next-generation WBAN applications.

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