Energy efficient improved content addressable memory using quantum-dot cellular automata

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Article Info

ABSTRACT

Quantum-dot cellular automata (QCA) is an emerging technology with high integration density, low power consumption, and high operating speed. This study introduces a QCA-based modified content addressable memory (CAM) cell employing a five-input minority gate. The functionality, temperature sensitivity, and heat distribution of this modified CAM cell are comprehensively analyzed using QCADesigner E and QCA Pro simulation tools. The results reveal significant advancements over existing designs, with a remarkable 8.33% reduction in area and a substantial 63.7% decrease in energy consumption. Additionally, this modified CAM cell exhibits a notable 5% enhancement in temperature tolerance. These findings emphasize the QCA-based modified CAM cell is more efficient and thermally robust.

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1. INTRODUCTION

In recent years, metal oxide semiconductor (MOS) technology has met the challenges to be solved, which are high energy consumption and physical limitation of transistor dimension [1], [2]. In response to this conundrum, the nanoscale devices are fabricated with graphene as the semiconductor material [3], [4]. Further scaling the device at atomic level quantum-dot cellular automata (QCA) has emerged as a compelling and avant-garde technological avenue [5], [6]. QCA is positioned as an alternative to conventional MOS technology, offering promises of unprecedented improvements in circuit speed and compactness. The QCA as a transformative technology that holds the potential to redefine the scenery of electronic circuitry [7], [8]. Through a detailed examination of QCA principles, advantages, and challenges, this study aims to shed light on the transformative potential of this innovative approach in the ongoing quest for advanced and efficient memory design for the integrated circuits.

In this internet of things (IoT) era, to deal with big data and artificial intelligence, high speed and low power consumption memory modules are essential in data-retrieving applications. QCA-based content addressable memory (CAM) modules [9], [10] are suitable for this application. CAM is considered as a high-speed memory module due to its parallel searching operation method. In the literature, CAM cells are designed with majority gates as basic building blocks [11], [12]. Further research can be extended to improve the efficiency of CAM cell [13], [14].

In this paper, a modified CAM cell utilizing the minority gate is presented, to improve the efficiency. All simulations are executed utilizing the QCADesigner E simulation tool, Additionally, power

dissipation analysis is carried out using QCA Pro. The subsequent sections are structured as follows: section 2 describes the background on QCA technology and related works on QCA CAM cells. Section 3 describes the proposed CAM cell design is presented in section 4 along with simulation results. In section 5, conclusions are drawn based on the findings and implications of the study.

2. BRIEF BACKGROUND OF RELATED WORKS

QCA cell is a square-shaped structure that has four dots, among them two dots are occupied by the electronic charge, based on columbic repulsion. The charge distributed among the four dots is termed as polarization. Binary values 0 and 1 are derived from the charge configuration, with polarization -1 and 1 [15]. A chain of cells with fixed polarization at the left most cell acts as a QCA wire with current flow. In this way, QCA technology provides a way for signal transmission. QCA clock plays a vital role in powering the circuit and signal transmission. Four clocking zones such as switch, hold, and then release, relax, each zone has a phase shift of 90° as shown in Figure 1. In the release zone cells get polarized, and in the switch phase signal is raised and maintained high in the hold phase. In the relaxation phase cell becomes unpolarized [16].
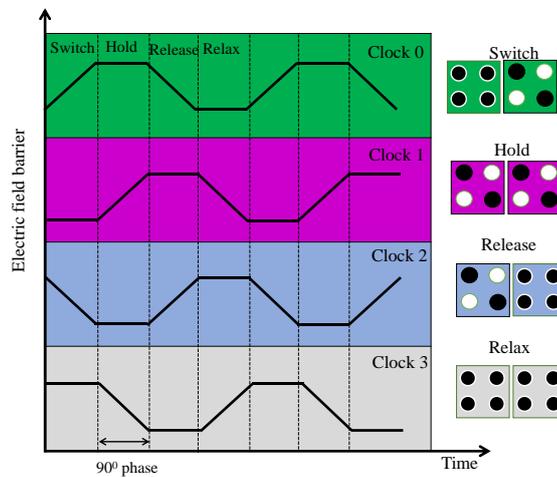

Figure 1. Clock distribution scheme of QCA cell

In a content addressable memory, when the input data word is applied to search, it looks for the data stored in the memory. After that it returns the address value, i.e., memory location where the searched data is stored. This entire operation is done using an active parallel circuit in a single clock cycle [17], [18]. The CAM circuit has the memory and matching parts. The data input and the read/write signal are received by the memory part, meanwhile the matching part gets the memory cell contents accompanied by arguments along with key signals as well. This construction enables the match signal set in case the queried data existed and reset in another case [19], [20]. The block diagram of CAM circuit is shown in Figure 2.
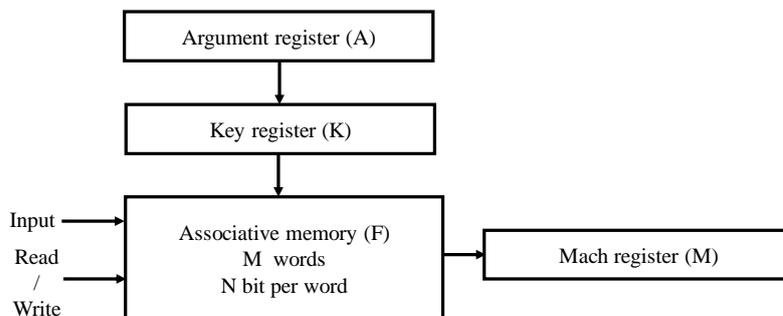

Figure 2. Block diagram for CAM cell organization

In the literature, the maximum of the existing CAM architectures is designed by using the majority gates [21], [22]. The CAM architecture consists of 7 majority gates with 6 three inputs and 1 five input. The memory unit input signal receives the signal and write the data as well as read [23], [24]. The design of CAM cell using majority gates is shown in Figure 3. In this paper, we have proposed CAM architecture using five input minority gates, which is much better than the five input majority CAM circuit in the terms of output robustness and temperature sensitivity.
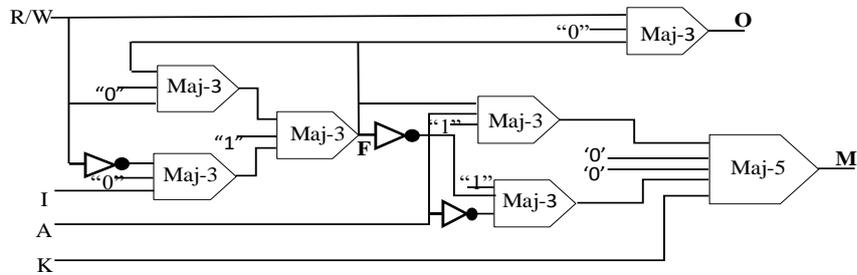

Figure 3. Implementation of basic CAM cell

3. DESIGN OF PROPOSED CAM CELL AND RESULTS

The QCADesigner tool is used to design the proposed CAM circuit. The proposed CAM cell is designed with minority gate and shown in Figure 4. For the efficient design, a highly robust five input minority gate is used. The memory unit received an R/W signal and keeps a record of the previous output data, and the matching unit (M) matches the data with the current input data if the data is matched, the address of the data is returned and it has to be taken care that only address is returned, not the actual content. The circuit has an XNOR gate and RS flip flop, the XNOR gate works as a matching unit, and the RS flip flop works for its memory unit.
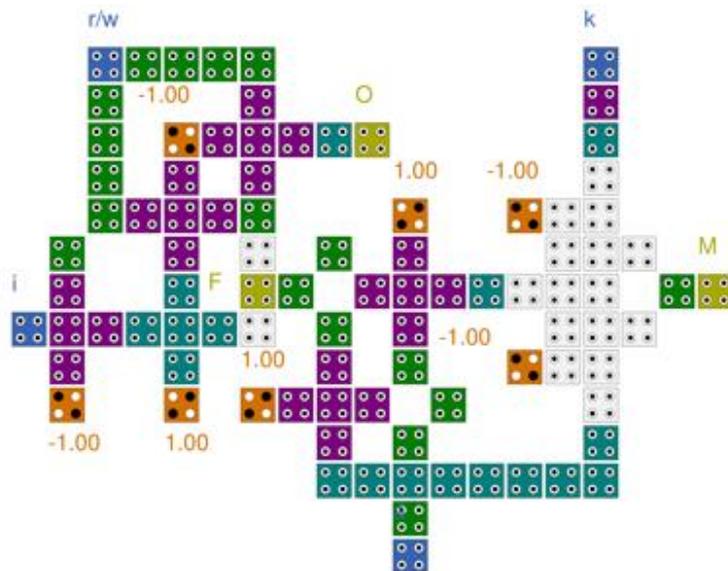

Figure 4. Proposed CAM cell by using the five input minority gate

Table 1 describes the operation of the memory cell. From Table 1, it can be observed that during the write operation, the R/W signal = 0 and F(t) is a do not care condition the value of input we are giving to the input (t) will go to the output $F(t + 1)$. For example, when is input is 1 and the value of $F(t + 1)$ becomes 1. Similarly, when the read operation, the signal for the R/W port = 1. The value of $F(t)$ will goes to $F(t + 1)$ irrespective of the input signal conditions. The match unit operation is described in Table 2. When K=0, independent of A and $F(t)$ conditions the value of M sets to 1. The ports A and $F(t)$ activated when K=1.

For the case of *A*=0 and *F(t)*=0, the *M* produces the value 1 and also for the case *A*=1 and *F(t)*=1. This means that the match operator produces 1 when both Augment and port *F* are same. For the remaining test cases, where *A* and *F(t)* are different, the value of *M*=0.

The version of the software used is 2.0.3 for designing, simulating, and verifying the CAM cells. The power is estimation using QCA Pro. The methods of simulation engines available in QCA are bistable and coherence vector approximation techniques [24]. The default simulation parameter values are used for both the simulations.

For the comparison, the previously presented [25] circuit design is also simulated. Using the RS flipflop, the memory unit is implemented and the match unit is implemented using the XNOR gate. The results are placed in Figure 5. It is observed that the existing CAM cell output is noisy and difficult to get the full rail-to-rail swing in the output O. The QCADesinger simulation results of proposed circuits are placed in Figure 6. The output of five input minority gate is shown in Figure 6(a) and the results of proposed CAM cell are placed in Figure 6(b). From the Figure 6(a), it can be noticed that the output function is acts like a minority voter gate. The minority value of the input is transferred to the output. From Figure 6(b), it can be observed that the designs are highly robust and also observed the full rail-to-rail swing at the output.

Table 1. Memory operation

Input(I)	Operation	R/W	F(t)	F(t+1)
1	Write	0	X	1
0	Write	0	X	0
X	Read	1	0	0
X	Read	1	1	1

Table 2. Match operation

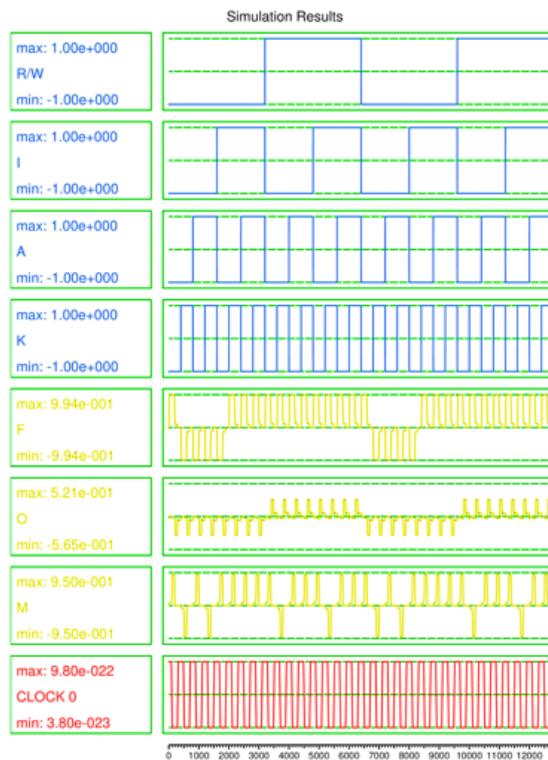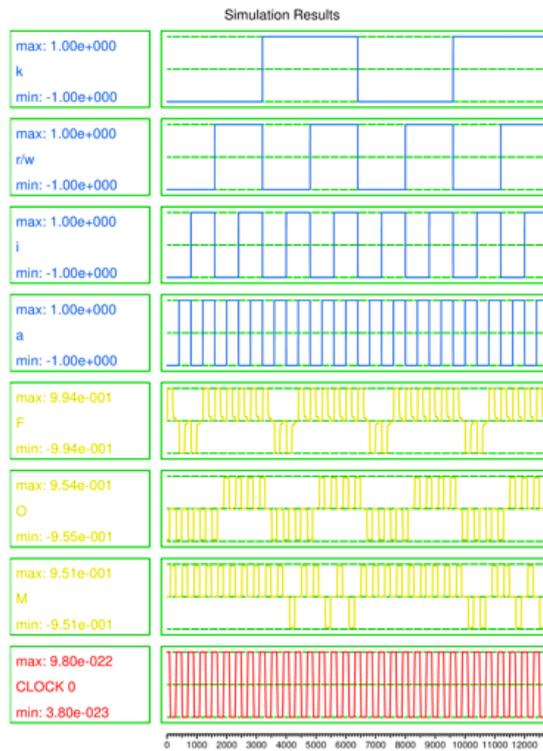| K	A	F(t)	M
0	X	X	1
1	0	1	0
1	0	0	1
1	1	1	1
1	1	0	0

Figure 5. Simulation waveform existing CAM cell by using five input majority gate [25]

(a)

(b)

Figure 6. Simulation results of (a) five input minority gate and (b) proposed CAM cell

The other performance parameter comparison among the proposed CAM circuit and existing circuits like total energy dissipation, average energy dissipation, and latency are shown in Table 3. The CAM area presented in the literature [17], [19], [25] are respectively measured as 0.14, 0.11, and 0.12 µm², whereas the

proposed CAM cell occupies the area of 0.11 μm². The proposed CAM and [19] occupies the same area, however, the power dissipation is several times smaller than the existing circuits. The percentage of reduction in total energy consumption is almost 74% with respect to the circuit presented in [17]. We may draw from the results that the suggested approach to the design of CAM circuit show better results compared to existing literature. We also investigated the temperature effects on proposed CAM cell output polarization. Figure 7 shows the findings of this analysis. From Figure 7(a), the existing CAM cell polarization is more unstable and also noticed that the slope for the match line is very high. The proposed CAM cell temperature sensitive analysis is shown in Figure 7(b), it is observed that the proposed is more stable and variations for both O and M are low with a moderate slope.

Table 3. Performance parameter comparison of proposed CAM circuit

Design Type	Area (μm²)	Performance Parameters Total energy consumption (meV)	Layer Type
CAM [17]	0.14	282.85	single
CAM [19]	0.11	167.56	single
CAM [25]	0.12	197.12	single
Proposed CAM	0.11	71.54	single

In general, the power dissipation analysis of the circuits on the entire circuit and it delivers the either average value or the total dissipation value [26]. However, in QCA due to the confinement of the electron flow we need to analyze the power dissipation of each cell by analyzing the thermal maps [27], [28]. The thermal map shows the rate of power dissipation of each cell. Using the QCA Pro tool, we can plot the intensity curves for each circuit. In Figure 8, the thermal map of proposed CAM circuit is presented. The darker cell in the thermal map represents more power dissipation and the lighter one represents less. It can be observed that the QCA cell with voting decision dissipating more heat compared to the other cells. The total number of critical cells that dissipates more power is observed to be 5.
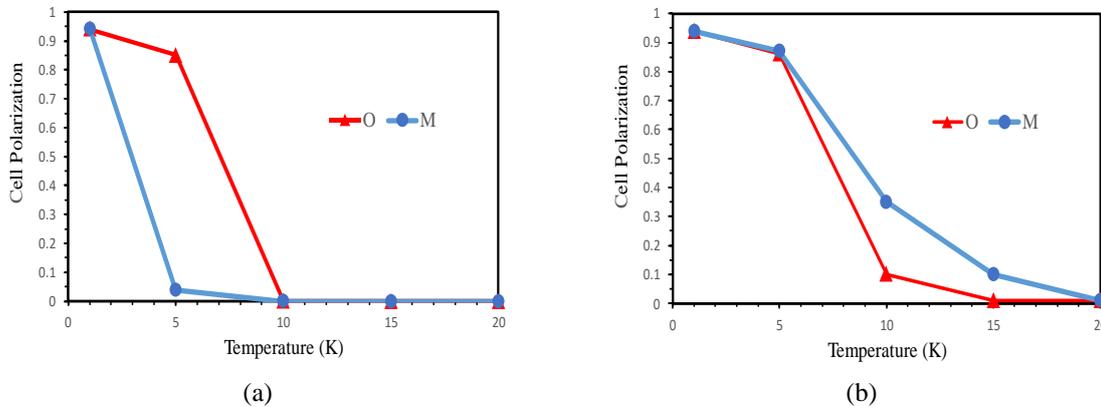

(a)   (b)

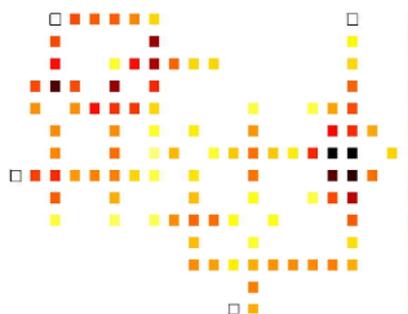Figure 7. Effect of temperature changes (a) existing CAM cell [25] and (b) proposed CAM cell

Figure 8. Thermal map of proposed CAM cell

4. CONCLUSION

The energy efficient improved CAM cell is designed in this work. The proposed CAM cell is extensively simulated using QCA designer tool. The proposed design is based on the minority gate, whereas most of the existing CAM cells are based on the majority gates with five inputs. With the comparison of existing circuits, the proposed design is highly robust and also has the highest noise margin.

We also performed the temperature sensitive analysis of the proposed design. The proposed design is less sensitive to temperature effects. The existing circuit output polarization drops quickly with an increase in temperature. For instance, the polarization drops to 50% with increase of 2.5K, whereas for the proposed design, the polarization is almost constant at 2.5K. The power dissipation is also performed and noticed that the proposed CAM circuit is more power efficient and most of the energy is dissipated at the voting cell and less energy is dissipated at input and output ports. The proposed CAM circuit will be useful for miniaturization of integrated circuits and can be used for the high-speed memory designs.

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