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# Electrical signal interference minimization using appropriate core material for 3D integrate circuit at high frequency applications

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**ABSTRACT**

As demand for smaller, quicker, and more powerful devices rises, Moore's law is strictly followed. The industry has worked hard to make little devices that boost productivity. The goal is to optimize device density. Scientists are reducing connection delays to improve circuit performance. This helped them understand three-dimensional integrated circuit (3D IC) concepts, which stack active devices and create vertical connections to diminish latency and lower interconnects. Electrical involvement is a big worry with 3D integrates circuits. Researchers have developed and tested through silicon via (TSV) and substrates to decrease electrical wave involvement. This study illustrates a novel noise coupling reduction method using several electrical involvement models. A 22% drop in electrical involvement from wave-carrying to victim TSVs introduces this new paradigm and improves system performance even at higher THz frequencies.

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## 1. INTRODUCTION

Over the previous four decades, Moore's law has shortened device lengths, improving integrated circuit performance. Integrate circuits (ICs) employed horizontal gates during precise scaling. Now there are two more challenges. The first hinders device scaling. Interconnections restrict system display, which is the biggest issue. The major limitation, connection disruption, is almost inseparable from device latency. System performance requires innovative designs and novel connecting materials. Interconnection latency has been diminished by new integration methodologies [1], [2].With its capacity to stack several layers of devices with bigger interconnects, Three-dimensional (3D) integration method is promising for complementary metal-oxide semiconductor (CMOS). The ability to combine independently manufactured parts is another characteristic of three-dimensional integrate circuit (3D IC). Common methods for integrating three dimensions include wafer-on-wafer (W-o-W), chip-on-chip (C-o-C), and chip-on-wafer (C-o-W) stacking. One common technique for vertical device integration in the semiconductor industry is Cu-Cu-WoW bonding [3]–[10]. Modern hardware [11]–[16] integrated in three dimensions may enhance system performance. Core materials and various liners can withstand high frequencies. THz frequencies were used to study the proposed architecture. One system must incorporate several new technologies and approaches. Therefore, 3D ICs are the ideal systems for such a wide variety of purposes. If the platform is to succeed, 3D ICs' intriguing issues must be solved. This study addresses device and structural issues with 3D ICs. Electrical and thermal models

are used to represent through silicon via (TSVs) in this three-dimensional IC arrangement. TSVs can be converted for the 3D gateway, although it will create complications. For sophisticated 3-D integrated circuits, we provide a number of models, materials, and circuit methodologies for studying and fixing platform coupling issues including TSV-substrate noise coupling. This research presents a new approach to reducing electrical involvement in TSV designs by using different dielectric liner and core materials. A number of different types of liner materials and core materials may be processed at high frequencies using the electrical wave carrying (ETSV) technology. The suggested design was studied using THz frequencies.

## 2. LITERATURE STUDY

Efficiency and user-friendliness in system operation have always been primary goals of development and scaling. For any mixed system, 3D IC provides a platform that accommodates the particular technologies, processes, and materials that are anticipated to coexist inside it. Several researchers have used dielectric materials, shielding, and surrounding TSVs to enhance electrical engagement. A lot of these ways are either too time-consuming or too costly. Using thorough levels and crossings from all these new devices, this work successfully overcomes several critical 3D IC challenges, improving system performance while minimizing chip size and area.

The three interconnects in three-dimensional silicon interposer (3DSI) topologies are metal, TSV, and redistribution layer (RDL). There has been evaluation and examination of the interconnection linkages both individually and in combination. This study accurately measures and models electrical characteristics of 3DSi interposers with IC interconnects up to 20 GHz [17] by evaluating them using the S-parameter.

Uemura *et al.* [18] detailed TSV-based noise coupling techniques that disperse the wave across many substrates. The finest performance, efficiency, cost-effectiveness, and usefulness are offered by radio frequency (RF) or mixed waves because of CMOS technology. But digital system noise and circuit sizes are on the rise. RF circuits are susceptible to digital noise that is generated by the substrate. Between radio frequency and digital electronics, there must be a significant decrease in noise. He separated noise and found out what happened by using electrodes made of a Cu outer layer and a TSV inner layer [18]. A large number of TSV prototypes and the electrical involvement of 3D ICs were examined by Kim *et al*. [19] using TSV, or upright interconnection, is the ideal way to build 3D IC systems. A newly developed, tested, and matched high-frequency TSV electrical prototype up to 20 GHz has the potential to make TSV-based 3D ICs more practical and dependable [19]. A TSV noise coupling system was built by researchers using three-dimensional transmission line modeling (TLM) [20].

Assuming the TSVs would be insulated by their lined structure, the noise coupling conductance surrounding them was first verified by the researchers. Their hypothesis of a three-dimensional, multi-layered structure to reduce noise coupling was proven correct. Noise isolation is over 40% when utilizing Benzocyclobutene (BCB), copper, and BCB or Teflon, copper, and Teflon to confirm the findings [21], [22]. Because of the challenges associated with producing TSVs and the lower melting point of Teflon, the via-middle technique was chosen by the industries. For their project, they settled on a 30 nm BCB dielectric and a 90 nm Cu metal thickness. Stacking liner arrangement and one-liner construction separated TSVs. Researchers looked examined BCB, Teflon, SiO2, Cu, and Polysilicon to see whether they might inhibit electrical involvement [23]–[25].

Using stacked electrical TSVs (ETSVs), ETSVs with heat sources, and the correct dielectric material lining aggressive TSVs are all ways that researchers hope to reduce electrical wave disturbance. In noise coupling experiments, the conductivity of the wave-carrying TSV was improved and the electrical involvement between the aggressor and victim TSVs was reduced when non-copper core materials were used. The proposed designs were tested using CMOS-compatible materials and a finite element model (FEM) simulator [26]–[28].

## 3. PARAMETERS FOR SIMULATION AND ITS DESIGN

Using several models across chips diminishes background noise during 3D IC integration. TSVs stack chips electrostatically and vertically for 3D IC synchronization. The performance-to-noise-coupling ratio of 3D integrated networks wield TSVs is a serious trouble. To interface with other active devices, 3D ICs need TSVs. The major issue is that the victim's TSV may take up electrical signaling route noise. This research shows that changing core materials for liners may lessen noise coupling between ETSV and victim TSV and TSV and silicon.

It has been shown and examined that the strong TSV-victim TSV noisy connection exists. TSV pitches are typically between 2 and 8 meters, as stated in the ITRS International Technology Roadmap for Semiconductors (ITRS) roadmap, which is a semiconductor roadmap document. Finite element analysis and the three-dimensional integrated circuit model shown in Figure 1 have the potential to evaluate and simulate

the electrical involvement between wave-carrying TSVs and victim TSVs. Electrostatic and thermal physics are what are used in FEM modeling. Table 1 reveals that the TSVs are 0.15 m thick, 8 m tall, and 0.2 m thick, with a total area of 4 µm. Many dielectric materials with different ratios were simulated.

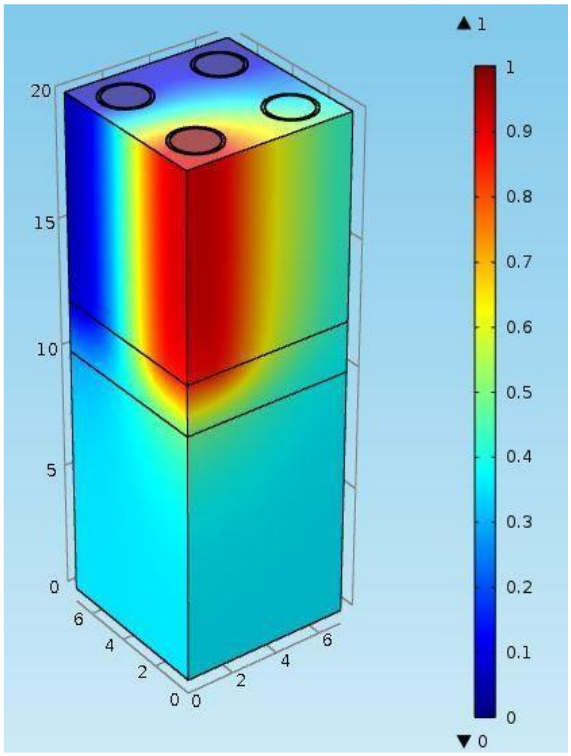


Figure 1. 3D IC structure model consisting of several blocks

Table 1. ITRS Road map variables

| Variable | Value |
|---|---|
| Diameter of TSV | 2 µm |
| Thickness | 0.2 µm |
| Height of TSV | 10 µm |
| Aggressive TSV to victim TSV distance | 4 µm |
| Pitch | 2 µm |

Modern 3D ICs employ SiO2, BCB, Teflon, and Perylene-D. Each dielectric substance was helpful in electronics. Industrial, glass, and optical industries use SiO2, which has a dielectric constant of 3.9. Benzocyclobutene (BCB) is turned into photosensitive polymers and coated on various substrates for micro electromechanical systems (MEMS) and mechanical, electrical and plumbing (MEP). The 2.5 dielectric constant makes it suitable for optical interconnects and wafer bonding. The cheap cost of silicon (Si) makes it the substrate material of choice for the majority of applications, including those involving memory and processors. The typical circuit uses several dielectric materials. Table 2 lists several dielectric materials' electrical resistivity and dielectric constants. Noise coupling studies depend on material resistivity and dielectric constant. Dielectric materials are utilized to study a limited noise coupling range.

Table 2. Liner materials and their simulated properties

| | SiO2 | BCB | Teflon | Perylene-C | Perylene-N |
|---|---|---|---|---|---|
| Dielectric constant | 3.90 | 2.50 | 2.30 | 2.950 | 2.20 |
| Volume resistivity (Ω·m) | $>10^{18}$ | $1\times10^{19}$ | $10\times10^{22}$ -$10\times10^{24}$ | $8.8\times10^{16}$ | $1.4\times10^{17}$ |
| Melting point (MP) | >1500 | 350 | 327 | 290 | 420 |
| Coefficients of thermal conductivity (W/mK) | 1.40 | 0.30 | 0.250 | 0.0840 | 0.1260 |
| Co-efficient of thermal expansion | 0.50 | 42 | 1.20 - 1.70 | 35 | 69 |

## 4. RESULTS AND DISCUSSION

Multiple models combine 3D ICs with diminished noise in abundant ICs. Vertical stacking and electrical alignment of 3D IC chips are possible with TSVs. Current TSV-based 3D-integrated circuits suffer from noise coupling, reducing system performance-to-size. Electrical wave transfer linking 3D ICs and other active devices depends on TSVs. Noise coupling linking the victim and electrical waves TSVs causes the most problems. By changing the core material with a stronger electrical conductor, this research shows how to diminish electrical involvement between an ETSV and a substrate or victim TSV. The ETSV model in Figure 1 also tested standard SiO2 and other core materials. The core was made of electroplating- and CMOS-deposition-friendly materials with high electrical conductivity. Finally, COMSOL Multi physics simulates frequency response model up to 1 THz. Figure 2 shows ETSV type simulation with typical SiO2 dielectric and copper core. From Figure 2, the victim's TSV of 0.65 v is easy to compute. In the scenario, aggressive TSV (ETSV) conveys 1 Volt at 50 Hz.

Crystalline Silicon, Polysilicon, crystalline germanium, Polygermanium, and conductive zinc oxide were simulated using the same model as conventional SiO2 as the dielectric. An illustration of the participation of electrical waves from active TSV (ETSV) to victim TSV via a variety of core materials is shown in Figure 3. Each wave of ETSV is one volt. As shown in Figure 3, crystalline Ge core material is superior in its ability to reduce noise-coupling.

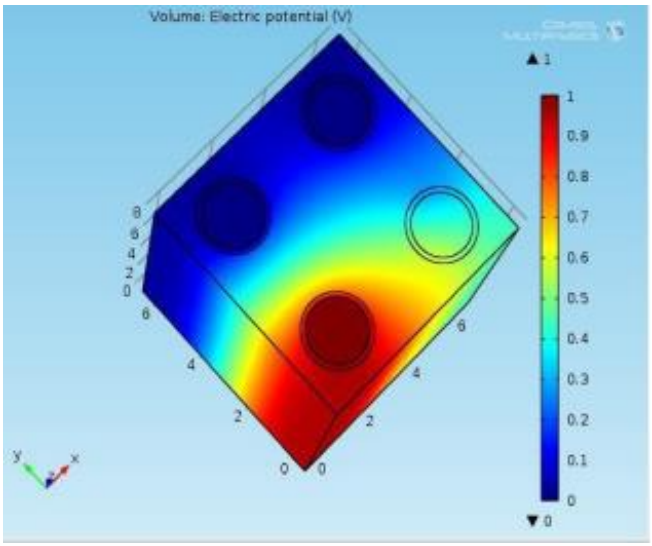


Figure 2. Top-view SiO2 electrical involvement study for ETSV concept

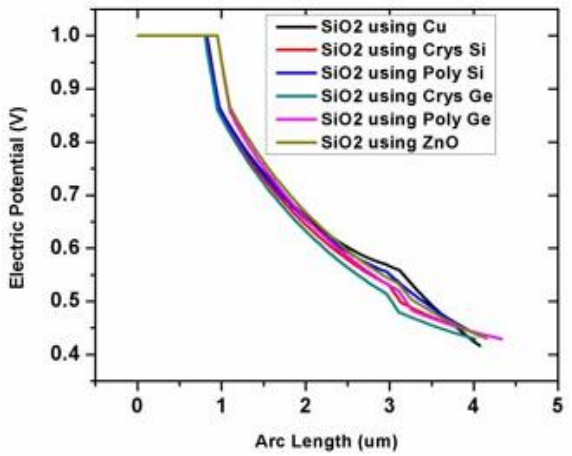


Figure 3. The ETSV's electrical wave is altered as it travels to the helpless TSV due to the SiO2 lining material

The ETSV scenario in Figure 1 was used in order to evaluate the electronic involvement between the wave-carrying TSV and substrate, as well as the ETSV and victim TSV. This evaluation was carried out via the utilization of Perylene-N dielectric material and different core materials. As may be shown in Figure 4, perylene-N reduces the electrical involvement of the ETSV sufferer by 0.45 V. The midway point between the transmitter and receiver TSVs is referred to as the wave distance. With a variety of the foundation and perylene-non as the dielectric liner, Figure 5 illustrates the electrical involved across wave-carrying TSV to substrate and ETSV to victim TSV.

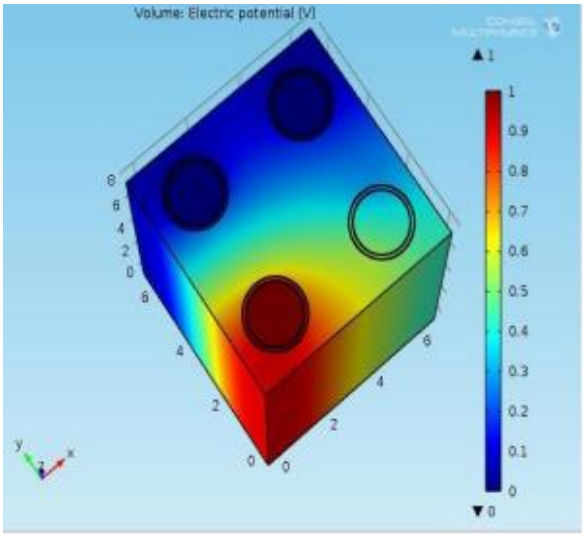


Figure 4. Perylene-N's dielectric characteristics were examined using an ETSV model for electrical involvement (top view)

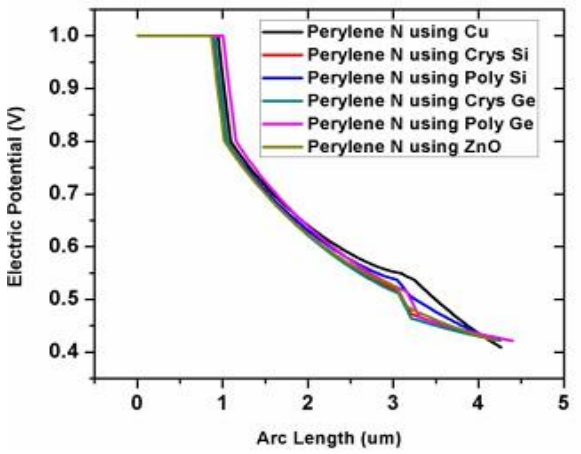


Figure 5. Electrical wave variation with perylene-N lining

Crystalline germanium, like SiO2 lining material, exhibits less electrical involvement than other core materials as shown in Figure 5. Electrical involvement was also tested using TSV waves up to THz. In ETSV model simulations, Perylene-N and Crystalline-Ge liners lower wave-to-noise ratios more than other liners as shown in Figure 6. Stacking and single liner structures containing Cu, Germanium, N-silicon, and P-silicon core materials are studied electrically using Benzocyclobutene (BCB), despite its low dielectric constant. The core materials were selected for their high electrical conductivity and ease of depositing using physical vapor deposition (PVD) or chemical vapor deposition (CVD), two processes often used by semiconductor manufacturers. Different electrical involvement is encountered by aggressive TSV (ETSV) and victim TSV, as seen in Figure 7. The ITRS road design specifies a distance of 4 um between the victim

and aggressive TSVs. The use of BCB dielectric for TSV noise coupling is shown in Figure 7. Research indicates that geranium performs optimally as a noise coupling material for single liner cores. Additional research has focused on multilayer liner structures made of BCB-dielectric. Using a layered liner architecture, the noise coupling between an ETSV and a victim TSV is examined in Figure 8. Figure 8 shows that compared to other core materials, P-Silicon has superior electrical involvement performance.

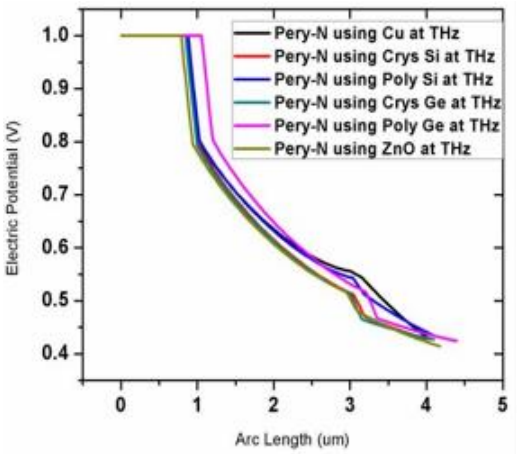


Figure 6. ETSV model dielectric material studies for electrical involvement at extremely high frequencies up to 1 THz

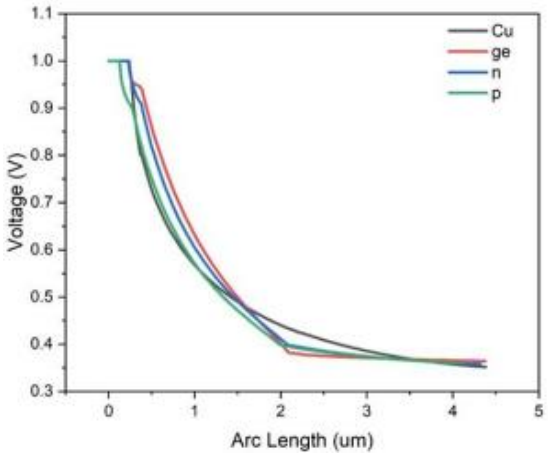


Figure 7. The effects of dielectric BCB on electrical involvement in a single-liner structure

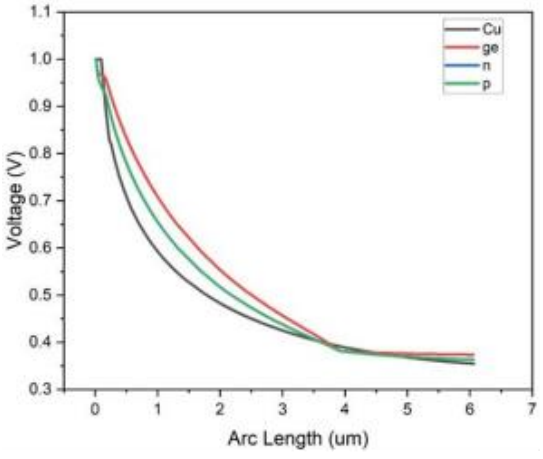


Figure 8. Evaluation of BCB as a dielectric in a layered liner construction for electrical involvement

## 5. CONCLUSION

Scaling and development efforts have always prioritized making the system as easy to use and effective as possible. A plethora of promising new methods, materials, and technologies are brought together by 3D-IC. This thesis reveals the many serious issues with 3D-IC and provides new methods to increase system efficiency while decreasing chip area and size, in addition to these innovative technologies. Using a combination of core materials and liner dielectrics, this study introduces a new approach to electrically lowering TSV structures. There are a number of core and liner materials used, some of which are high-frequency, in accordance with the electrical wave carrying (ETSV) idea. The suggested layout was evaluated at hertz (THz). For several liner systems using various core materials, the dielectric properties of perylene-N and BCB were studied. The results enhance electrical signaling and system performance by decreasing the electrical participation of ETSV to victim TSV. Using copper-based alloys such as Manganin and Constantan, we aim to enhance electrical engagement. For frequencies greater than one terahertz, a different model is used.

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