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Analysis of an operational trans-conductance amplifier with positive feedback

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ABSTRACT

In this paper, we present an analysis of an operational trans-conductance amplifier (OTA) with two positive feedback. The direct current (DC) transfer function is obtained by analyzing the OTA using the drain current in the weak inversion region. The analysis results were verified through comparison with SPICE simulations, and the characteristics of the DC transfer function analysis for the OTA design are well matched with the simulation results. The designed OTA dissipates a low power of 41.4 nW, and features the slew rate is improved by 436% compared to a conventional OTA without two positive feedback. Additionally, a DC gain and a unity-gain bandwidth is improved by 36 dB and 6.7 times, respectively. The OTAs are designed for the 0.18 μm complementary metal–oxide–semiconductor (CMOS) process.

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1. INTRODUCTION

The operational trans-conductance amplifiers (OTAs) are an analog circuit widely used at the input stage of amplifiers in integrated circuits, and high-performance OTA is becoming more important for low-power and low-voltage circuit purposes in mixed-signal integrated circuits. As a result, The OTA design consumes a significant amount of time in overall circuit design, and a lot of research is being done to improve it [1]–[5]. In order to increase design productivity in the entire circuit, the input OTA must be designed considering various specifications such as stability, low power, high DC gain, and unity-gain bandwidth. For these OTA input stages, the bulk-driven type is being widely studied these days for the purpose of low power consumption. However, this type of bulk-driven generates large input offset and noise due to reduced transconductance, which impairs the stability of the circuit [6]–[10]. On the other hand, the gate-driven type, which has been used for a long time, has a smaller input common range than the bulk drive type, but is excellent for use as an OTA input stage in all aspects such as simple structure, low power, small input offset, and large transconductance [11]–[23]. Much research has been done to increase the DC gain by using gate-driven type as the input stage of OTA and using positive feedback [24]–[27].

While conducting this research, we discovered a problem in [24]. This problem is in the process of solving (10) and (14) of [24], and we have correctly organized the equations and proven that (10) and (14) of [24] are erroneous. This paper also presents a DC transfer function analysis using the drain current in the weak inversion region for an OTA with two positive feedback. The presented analysis results proved that there were no problems through comparison and verification with SPICE simulation, and the characteristics of the DC transfer function analysis for OTA design matched well with the simulation results.

As for the remainder of the paper, section 2 presents circuit analysis concepts and gain enhancement techniques for each positive feedback of an OTA with two positive feedback. Additionally, SPICE code is presented for comparison with circuit analysis concepts. Section 3 discusses OTA design and simulation results that validate the proposed circuit analysis concept and strategy of gain enhancement techniques. Finally, in section 4, conclusions are presented.

2. CIRCUIT ANALYSIS

2.1. Input differential pair circuit analysis with positive feedback

Figure 1 is a schematic of the input stage of the designed OTA, and this circuit is characterized by positive feedback on the input differential pair and the active load, respectively. The DC gain is increased by these two positives feedbacks. Two equations that can control this DC gain are derived and explained. Table 1 shows the states of input differential pairs with positive feedback.

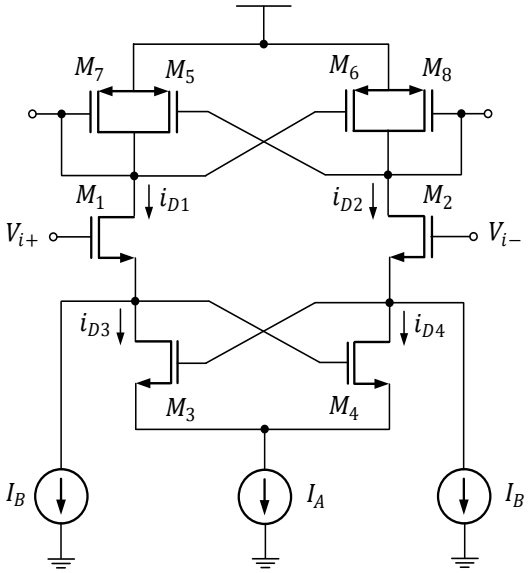

Figure 1. Input stage of the designed OTA

Table 1. States of input differential pair circuit with positive feedback

Operation condition	MOSFET state
Vi+ ↑	M1: ID1 ↓, Drain Voltage ↑
	M2: ID2 ↑, Drain Voltage ↓
	M3: ID3 ↓, Drain Voltage ↑
	M4: ID4 ↑, Drain Voltage ↓
Vi− ↑	M1: ID1 ↑, Drain Voltage ↓
	M2: ID2 ↓, Drain Voltage ↑
	M3: ID3 ↑, Drain Voltage ↓
	M4: ID4 ↓, Drain Voltage ↑

This input stage features a structure containing two current sources I_B. If there are no current sources I_B, the output characteristic operates like a comparator. Therefore, the operation of the amplifier becomes unstable. To find i_{D1}, i_{D2}, i_{D3}, and i_{D4}, we derive them in the following manner. When the input stage is gate-driven, the drain current in the weak inversion region is expressed as (1),

$$i_D = I_S \frac{W}{L} exp\left(\frac{v_{GS}-V_t}{nV_T}\right)\left[1 - exp\left(-\frac{v_{DS}}{V_T}\right)\right] \quad (1)$$

where I_S is the characteristic current, n is the slop factor in weak inversion region, V_T is the thermal voltage. When $V_{DS} \geq 4V_T$, the last factor can be omitted. The exponential relationship applied to each of M_1 and M_2 transistors can be written as (2),

$$i_{D1} = I_s \frac{W}{L} exp\left(\frac{v_{GS1} - V_t}{nV_T}\right) \quad (2)$$

$$i_{D2} = I_s \frac{W}{L} exp\left(\frac{v_{GS2} - V_t}{nV_T}\right) \quad (3)$$

These two equations can be combined to obtain,

$$\frac{i_{D1}}{i_{D2}} = e^{(V_{GS1} - V_{GS2})/nV_T} \quad (4)$$

which can be manipulated to yield,

$$\frac{i_{D1}}{i_{D1} + i_{D2}} = \frac{1}{1 + e^{(V_{GS2} - V_{GS1})/nV_T}} \quad (5)$$

$$\frac{i_{D2}}{i_{D1} + i_{D2}} = \frac{1}{1 + e^{(V_{GS1} - V_{GS2})/nV_T}} \quad (6)$$

$i_{D1} + i_{D2}$ is expressed as (7).

$$i_{D1} + i_{D2} = I_A + 2I_B \quad (7)$$

Using (7) together with (5) and (6), i_{D1} and i_{D2} can be obtained as (8) and (9).

$$i_{D1} = \frac{I_A + 2I_B}{1 + e^{(V_{GS2} - V_{GS1})/nV_T}} \quad (8)$$

$$i_{D2} = \frac{I_A + 2I_B}{1 + e^{(V_{GS1} - V_{GS2})/nV_T}} \quad (9)$$

In the same manner as above, i_{D3} and i_{D4} can also be obtained as (11) and (12).

$$i_{D3} + i_{D4} = i_{D1} + i_{D2} - 2I_B = I_A + 2I_B - 2I_B = I_A \quad (10)$$

$$i_{D3} = \frac{I_A}{1 + e^{(V_{GS4} - V_{GS3})/nV_T}} \quad (11)$$

$$i_{D4} = \frac{I_A}{1 + e^{(V_{GS3} - V_{GS4})/nV_T}} \quad (12)$$

From $i_{D1} = I_B + i_{D3}$,

$$\frac{I_A + 2I_B}{1 + e^{(V_{GS2} - V_{GS1})/nV_T}} = I_B + \frac{I_A}{1 + e^{(V_{GS4} - V_{GS3})/nV_T}} \quad (13)$$

to simplify the equation,

$$x \equiv e^{\frac{V_d}{nV_T}} \quad (14)$$

where $V_d = V_{GS1} - V_{GS2}$. The differential input voltage can expressed as $v_{id} = V_{GS1} - V_{GS2} + V_{GS4} - V_{GS3}$. Equation (13) can expressed as (15).

$$\frac{I_A + 2I_B}{1 + \frac{1}{x}} = I_B + \frac{I_A}{1 + e^{(v_{id})/nV_T}\frac{1}{x}} \quad (15)$$

In the same manner as above, $i_{D2} = I_B + i_{D4}$ can also be obtained as (16).

$$\frac{I_A + 2I_B}{1 + x} = I_B + \frac{I_A}{1 + \frac{x}{e^{(v_{id})/nV_T}}} \quad (16)$$

From (16), we can write the equation for x as (17).

$$I_B\,x^2 + (I_A + I_B)\left(e^{\frac{v_{id}}{nV_T}} - 1\right)x - I_B\,e^{\frac{v_{id}}{nV_T}} = 0 \tag{17}$$

The physically possible solution of (17) is found as (18).

$$x = \frac{-(I_A + I_B)\left(e^{\frac{v_{id}}{nV_T}} - 1\right) \pm \sqrt{((I_A + I_B)\left(e^{\frac{v_{id}}{nV_T}} - 1\right))^2 - 4I_B^2 e^{\frac{v_{id}}{nV_T}}}}{2I_B} \tag{18}$$

Equation (18) can be used to find the equations of i_{D1}, i_{D2}, i_{D3}, and i_{D4} by substituting into (15) and (16). Equation (18) is also used to prove the analysis and simulation results of the drain currents of transistors M_1 and M_2 in SPICE code.

– Positive feedback cell

$xm1\ 7\ 1\ 3\ mos1$
$xm2\ 8\ 2\ 4\ mos1$
$xm3\ 3\ 4\ 5\ mos3$
$xm4\ 4\ 3\ 5\ mos3$
$iba\ 5\ 0\ DC\ 20n$
$ib1\ 3\ 0\ DC\ 2n$
$ib2\ 4\ 0\ DC\ 2n$

– Analytical model for iD1, iD2, iD3, iD4, x

$.param\ IA = 20nA\ IB = 2nA$
$bi1\ 31\ 0\ i = (IA + 2 * IB)/(1 + 1/v(37))$
$bi2\ 32\ 0\ i = (IA + 2 * IB)/(1 + 1 * v(37))$
$bi3\ 33\ 0\ i = ia/(1 + v(35)/v(37))$
$bi4\ 34\ 0\ i = ia/(1 + v(37)/v(35))$
$bc1\ 35\ 0\ i = exp(v(1,2)/nVt)$
$bb1\ 36\ 0\ i = (v(35) - 1) * (IA + IB)$
$bx1\ 37\ 0\ i = (sqrt(v(36)^2 + 4 * I_B^2 * v(35)) - v(36))/2 * IB$

– nMOS D G S (subthreshold model)

$.subckt\ mos1\ 3\ 2\ 1$
$bid\ 3\ 1\ i = is1 * exp((v(2,1) - vt0)/nVt) * (1 - exp(-v(3,1)/Vt))$
$.ends$
$.subckt\ mos3\ 3\ 2\ 1$
$bid\ 3\ 1\ i = is3 * exp((v(2,1) - vt0)/nVt) * (1 - exp(-v(3,1)/Vt))$
$.ends$

Figure 2 is to check the transfer characteristics for two different values of I_B. These are the analysis and simulation results of the drain current i_{D1} and i_{D2} when I_B is 0 nA and the drain current i_{D1} and i_{D2} when I_B is 2 nA. The analysis results match the simulation results well. The effective transconductance G_m is determined by the slope of the transfer curve at $v_{id} = 0$, and as shown in Figure 2, as I_B increases, the effective transconductance decreases and the linear range increases. When I_B is 2 nA, the effective transconductance at $v_{id} = 0$ becomes 4 μS. It is observed that the effective transconductance at $v_{id} = 0$ is 40 mS when I_B is 0 nA. Although G_m has increased by more than 1,000 times, OTA operates like a comparator and becomes unstable. The differential output current i_{od1} of differential pair can be expressed as (19),

$$i_{od1} \equiv i_{D1} - i_{D2} = \frac{I_A + 2I_B(x-1)}{x+1} \tag{19}$$

To simplify the equation, substituting (14) into (19) can be obtained as,

$$(I_A + 2I_B)tanh\left[\frac{\frac{v_{id}}{2} - nV_T asinh\left(\frac{I_A + I_B}{I_B}\sinh\left(\frac{v_{id}}{2nV_T}\right)\right)}{2nV_T}\right.$$

We have proven that (10) in [24] is incorrect. The effective transconductance G_m at $v_{id} = 0$ can be found as (20),

$$G_m = \frac{\partial_{i_{od1}}}{\partial_{v_{id}}} = -\frac{I_A}{2nV_T}\,\frac{(I_A + 2I_B)}{2I_B} \tag{20}$$

using $I_A = 2i_{D3}$ and $I_B = i_{D1} - i_{D3}$, G_m can be also expressed as (21),

$$= -\frac{I_A}{2nV_T}\frac{1}{(1-\frac{I_{D3}}{I_{D1}})} \quad (21)$$

where $I_A/2nV_T$ is the effective transconductance of the input differential pair circuit. $1/(1 - I_{D3}/I_{D1})$ is the gain improved by configuring positive feedback on the input differential pair circuit.

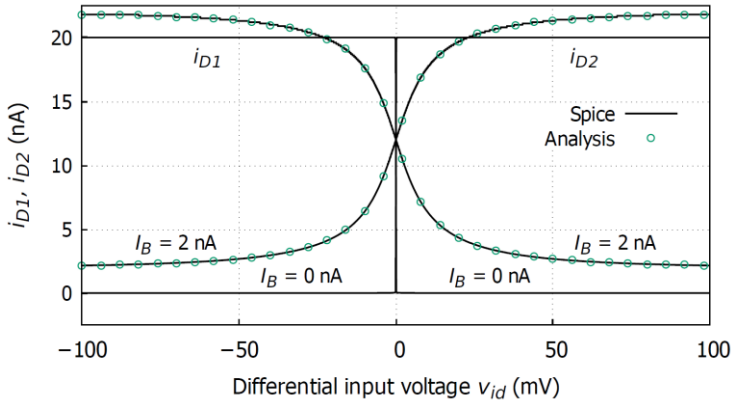

Figure 2. Simulation results for i_{D1} and i_{D2}: SPICE and analysis

2.2. Active loads with positive feedback

The drain current i_{D5} in weak inversion region can be expressed as (22),

$$i_{D5} = I_s\frac{W}{L}exp\left(\frac{v_{GS}-|V_t|}{nV_T}\right) = I_{s5}e^{(V_{GS5}-|V_t|)/nV_T} \quad (22)$$

where $I_{s5} \equiv I_s\ (W_5/L_5)$. The gates of M_5 and M_8 are connected to the same node.

$$i_{D8} = I_{s8}e^{(V_{GS8}-|V_t|)/nV_T} \quad (23)$$

$$i_{D5} = \left(\frac{I_{S5}}{I_{S8}}\right)i_{D8} \quad (24)$$

From $i_{D8} = i_{D2} - i_{D6}$,

$$I_{D5} = \left(\frac{I_{S5}}{I_{S8}}\right)(i_{D2} - i_{D6}) \quad (25)$$

The gates of M_6 and M_7 are connected to the same node.

$$i_{D6} = \left(\frac{I_{S6}}{I_{S7}}\right)i_{D7} \quad (26)$$

Substituting i_{D6} into (25).

$$i_{D5} = \left(\frac{I_{S5}}{I_{S8}}\right)(i_{D2} - \left(\frac{I_{S6}}{I_{S7}}\right)i_{D7}) \quad (27)$$

In the matching condition, I_{S5} is the same as I_{S6} and I_{S7} is the same as I_{S8}.

$$i_{D5} = \left(\frac{I_{S5}}{I_{S7}}\right)(i_{D2} - \left(\frac{I_{S5}}{I_{S7}}\right)i_{D7}) \quad (28)$$

Substituting i_{D5} obtained into $i_{D1} - i_{D7} = i_{D5}$.

$$i_{D1} - i_{D7} = \left(\frac{I_{S5}}{I_{S7}}\right)(i_{D2} - \left(\frac{I_{S5}}{I_{S7}}\right) i_{D7}) \quad (29)$$

Thus i_{D7} can be obtained as (30).

$$i_{D7} = \frac{[i_{D1} - \left(\frac{I_{S5}}{I_{S7}}\right) i_{D2}]}{1 - \left(\frac{I_{S5}}{I_{S7}}\right)^2} \quad (30)$$

In a similar process, i_{D8} can be found as (31).

$$i_{D8} = \frac{[i_{D2} - \left(\frac{I_{S5}}{I_{S7}}\right) i_{D1}]}{1 - \left(\frac{I_{S5}}{I_{S7}}\right)^2} \quad (31)$$

A SPICE code is used to prove that the analysis and simulation results for the drain current of transistors M_7 and M_8.

– Positive feedback cell

$xm1\ 7\ 1\ 3\ mos1$
$xm2\ 8\ 2\ 4\ mos1$
$xm3\ 3\ 4\ 5\ mos3$
$xm4\ 4\ 3\ 5\ mos3$
$xm5\ 9\ 10\ 6\ mos5$
$xm6\ 10\ 9\ 6\ mos5$
$xm7\ 11\ 9\ 6\ mos7$
$xm8\ 12\ 10\ 6\ mos7$
$iba\ 5\ 0\ DC\ 20n$
$ib1\ 3\ 0\ DC\ 2n$
$ib2\ 4\ 0\ DC\ 2n$

– Analytical model for iD1, iD2, iD3, iD4, x

$.param\ IA = 20nA\ IB = 2nA$
$bi1\ 31\ 0\ i = (IA + 2 * IB)/(1 + 1/v(37))$
$bi2\ 32\ 0\ i = (IA + 2 * IB)/(1 + 1 * v(37))$
$bi3\ 33\ 0\ i = IA/(1 + v(35)/v(37))$
$bi4\ 34\ 0\ i = IA/(1 + v(37)/v(35))$
$bc1\ 35\ 0\ i = exp(v(1,2)/nVt)$
$bb1\ 36\ 0\ i = (v(35) - 1) * ((ia + ib)/ib)$
$bx1\ 37\ 0\ i = (sqrt(v(36)^2 + 4 * v(35)) - v(36))/2$

– Analytical model for iD7, iD8

$bi5\ 38\ 0\ i = ((i(vm1)) - ((IS5/IS7) * (i(vm2))))/(1 - ((IS5/IS7)^2))$
$bi6\ 39\ 0\ i = ((i(vm2)) - ((IS6/IS8) * (i(vm1))))/(1 - ((IS6/IS8)^2))$

– nMOS D G S (subthreshold model)

$.subckt\ mos1\ 3\ 2\ 1$
$bid\ 3\ 1\ i = is1 * exp((v(2,1) - vt0)/nVt) * (1 - exp(-v(3,1)/Vt))$
$.ends$
$.subckt\ mos3\ 3\ 2\ 1$
$bid\ 3\ 1\ i = is3 * exp((v(2,1) - vt0)/nVt) * (1 - exp(-v(3,1)/Vt))$
$.ends$

– pMOS D G S (subthreshold model)

$.subckt\ mos5\ 3\ 2\ 1$
$bid\ 1\ 3\ i = is5 * exp((v(1,2) - vt0)/nVt) * (1 - exp(-v(1,3)/Vt))$
$.ends$
$.subckt\ mos7\ 3\ 2\ 1$
$bid\ 1\ 3\ i = is7 * exp((v(1,2) - vt0)/nVt) * (1 - exp(-v(1,3)/Vt))$
$.ends$

Figure 3 shows the analysis and simulation results of drain current i_{D7} and i_{D8}. The analysis results match well with the simulation results. The differential output current i_{od2} of active loads can be expressed as,

$$i_{od2} \equiv i_{D7} - i_{D8} = \frac{1}{1 - \left(\frac{i_{D5}}{i_{D7}}\right)}(i_{D1} - i_{D2}) \quad (32)$$

Substituting $i_{D1} - i_{D2}$ obtained in (19).

$$= \frac{1}{1-\left(\frac{i_{D5}}{i_{D7}}\right)}\left[(I_A + 2I_B)tanh\left[\frac{\frac{v_i}{2} - nV_T asinh\left(\frac{I_A+I_B}{I_B}\sinh\left(\frac{v_{id}}{2nV_T}\right)\right)}{2nV_T}\right]\right]$$

We proved that (14) in [24] is in error. When drain current i_{D5} and i_{D7} become equal, i_{od2} becomes infinite. In this case, DC gain increases significantly, but PM is observed to be negative. Also, when drain current i_{D5} is 0, i_{od2} and i_{od1} become equal and positive feedback does not work at active loads. Therefore, the current ratio i_{D5}/i_{D7} must be carefully selected and designed considering OTA stability.

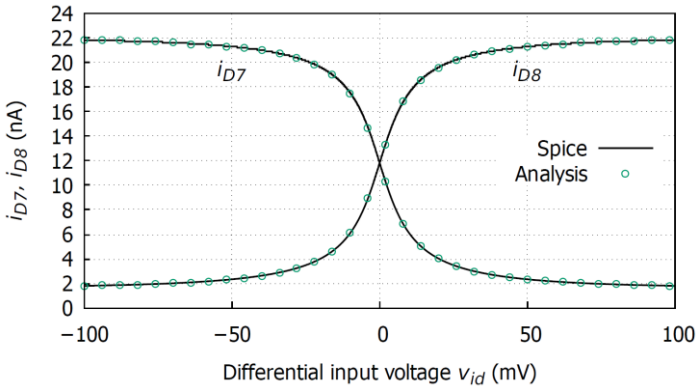

Figure 3. Simulation results for i_{D7} and i_{D8}: SPICE and analysis

2.3. The designed OTA

Figure 4 shows the designed OTA circuit diagram. The designed OTA operates in the weak inversion region and provides high DC gain without increasing power consumption. To improve DC gain, the designed OTA is configured with two positive feedbacks. One is an input differential pair with positive feedback, and the current ratio i_{D3}/i_{D1} is designed to be 0.8 to consider the stability. The other is an active load with positive feedback. In this case, the current ratio i_{D5}/i_{D7} was designed to be 0.7 considering the stability.

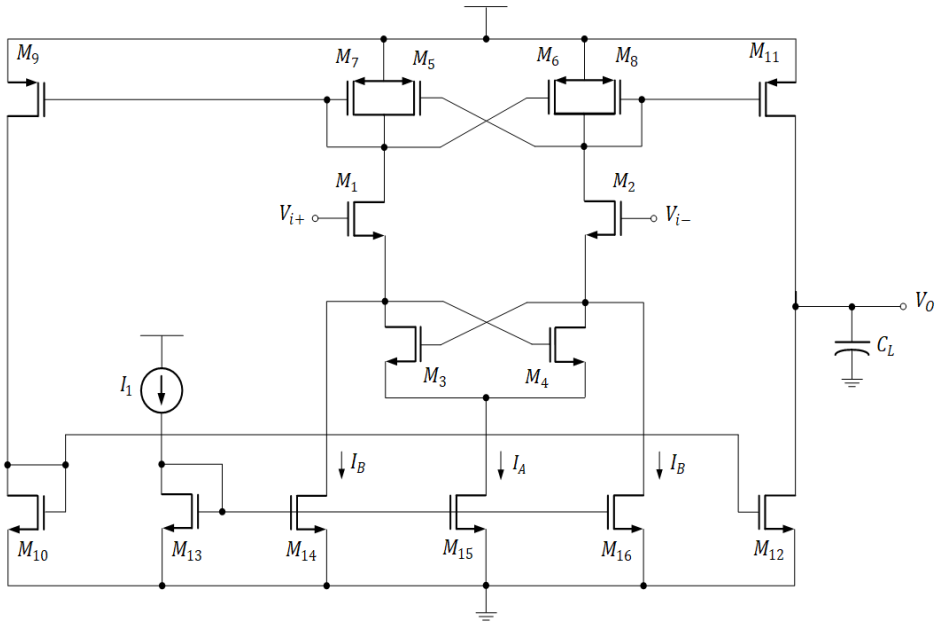

Figure 4. The designed OTA schematic

3. SIMULATION RESULTS

The designed OTA (with the current ratio $i_{D3}/i_{D1} = 0.8$, and $i_{D5}/i_{D7} = 0.7$, and the bias current $I_A = 20$ nA) operates at a power voltage of 1 V and a load capacitance of 15 pF, and a 0.18 µm complementary metal–oxide–semiconductor (CMOS) process was used to confirm the performance advantage. The characteristics of the frequency response can be seen in Figure 5, where the DC gain and gain bandwidth (GBW) of the existing OTA are 33 dB and 3.5 kHz, respectively, while the DC gain and GBW of the designed OTA are 68.5 dB and 23.1 kHz, respectively. As shown in Figure 5, the performance advantage is 2 times in DC gain and 6.6 times in GBW compared to the conventional OTA. The phase margin is 92° for the conventional OTA, whereas it is 66.8° for the designed OTA, but it is sufficient to ensure stable operation. Figure 6 is the result of small signal step response analysis and the square wave is applied to 50 mV at 3.3 kHz. The 1% rise settling time is 150 µs for the conventional OTA, but was shortened to 64 µs for the designed OTA. The designed OTA has a short settling time of 1%, indicating the improved transconductance. The designed OTA consists of two positive feedbacks, and in this case, the DC gain is improved by 2 times, but stability may be an issue. This stability is related to phase margin and requires verification of stability and performance due to device mismatch and process variation. This can be verified through Monte Carlo simulation. Table 2 shows the average and standard deviation for DC gain, GBW, and phase margin. Figure 7 also shows DC gain, GBW, and phase margin. These are the results of 2,000 samples from Monte Carlo simulation. It can be concluded that the designed OTA is robust through Monte Carlo simulations for device and process mismatch. All performance comparisons of the conventional OTA and the designed OTA are listed in Table 3.

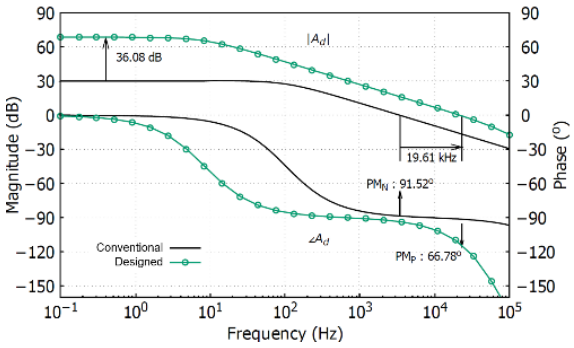

Figure 5. The result of frequency responses for the designed OTAs

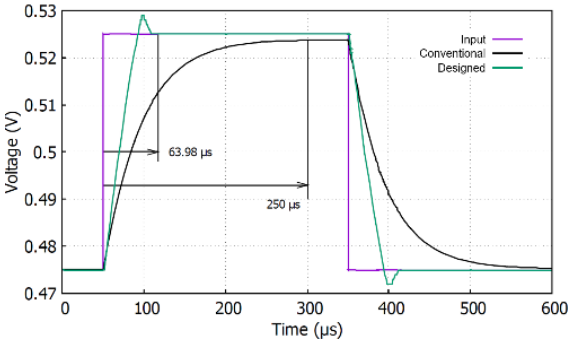

Figure 6. The result of step responses for the designed OTAs

Table 2. The Monte Carlo simulation

Typical Performances	Values
DC gain average μ_A	68 dB
DC gain standard deviation σ_A	1.9 dB
GBW average μ_G	21.9 kHz
GBW standard deviation σ_G	3 kHz
Phase margin average μ_p	67^o
Phase margin standard deviation σ_P	1.7^o

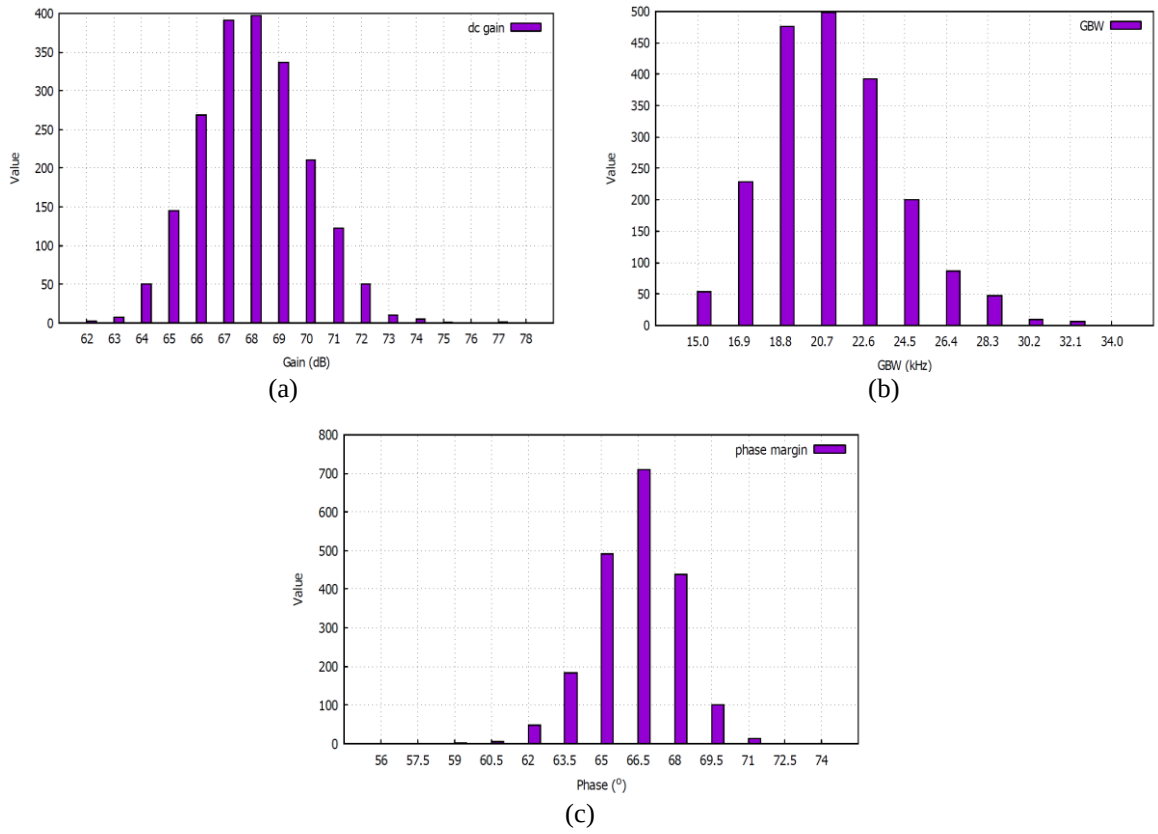

Figure 7. The result of Monte Carlo simulation for the designed OTA: DC gain, GBW, and phase margin

Table 3. The performance of the designed OTA

Parameter	Conventional OTA	Designed OTA
Technology	0.18 µm CMOS process	0.18 µm CMOS process
Power supply (V)	1	1
Power consumption (nW)	45.3	41.4
CL (pF)	15	15
DC gain (dB)	32.4	68.5
Phase margin (o)	92	66.8
GBW (kHz)	3.5	23.1
CMMR (dB)	72	82
SR + (V/ms)	0.3	1.2
SR - (V/ms)	-0.2	-1.2
1% settling time (µs)	150	64
Area (μm^2)	1420	1420
FOM (V^{-1})	1.1	8.5
Input-referred noise (nV/$\sqrt{Hz}$	1506@1 kHz	5,261 kHz

4. CONCLUSION

In this paper, we present one circuit analysis method for an input differential pair with positive feedback and an active load with positive feedback. The presented circuit analysis results match well with the simulation results. The designed OTA operates in the weak inversion region and provides high DC gain without significantly increasing power consumption compared to conventional OTA. The designed OTA technology can be usefully applied in OTA for low power applications.

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