Exploring distance-based wireless transceiver placements for wireless network-on-chip architecture with deterministic routing algorithms

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ABSTRACT

Network-on-chip (NoC) technology is crucial for integrating multiple embedded computing cores onto a single chip. Consequently, this has led to the development of the wireless network-on-chip (WiNoC) concept, seen as a promising strategy to overcome scalability issues in communication systems within chips for future many-core architectures. This research analyses the impact of wireless transceiver subnet clustering on the hundred-core mesh-structured WiNoC architecture. The study aims to examine the effects of distance-based wireless transceiver placements on the transmission delay, network throughput, and energy consumption within a mesh wireless NoC architecture featuring a hundred cores, under specific routing strategies: X-Y, west-first, negative-first, and north-last. This research investigates the impact of positioning radio subnets at the farthest, farther, nearest, and closest positions within an architecture equipped with four wireless transceivers. The Noxim simulator was utilised to simulate the analysed wireless transceiver placements within the hundred-core mesh-structured WiNoC designs, with the objective of validating the results. The architecture with the wireless transceivers positioned at midway proximity (nearer and further) demonstrated the best performance, as evidenced by the lowest latencies for all evaluated deterministic routing algorithms, according to the simulation outcomes.

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1. INTRODUCTION

In recent years, there has been a growing interest in using on-chip interconnect layouts for communication among chip multiprocessors, supported by various studies [1]–[5]. Advancements in the semiconductor industry have been pivotal in driving technological progress, enabling the integration of hundreds or more processing units into a single chip system. Numerous prototypes employing network-on-chip (NoC) designs with multiple cores have been developed and implemented in several works including SCORPIO [6], RAW [7], Xeon Phi [8], and TILERA [9]. The issue of wire delay becomes more significant in large on-chip networks, potentially severely impacting network performance. The traditional wired NoC architecture struggles under the increasing number of computing cores, due to its dependence on long-distance communication that requires multiple hops, leading to designs that consume more power and experience higher latency. Consequently, to mitigate the challenges associated with significant signal delay and the necessity for long distance communication between processing units, computer architects or researchers are converging on the promise of wireless NoC connections as a feasible alternative [10]–[13].

The primary challenge addressed in this study is to investigate and optimise the placement of wireless transceivers within a wireless NoC architecture, particularly in systems employing deterministic routing algorithms. The study aims to determine how varying distances between transceivers, as well as their strategic positioning, can significantly influence key performance indicators such as latency, throughput, energy efficiency, and wireless utilisation. This investigation is critical for advancing the design and efficiency of multicore and many-core systems, where optimal wireless communication pathways are crucial for enhanced WiNoC performance.

The structure of the paper is as follows: beginning with section 2, it includes an outline of the hundred core mesh-structured WiNoC network structure, and the description of deterministic routing mechanism. Section 3 offers a detailed account of the methodological framework used in the Noxim simulation setup. Following this, section 4 engages in an examination of the experimental results and their analysis. Finally, section 5 concludes the paper and suggests directions for future research.

2. MESH-STRUCTURED WIRELESS NOC WITH HUNDRED-CORE

2.1. Mesh-structured WiNoC architecture

WiNoC introduces wireless communication links into the NoC architecture, aiming to overcome the limitations of wired connections. By using wireless links for long-distance communication across the chip, WiNoCs can reduce latency and power consumption compared to their entirely wired counterparts [14] . These wireless connections are typically established through on-chip antennas and transceivers that support high-frequency radio waves or other electromagnetic signals [15]–[18]. Additionally, the emergence of integrated wireless transceiver [19], [20] and millimetre-wave CMOS-compatible antennas [21], [22] has highlighted the possibility of WiNoC as a viable alternative to traditional NoC designs [23]. The configuration of component interconnections in a WiNoC that has a substantial impact on both the performance of the network and the associated architectural expenses. Consequently, it is a crucial matter that must be taken into account during the design process. The architectural design of a WiNoC infrastructure is affected by numerous aspects, such as the physical arrangement, interconnections between processors, the quantity of wireless channels, and the distribution of wireless transceivers throughout the WiNoC system [24]–[26]. The diagram shown in Figure 1 depicts a mesh-structured WiNoC topological design. It consists of a 10×10 grid layout with hundred cores and four wireless transceivers spread over the Mesh-structured WiNoC architecture. The integration of wireless transceivers into the NoC tiles facilitates direct connection between the processor cores that are spatially distant from each other, hence enabling wireless single-hop communication.

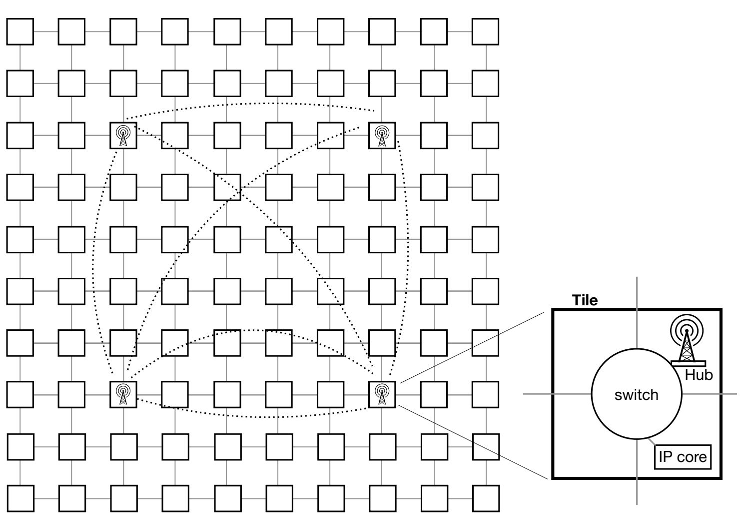

Figure 1. Hundred cores mesh-structured wireless NoC design with four wireless transceiver

2.2. Routing algorithm with deterministic approach

In chemical-mechanical polishing (CMP) applications where buffering resources are limited due to strict latency requirements, a deterministic routing scheme is a preferred strategy. This routing scheme, based on wormhole routing, involves fragmenting packets into flow control digits (flits). Each flit within the packet contains the necessary routing information for navigation through the WiNoC network, embedded in its header. During instances of network congestion that halt the progress of a flit's header, all flits that follow must remain at their starting tile nodes until the congestion is alleviated. The mesh-based structure is highly suitable for deterministic routing approach as it enables the establishment of the minimum distance feasible pathway between transmitting computing cores. Moreover, this technique eliminates the need for tables and ensures prevention of deadlock and live-lock issues throughout the chip network [27]–[30] .

Figure 2(a) demonstrates the possible directions available in X-Y routing. The solid lines represent valid directions that can be taken, while the dashed lines indicate prohibited turns. For instance, using the XY routing method, a packet can be initially routed in the X-direction, followed by the Y-direction, to arrived its intended processing core. As shown in Figure 2(b), the west-first routing algorithm prioritises routing a packet in the west orientation first, if it is a effective orientation, while allowing for the selection of any shortest path if the west direction is not viable. In the negative-first routing scheme as shown in Figure 2(c), if the destination of a data packet lies in any negative-axis direction (either vertical or horizontal) along with another orientation, the packet is initially directed in the direction of the negative-axis orientation and subsequently towards the other direction. Finally, Figure 2(d) shows the north-last routing scheme required that when traffic is heading towards the north, the north direction should be chosen as the last option, while allowing for all possible shortest paths when traffic is headed south. However, for traffic going north, only a single path is permitted.

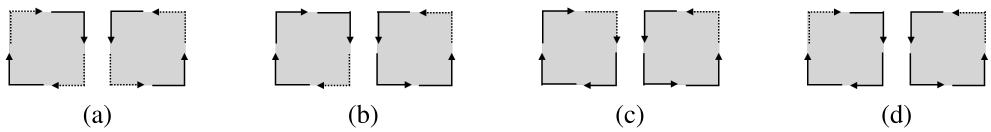

Figure 2. The possible directions for turns in deterministic routing (a) X-Y, (b) west-first, (c) negative-first, and (d) north-last

3. METHODOLOGICAL SIMULATION

The performance of the explored wireless transceiver emplacement based on distance has been evaluated on the hundred cores mesh-structured wireless NoC topology using the well-known network-on-chip simulator, Noxim [31]. By using a deterministic wormhole-based routing method, mesh-WiNoC topologies may provide wireless transmission through the Noxim simulator. In order to model various wireless transceiver placement designs into wireless NoC infrastructure, Noxim was also built to provide placement configuration adaptation. This Noxim simulator effectively captures the latency involved in routing path and crossbar arbitration selection by employing real data derived from the design of a real prototype router. This approach ensures the simulation results closely real performance, providing valuable insights for optimising CMP architectures.

Table 1 displays the simulation setup parameters that were employed in this study. Four different wireless transceiver placement configurations such as furthest, farther, nearer, and nearest were used in the simulations, as shown in Figure 3(a), 3(b), 3(c), and 3(d) respectively. The use of various routing algorithms—X-Y, west-first, negative-first, and north-last—suggests a comprehensive study into the efficiency and effectiveness of different routing methodologies under the same network conditions. By employing multiple algorithms, the experiment can provide insights into which routing strategy performs best in a WiNoC environment with the given configuration. The selection behind these routing offers several advantages, including deadlock avoidance, as it is specifically designed to prevent the formation of cyclic dependencies, which greatly enhances the reliability of the network. Additionally, this model boasts simplicity, as the routing decisions it requires are relatively straightforward to implement, particularly in hardware contexts. Furthermore, its deterministic nature contributes to predictable performance, ensuring a consistent and reliable operation within the network system. Every simulation in the placement on the investigated WiNoC architecture was performed a total of 100,000 times to get a state that was stable. Random traffic distributions were used in the simulation, giving each processing unit an equivalent chance of sending a packet of information to any other processing core.

Table 1. Noxim simulation setup

Specification	Details
Clock frequency	1 GHz
IP cores	100
Technology	65 nm
Wireless transceiver	4
Emplacement	Nearest, Nearer, Further, Furthest
Simulation time	100,000 cycles
Wireless data rate	16 Gbps
Routing algorithm	X-Y, west-first, negative-first, north-last

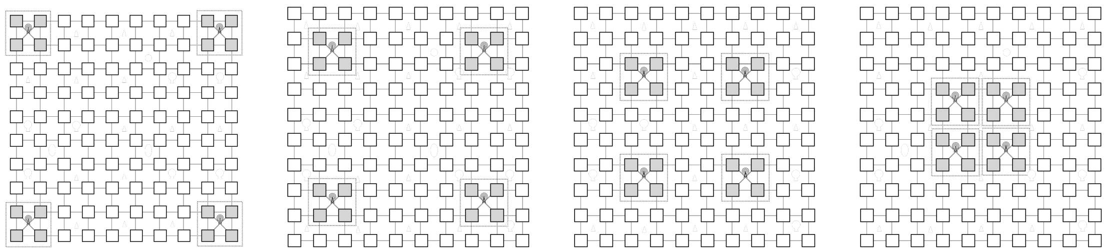
(a) (b) (c) (d)

Figure 3. The 100-cores wireless NoC architecture with varying distances between transceiver placements (a) furthest, (b) further, (c) nearer, and (d) nearest

4. RESULTS AND ANALYSIS

This section evaluates the performance of a hundred-cores mesh structured WiNoC architecture with four wireless transceiver placements, taking random distribution workload into account. The effectiveness of the investigated system is evaluated using measurements of performance including network throughput and communication delay. These metrics are frequently employed for evaluating and illustrating the performance of the on-chip WiNoC system. Moreover, the study was conducted on the wireless usage and energy consumption of several WiNoC designs with varied wireless transceiver positions according to the proximity of distance.

4.1. The effect of network latency

Latency is the aggregate count in clock cycles necessary for a data packet to traverse the WiNoC network, originating from its source and reaching its designated destination. Figure 4 illustrates the effect of latency on wireless transceiver placement, considering numerous routing algorithms, namely X-Y in Figure 4(a), west-first in Figure 4(b), negative-first in Figure 4(c), and north-last in Figure 4(d). Meanwhile, Table 2 summarises the average latency at saturation PIR in cycles at the saturation workload attained in this simulation for the furthest, further, nearer, and nearest placements under various routing algorithms. The graph illustrates the relationship between the injected packet load and the accompanying latency. The presented graphs exhibit a variety of delay values, each characterised by a distinct curvature. The delay experiences a consistent increase as the packet injection rate or in short, PIR of the given workload increasing. Nevertheless, when subjected to greater loads, the latency experiences an apparent rise in the presence of PIR, indicating that the WiNoC system has established a state of saturation. In general, the wireless transceivers in all examined placements exhibit saturation at comparable points of PIR saturation: 0.013 (X-Y), 0.011 (west-first), 0.010 (negative-first), and 0.011 (north-last) flit/cycle/tile. However, the placement located in the middle demonstrates better results in terms of latency. Specifically, it requires 68 cycles for X-Y routing and 46 cycles for west-first routing. It is noteworthy that the placement at a greater distance exhibits the lowest delay, as evidenced by 43 cycles for negative-first routing and 53 cycles for north-last routing.

4.2. The effect of the throughput saturation

The term network throughput is used to describe the speed at which data packets move across the WiNoC system. Moreover, throughput saturation defines the specific point where the network's capacity is fully utilized, aligning the throughput with the demands of the workload. At this saturation point, the WiNoC system becomes less effective in handling the transmission of the data packets it produces. Figure 5 illustrates the impact of WiNoC throughput on diverse wireless transceiver placements, including several routing algorithms such as X-Y in Figure 5(a), west-first in Figure 5(b), negative-first in Figure 5(c), and north-last in Figure 5(d). Meanwhile, Table 3 shows the network throughput at PIR saturation in flits/cycle attained in this simulation for the furthest, further, nearer, and nearest placements under various routing algorithms. The figure shows how the throughput of the WiNoC system changes as the packet injection rate (PIR) progressively increases. For closer placements of the wireless transceivers, the saturation throughput levels are 10.35 flits per cycle for the X-Y routing algorithm and 8.81 flits per cycle for the west-first routing algorithm. Additionally, for the farthest wireless transceiver placement, the saturated network throughput rates are 7.99 flits per cycle for the negative-first routing algorithm and 8.80 flits per cycle for the north-last routing algorithm.

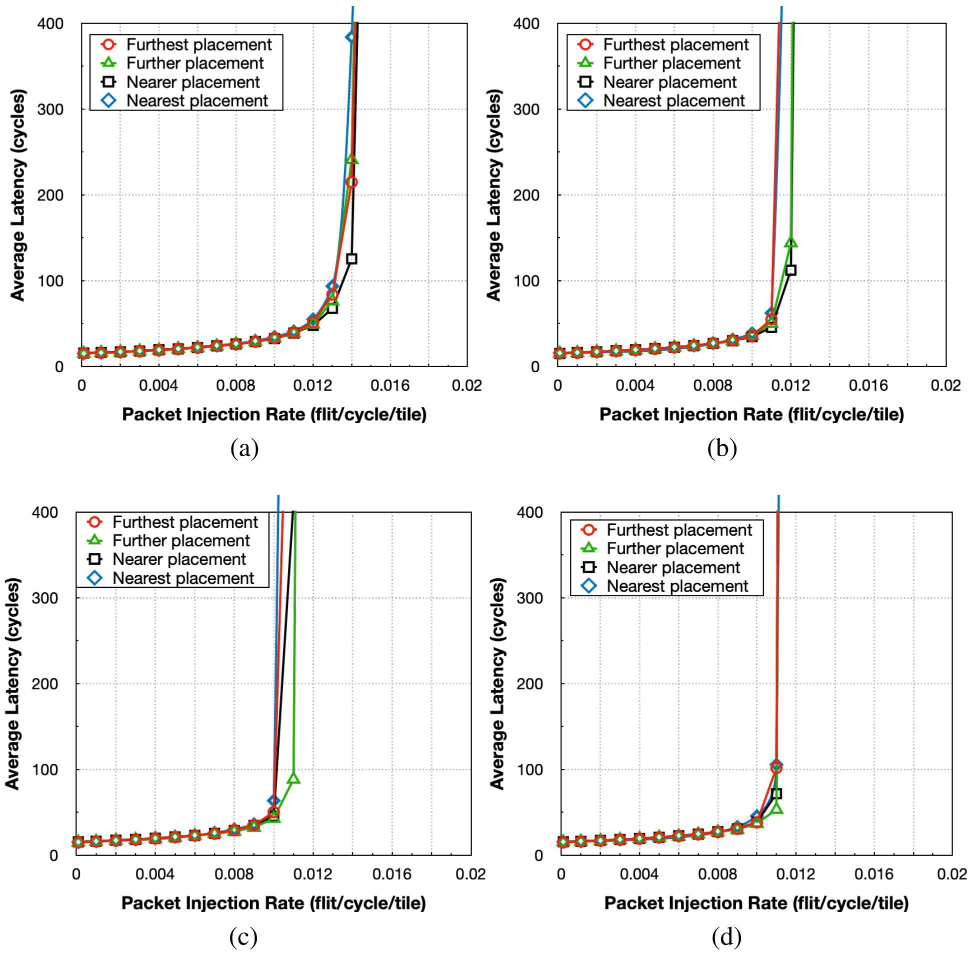

Figure 4. The effects of the network latency for varying wireless transceiver placements under various deterministic routing algorithm (a) X-Y, (b) west-first, (c) negative-first, and (d) north-last

Table 2. Average latency at saturation load under various deterministic routing algorithms

Routing Algorithm	Average latency (cycles)			
	Furthest	Further	Nearer	Nearest
X-Y	84	76	68	93
West-First	55	50	46	62
Negative-First	50	43	45	64
North-Last	102	53	72	106

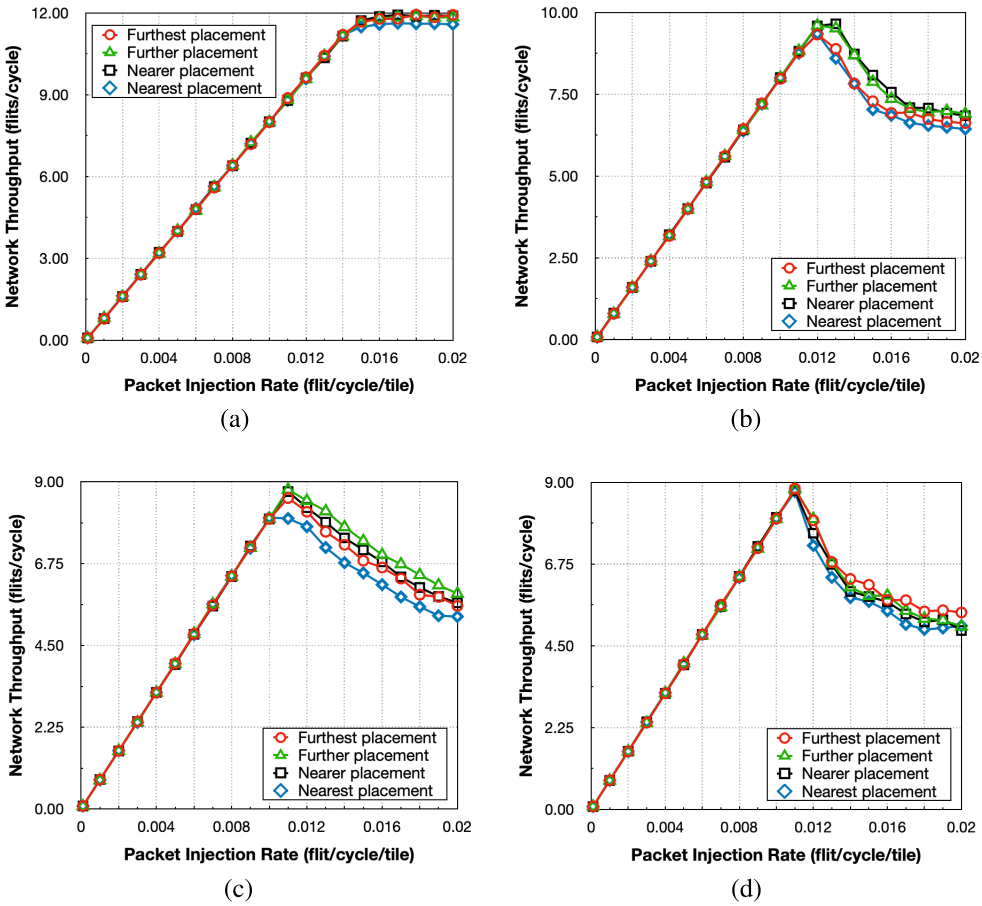

Figure 5. The effects on throughput for different wireless transceiver placements under varying deterministic routing (a) X-Y, (b) west-first, (c) negative-first, and(d) north-last

Table 3. Throughput at saturation load under various deterministic routing algorithms

Routing Algorithm	Network throughput (flits/cycle)			
	Furthest	Further	Nearer	Nearest
X-Y	10.43	10.42	10.35	10.41
West-First	8.77	8.83	8.81	8.76
Negative-First	7.98	7.99	7.98	8.01
North-Last	8.82	8.80	8.77	8.75

4.3. The effect of energy consumption

Energy consumption in WiNoC systems is a critical factor that impacts their design and performance.Energy consumption in WiNoC system refers to the amount of electrical power these processors use during their operation. Figure 6 illustrates how energy use in WiNoC is affected, highlighting how the positioning of wireless transceivers influences power consumption in conjunction with different routing algorithms such as X-Y in Figure 6(a), west-first in Figure 6(b), negative-first in Figure 6(c), and north-last in Figure 6(d). This information is derived from simulations run on Noxim. Meanwhile, Table 4 shows the network energy utilization at the load saturation attained in this simulation for the furthest, further, nearer, and nearest placements under various routing algorithms. Regarding energy usage, when the wireless transceiver is placed close to the source, it results in energy consumption values of 1.67×10^{-4} J for the X-Y routing strategy, and 1.77×10^{-4} J for the West-First routing approach. Moreover, for negative-first and north-last routing, the energy consumption is 1.65×10^{-4} J and 1.67×10^{-4} J accordingly, with the further placement of the wireless transceiver.

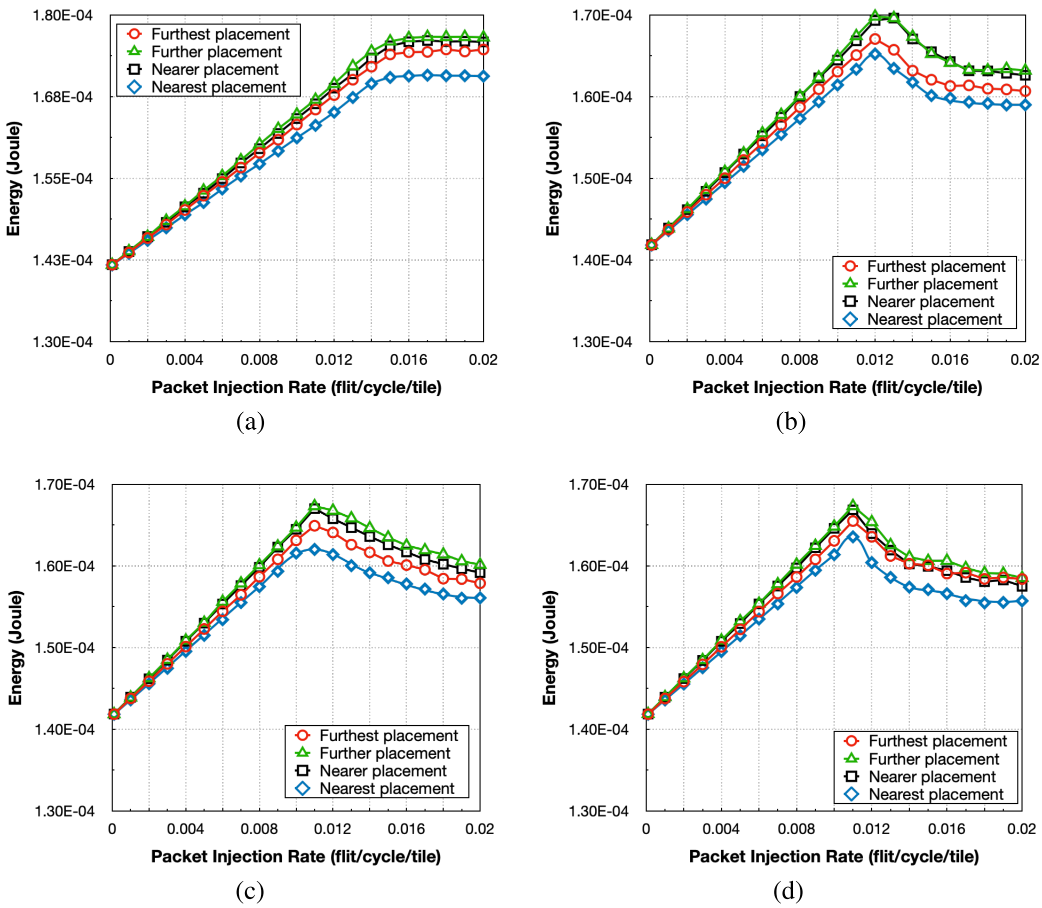

Figure 6. The effects of the energy consumptions for varying wireless transceiver placement for various deterministic routing algorithm (a) X-Y, (b) west-first, (c) negative-first, and (d) north-last

Table 4. Energy consumption at saturation load under various deterministic routing algorithms

Routing	Energy consumption ($\times 10^{-4}$ Joule)			
Algorithm	Furthest	Further	Nearer	Nearest
X-Y	1.70	1.72	1.71	1.67
West-First	1.65	1.67	1.67	1.63
Negative-First	1.63	1.65	1.64	1.62
North-Last	1.65	1.67	1.67	1.64

5. CONCLUSION

The objective of this research was to explore the implications of distance proximity of the wireless transceiver placements (specifically nearest, nearest, further, and furthest, further proximity) on the 100 cores mesh wireless NoC framework, utilising deterministic routing algorithms. The findings from the simulation suggest that positioning the wireless transceiver at an intermediate distance, either nearer or further, within the architecture results in the best performance and the least latency for deterministic the routing algorithms tested. Positioning the wireless transceiver closer offers optimal performance in both X-Y and west-first routing. On the other hand, the routing algorithms that show a preference for the further placement of the wireless transceiver include negative-first and north-last. Subsequent studies intend to delve into the effects of dynamic and adaptive routing using multiple channels for wireless transmissions on the WiNoC multicore framework, especially employing the increment count of wireless transceivers.

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