

An 8-bit successive-approximation register analog-to-digital converter operating at 125 kS/s with enhanced comparator in 180 nm CMOS technology

Fadi Nessir Zghoul¹, Yousra Hussein Al-Bakrawi¹, Issa Etier², Nithiyananthan Kannan³

¹Electrical Engineering Department, Jordan University of Science and Technology, Irbid, Jordan

²Department of Electrical Engineering, Faculty of Engineering, The Hashemite University, Zarqa, Jordan

³Department of Electrical Engineering, Faculty of Engineering, King Abdulaziz University, Rabigh, Kingdom of Saudi Arabia

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ABSTRACT

Data converters are necessary for the conversion process of analog and digital signals. Successive approximation register (SAR) analog-to-digital converters (ADC) can achieve high levels of accuracy while consuming relatively low amounts of power and operating at relatively high speeds. This paper describes a design of 8-bit 125 kS/s SAR ADC with a proposed high-speed comparator design based on dynamic latch architecture. The proposed design of the comparator enhances the performance compared to a conventional dynamic comparator by adding two parallel clocked input complementary metal-oxide semiconductor (CMOS) transistors which reduce the parasitic resistance in the latch ground path and serve to minimize the latch delay time. The design of each sub-system for the ADC is explained thoroughly, which contains a sample and hold circuit, successive approximation register, charge redistribution types digital-to-analog converter, and the new proposed comparator. The proposed design is implemented using 180 nm CMOS technology with a power supply of 1.2 V. The average inaccuracy in differential non-linearity (DNL) is +0.6/-0.8 LSB (least significant bit), and integral non-linearity (INL) is +0.4/-0.7 LSB. The proposed design exhibits a delay time of 157 ps at 1 MHz clock frequency.

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Corresponding Author:

Fadi Nessir Zghoul

Electrical Engineering Department, Jordan University of Science and Technology

Irbid 22110, Jordan

Email: FRNessirZghoul@just.edu.jo

1. INTRODUCTION

The growth in digital computing and digital signal processing has led to an increasing trend of storing, processing, and communicating information in the digital domain. To convert analog signals to digital ones, an analog-to-digital converter (ADC) is essential. ADCs with their counterparts, digital-to-analog converters (DACs) are critical building blocks in many applications. Digital circuits are less sensitive to noise and exhibit more robustness to variations in process and supply voltages, allowing for easier test automation compared to analog circuits [1]. There is a wide range of ADCs available with different specifications and features that cater to diverse application requirements. As a result, there is a constant need for the development of improved ADC models that offer better performance to meet the evolving application needs [2]–[5]. ADC integrated circuits are primarily evaluated based on their speed, power consumption, and accuracy. The sampling rate and resolution are two of the most important parameters used to measure the

accuracy of ADC. The advancement of ADC research focuses on improving the overall performance by enhancing the structure, refining the critical circuit design, and exploring digital calibration technology [6]–[11]. Among various types of ADCs, successive approximation register (SAR) ADC is a crucial component of any digital system that interfaces with the physical world. The ADC converts continuous analog signals into digital forms that can be processed by digital circuits. In low-power and low-speed applications, the SAR ADC architecture is a popular choice. It operates by approximating the analog input signal in successive comparison cycles, with each cycle refining the approximation until a digital output is obtained. In contrast to SAR ADCs, two-step ADCs, and flash ADCs are favorable for high-speed, low-resolution applications [12], [13]. Pipeline ADCs are commonly used in wireless network applications because they have medium sampling rates and resolutions. However, pipeline ADCs require several operational amplifiers, which can result in high power dissipation and a bulky design [14]. Another type of ADC that has been widely used is the time-interleaved analog-to-digital converter. Time-interleaved converters usually suffer due to timing mismatch in high frequency, recent work has been done to resolve this issue [15]. Σ - Δ ADCs have been also used in many applications such as electrocardiogram (ECG) signals. Their inherent complexity and higher power consumption compared to SAR ADCs make them less suitable. Recent work has been done to improve Σ - Δ ADCs, especially for ECG signal applications [16]. With the progress in technology, SAR ADC architecture has become an efficient solution for some high-speed conversion rate applications that need small areas and consume low power [17], [18]. The SAR ADC comprises a successive approximation register, control logic circuit, sample/hold circuit where much work has been conducted to improve its accuracy [19], DAC, and comparator.

This paper addresses the challenge of optimizing successive approximation register analog-to-digital converter (SAR ADC) performance. The central problem lies in the need to enhance the precision and efficiency of SAR ADCs, with a specific focus on minimizing integral non-linearity (INL) and differential non-linearity (DNL). The primary concern is the impact of the comparator's precision, speed, and noise characteristics on overall ADC performance. This study aims to innovate in the realm of SAR ADCs by introducing a novel dynamic comparator design, intending to improve speed, reduce time delays, and ultimately enhance the ADC's linearity and efficiency.

Research efforts have been dedicated to enhancing the performance of SAR ADCs. In study [20] the authors adopted a detect-and-skip switching scheme which helps improve linearity by avoiding unnecessary comparisons during the conversion process and enhances the speed. The speed-enhanced technique, and careful design choices led to improved INL and DNL characteristics in the low-power SAR ADC. The work in [20] where the hybrid architecture combining voltage-to-time conversion and time-to-digital converter (TDC) introduces additional complexity and requires calibration to achieve high linearity. Moving to [21], the focus was on refining INL and DNL through two techniques: a speed-enhanced SAR logic and a high-linearity capacitor digital-to-analog converter (CDAC). The speed-enhanced SAR logic reduces the conversion time by allowing the comparator to start the next comparison before the CDAC settles. The high-linearity CDAC employs a binary-weighted array with a split-capacitor technique to minimize the capacitor mismatch and parasitic effects. The split-capacitor technique used in [21] introduces additional parasitic capacitance and routing complexity. Additional parasitic capacitance and routing complexity degrades the linearity and speed of the CDAC.

Vafaei *et al.* [22] aimed to minimize variations in charge redistribution during the conversion process. This optimization contributes to reducing INL and DNL errors. On the other hand, this leads to minimizing the sampling rate. Others have used a bypass-switching scheme to reduce the INL and DNL. The bypass-switching scheme reduces the parasitic capacitance of the capacitor array [23]. The scheme bypasses the unnecessary switching operations and reduces the offset voltage and the noise of the comparator. The input common-mode voltage and the reference voltage are dynamically adjusted. The bypass-switching scheme requires a large number of switches and a complex control logic which may increase the complexity of the ADC. It also introduces a feedback loop that may affect the stability of the comparator. In study [24], a background mismatch calibration technique utilized a digital error correction algorithm to estimate and compensate the capacitor mismatch errors in the DAC array. The noise-reduction technique uses a dynamic element matching (DEM) scheme to randomize the noise and reduce its impact on the ADC INL and DNL. The circuit in [24] requires an extra bit trial in each conversion cycle which increases the conversion time and power consumption.

The solution proposed in this work centers around the development of a novel dynamic comparator design. By focusing on the precision, speed, and noise characteristics of the comparator we aim to enhance the overall performance of SAR ADCs. The innovation seeks to improve the speed of the comparator thereby reducing time delays and contributing to the minimization of INL and DNL. Through this novel design we anticipate achieving a higher level of accuracy and efficiency in SAR ADCs. The comparator's precision, speed, and noise characteristics significantly impact overall SAR ADC performance and improving the comparator enhances resolution, linearity, and conversion rate [25]–[29]. In response to the escalating

demand for efficient analog-to-digital converters (ADCs), this paper addresses the challenge of enhancing SAR ADC performance. Our innovation centers around a novel dynamic comparator design, aiming to improve speed, time delay, and power efficiency within the SAR ADC architecture. In section 2, we provide an overview of the SAR ADC architecture and introduce the novel dynamic comparator. Section 3 delves into the results, discussion, implementation effects, and SAR ADC layout. The study is summarized and concluded in section 4.

2. METHOD

The circuit shown in Figure 1 illustrates the fundamental structure of a successive approximation ADC. A sample/hold circuit sampled and held steady initially the analog input signal throughout the conversion. The SAR logic and control circuit executes the successive approximation algorithm and governs the conversion's timing and sequence. At the core of the converter, the comparator evaluates the input signal against reference voltages produced by the DAC circuit [30], [31].

The successive approximation converts the analog input signal to a digital output using the binary search algorithm. The working algorithm is briefly discussed here. At the start of the conversion, the most significant bit (MSB) is set to high as a guess, and all the remaining bits in the SAR are reset to zero. The digital value in the SAR is converted into an analog voltage by the DAC. This resulting voltage is compared with the actual analog input voltage using a comparator. If the DAC output is greater than the actual input voltage, the bit is set back to low, otherwise, the bit is maintained high. Then the next bit in the SAR is set to high (MSB-1), and the previous steps are repeated for this bit. This process continues sequentially for all the bits until the LSB is set. Finally, the control circuit generates the digital output code based on the values of the DAC outputs. Therefore, 'N' clock cycles are required for an N-bit ADC [32].

The complete schematic captured from the simulator for the 8-bit SAR ADC based on the proposed comparator is shown in Figure 2 SAR's sub-modules are all implemented in 180 nm technology. The array for the 8-bit binary weighted capacitive contains capacitors with values starting from 100 fF and increasing in powers of two until reaching 12.8 pF. The array's overall capacitance is 25.6 pF. The switches were implemented using N-channel metal-oxide-semiconductor (NMOS) and P-channel metal-oxide-semiconductor (PMOS) devices to configure a transmission gate. NMOS switches can pass a zero whereas PMOS switches can properly pass a strong one. The complementary metal-oxide semiconductor (CMOS) transmission gate combines the abilities of both NMOS and PMOS switches and is therefore capable of properly passing both zero and one. The inputs to one transmission gate are V_{ref} and ground. These switches control the connection of each bottom plate of the capacitor to either reference voltage or ground based on the desired binary representation.

The digital circuits in the SAR control logic employ the self-timing method to reduce delays, ensuring ample time for analog signals to stabilize within the DAC capacitor array and preamplifiers. For low power purposes and having pulses with a width equal to half a clock cycle in the simulation for the SAR logic circuit, the flip-flop's structure is employed with a combinational logic of XOR/AND gates, where the outputs of the flip-flops in the sequencer are the inputs of the XOR gate, then the output of it is the input of an AND gate with the CLK signal. Its output will be the settable pin for the code register as shown in Figure 3.

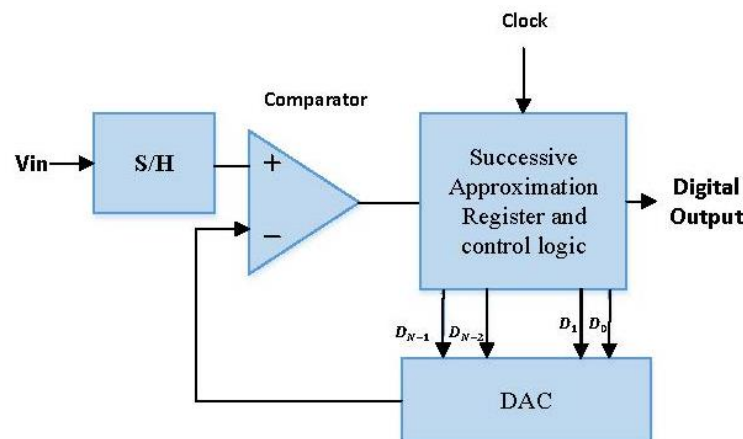


Figure 1. The conventional SAR logic

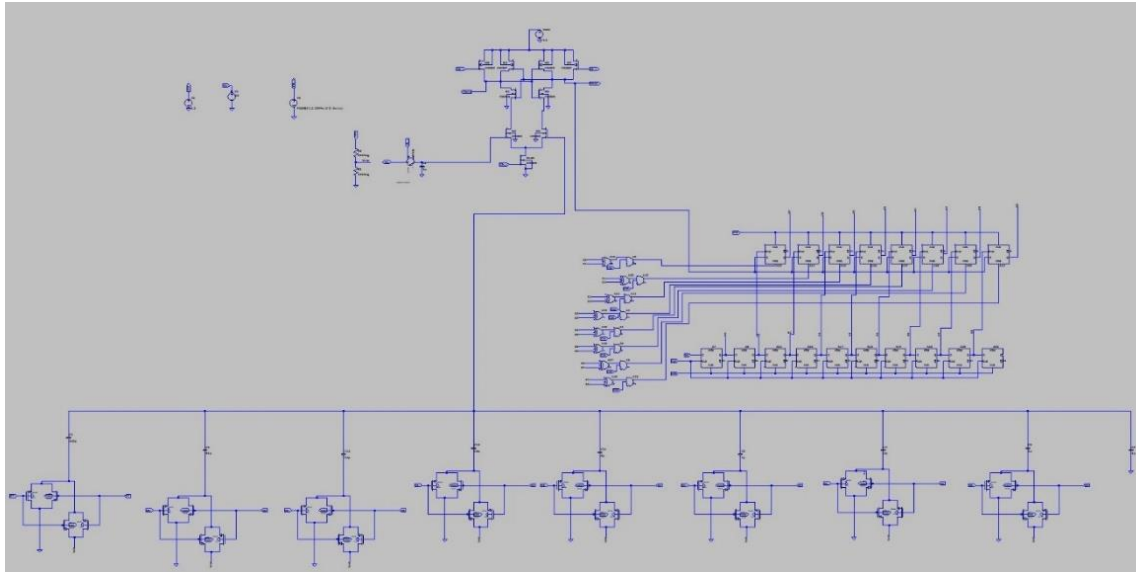


Figure 2. Schematic of SAR ADC module

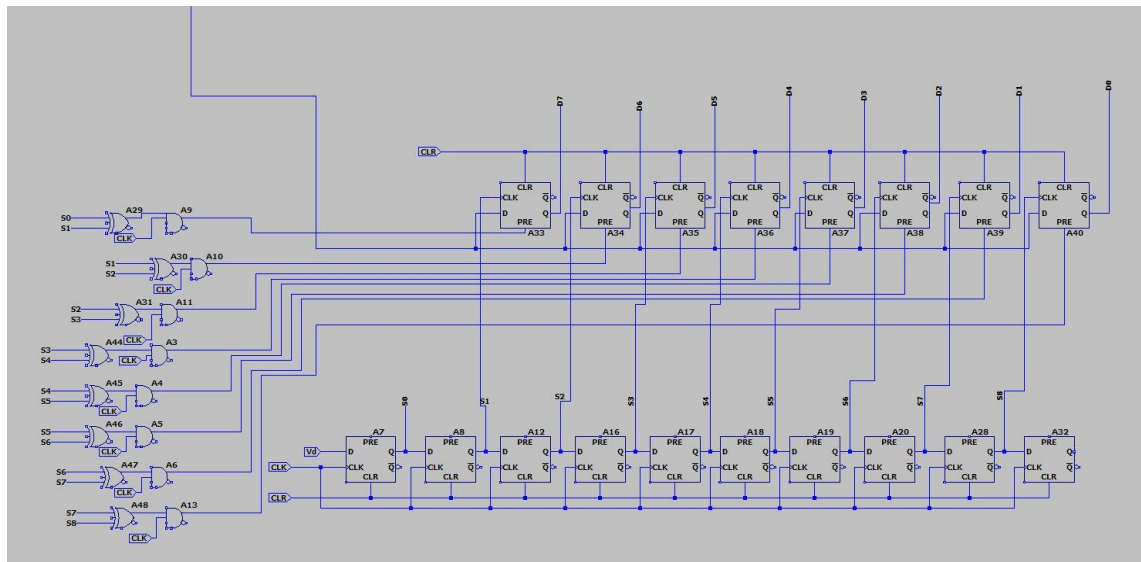


Figure 3. Digital control circuit for 8-bit SAR ADC

The output of the proposed SAR logic shows almost the same switching activity as the conventional digital control circuit but with a width equal to half a clock cycle for the pulses in the conversion phase, by avoiding the unwanted glitches in the pulse waveforms and that offers several advantages mainly by reducing power consumption. The active time of the circuit is decreased by narrowing the pulses resulting in lower power consumption. This is due to the fact that power is primarily consumed during transitions and active signal switching. The half-cycle width allows more accurate synchronization of the signals and ensures accurate timing between different parts of the circuit.

2.1. SAR ADC design and key components

This sub-section discusses in detail the SAR ADC design elucidating key components that collectively contribute to the circuit's overall performance. A thorough understanding of each element is imperative for unlocking the full potential of the ADC. By dissecting each component's role within the SAR ADC architecture, we aim to provide insights into the innovative design choices and methodologies that underpin our pursuit of an advanced 8-bit SAR ADC operating at 125 kS/s.

2.2. Sample/hold circuit

The sample and hold circuit are used to capture and hold the analog voltage signal for a brief period. In this brief period the analog signal is converted into a digital signal. The architecture shown in Figure 4 typically consists of a simple transmission gate (TG). The transmission gate works as a switch and a capacitor. The transmission gate is used to sample the analog signal and charge the capacitor to the sampled voltage level while the capacitor is used to hold the voltage level during the conversion process [33]. Simulations were used to determine the optimal sizes for the capacitor and transistors for the sampler to achieve the fastest switching speed and best holding time.

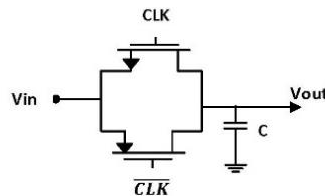


Figure 4. Sample and hold architecture

2.3. SAR control logic circuit

An asynchronous logic controller is chosen for the design of SAR ADC to preserve power and enhance the conversion speed, since the SAR logic controller can operate based on the arrival of input signals, and can potentially operate faster and with lower power consumption than a synchronous logic controller. Figure 5 outlines the block diagram of the asynchronous control logic circuit, which includes a sequencer and a set of bit registers. The sequencer of an 8-bit SAR logic controller made of shift registers consists of 10 D flip-flops that generate a sequence of pulses or rising edges that control the timing of the SAR ADC operation. The code register includes 8 flip-flops that receive the comparator's output consecutively, with each register determining a bit of the digital output [34]–[36]. The shift register is initially loaded with a digital value of all zeros. The SAR logic controller starts the conversion, where the MSB of the code register is set to one, which is then used to generate an analog voltage via a DAC. A comparison occurs between the resulting analog voltage and the input voltage, and the comparator's output guides the SAR logic controller. When the input voltage exceeds the DAC output, the MSB remains at one, and the next bit is set likewise. If the input voltage is lower than the DAC output, the MSB resets to zero, and the next bit is set to one. This procedure repeats until all bits in the code register are tested, yielding the final digital value. After completing the digitization, the sequencer and the registers are cleared for the next cycle. This iterative process applies to each sample needing digitization.

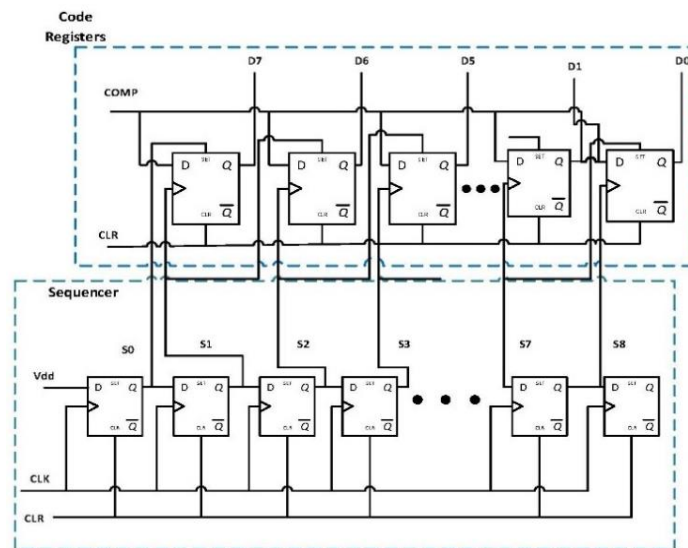


Figure 5. The conventional SAR logic

The code register is being used to store comparison results. Each time the clock input transitions from low to high (rising edge), the comparison result gets stored in the next flip-flop. When eight rising edge occurs in the sequencer, those corresponding flip-flops in the code registers are triggered to take the outputs of the comparator at the time specified as shown in Figure 6. After all, eight clock inputs have been triggered, the code register will contain the complete sequence of comparison results. The code register outputs are then used to control switches within a DAC [37].

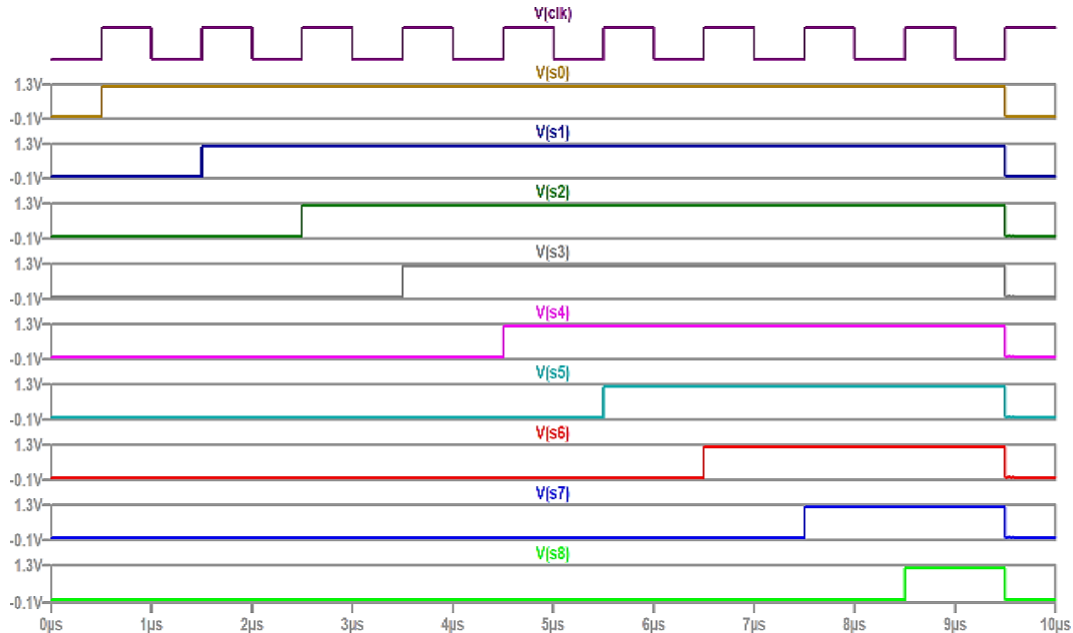


Figure 6. Sequencer output waveform for 8-bit SAR control logic

2.4. Digital to analog converter

Various DAC architectures are readily afforded for converting digital signals to analog ones, each with its advantages and disadvantages i.e. R2R ladder, current steering, and voltage division [38] in the design of a SAR ADC, charge-scaling DAC is used based on its low power consumption, accuracy, and high speed. The charge-scaling DAC architecture utilizes a parallel array of binary-weighted capacitors that have a total value of $2^N C$, where C represents the unit capacitance of any value, and N refers to the number of bits used in the DAC. For instance, in an 8-bit DAC, the capacitor array includes 128 capacitors. When the digital input signal is applied to the DAC, each capacitor is switched to either V_{ref} or ground, creating a voltage division between the capacitors, resulting in an analog output voltage, V_{out} [39]. The DAC's output voltage can be calculated using (1):

$$V_{out} = D_{N-1} \frac{V_{ref}}{2} + D_{N-2} \frac{V_{ref}}{4} + \dots + D_1 \frac{V_{ref}}{2^{N-1}} + D_0 \frac{V_{ref}}{2^N} \quad (1)$$

The architecture of the switched capacitor DAC is illustrated in Figure 7. The architecture has been simulated using CMOS capacitors and transmission gates (TG) used as switches, which are simulated using the spice simulator. The capacitor values (MSB capacitor ... LSB capacitor) are utilized as a multiple of 100 fF unit capacitor.

The circuit in Figure 8 illustrates the operational sequence of a 3-bit SAR ADC with a switching capacitive DAC. The conversion commences by linking the lower plate of the MSB capacitor to the reference voltage via a transmission gate switch. Subsequently, the comparator output is assessed. A high output signals that V_{in} is greater than or equal to the DAC-generated voltage, thus, the TG for the MSB capacitor stays closed, maintaining the connection to V_{ref} . Conversely, if the input voltage is less than the voltage on the top plate of the MSB capacitor, the comparator output is low, indicating that V_{in} is less than the DAC-generated voltage. So, the transmission gate switch for the MSB capacitor is opened, connecting the capacitor's bottom plate to the ground. This process continues until all capacitors in the DAC have been tested and the output gets converted to an analog signal [40]–[43].

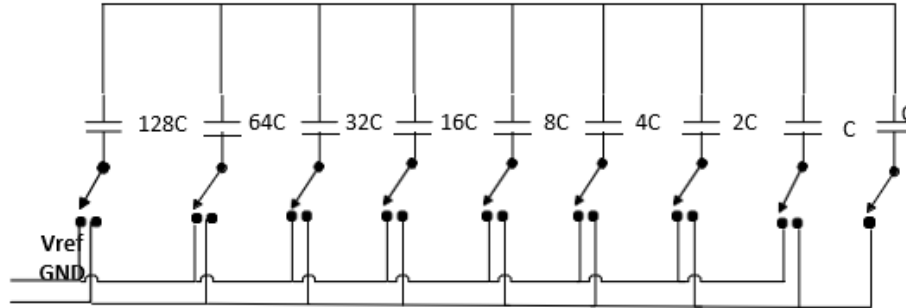


Figure 7. Switched capacitor DAC architecture

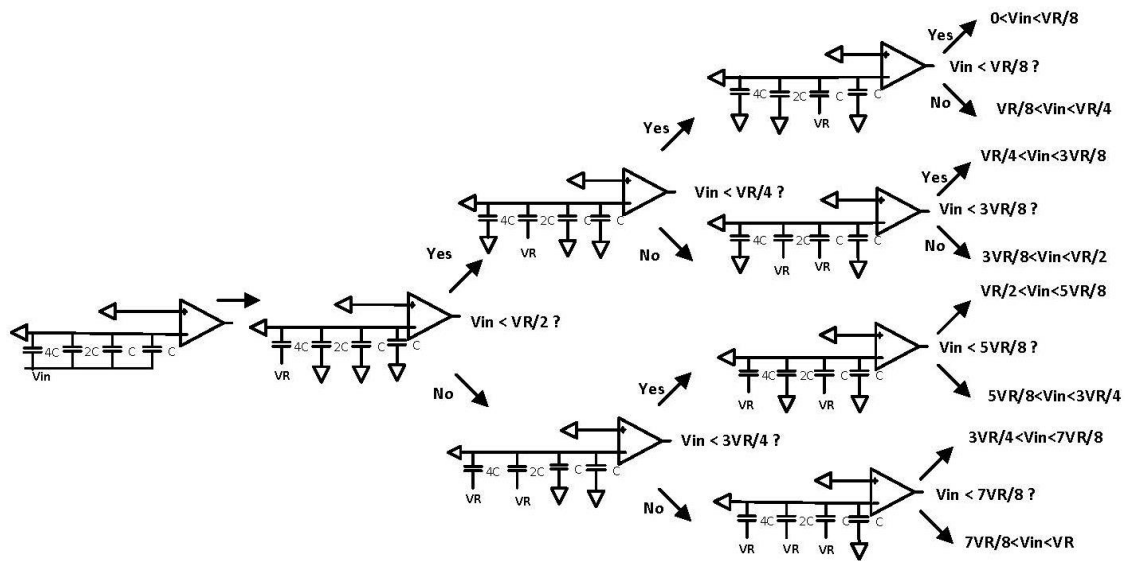


Figure 8. Working flow of 3-bit SAR ADC capacitive DAC switching method

2.5. Latch type comparator

High-speed ADC applications necessitate the use of fast decision-making comparators. The clocked regenerative comparator is one such comparator that is commonly used in high-speed ADC applications due to its ability to make quick decisions. The regenerative latch in the clocked regenerative comparator provides stable positive feedback, which amplifies the input signal’s difference with the reference voltage. This positive feedback ensures that the comparator quickly settles to either a high or low state, making fast decisions possible [43]–[45].

The circuit in Figure 9 illustrates the conventional dynamic latch comparator schematic. The circuit operates in two different conditions based on the state of the CLK signal. When the CLK signal is low, (M_{tail}) the tail transistor is off, and the transistors M_7/M_8 are switched on, resulting in both output nodes V_{outp} and V_{outn} being high (V_{DD}). This state is called the pre-charge state. The moment the CLK signal goes high, the transistors M_7/M_8 are turned off and the transistor M_{tail} is turned on. At this point, the two input voltages, I_{NN} and I_{NP} , begin to discharge the nodes V_{outn} and V_{outp} , respectively, at different rates depending on their relative magnitudes. Assuming that $V_{INN} > V_{INP}$, V_{outn} will discharge more quickly than V_{outp} and vice versa.

The circuit in Figure 10 represents the proposed dynamic comparator. The proposed comparator is similar to the comparator in Figure 9 but with some differences. The latch is formed by the MOSFETs pair (M1/M2 and M5/M6), the tail switch (M_{tail}) has been deleted, and two n-channel clocked switches were added to minimize parasitic resistances in the ground path so the comparator can operate more efficiently and with less time delay. Using NMOS and PMOS transistors in the differential pair as inputs allows for a wider input voltage range to be covered. The NMOS transistors can handle input voltages from V_{thn} to V_{DD} , while the PMOS transistors can handle input voltages from GND to $V_{DD} - |V_{thp}|$. Using both transistors, the circuit can accept input signals that span the entire voltage range from ground to supply voltage [46], [47].

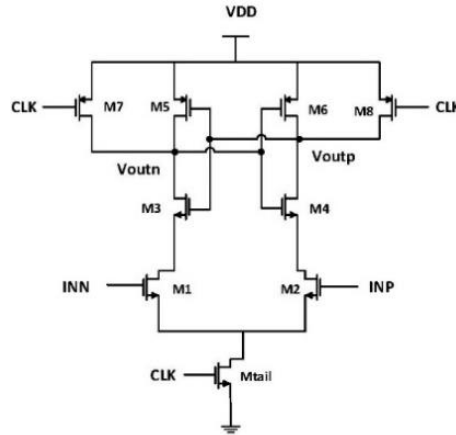


Figure 9. Schematic of the conventional dynamic latch comparator

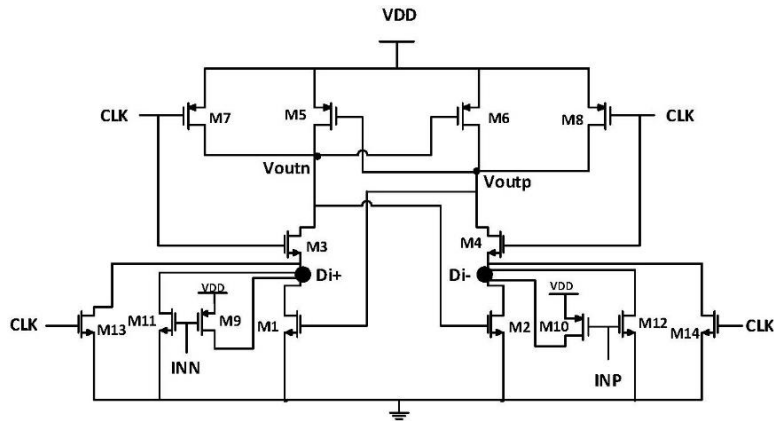


Figure 10. Schematic of the proposed dynamic comparator

The basic operation of this comparator is as follows. When CLK is low, the comparator is in the pre-charge phase, the P-channel clocked switches M_7/M_8 switched ON and pre-charging the output nodes V_{outn} and V_{outp} near V_{DD} , causing M_5 and M_6 to switch Off. M_3/M_4 that act as switches are also off. They are cutting off the connection between V_{DD} and ground to prevent direct current flow in the latch. M_1 and M_2 gates are charged up to V_{DD} , causing their drains to be driven to the ground. The two clocked N-channel switches that were added (M_{13}/M_{14}) switch off. The input signal INN is connected to both gates of input transistors PMOS (M_9) and NMOS (M_{11}), and V_{INP} is connected to both gates of M_{10} and M_{12} . The drains of M_{11} and M_{12} are pulled low because they are connected to the drains of the M_1/M_2 pair.

When CLK transitions to the high state, the comparator enters the evaluation phase, which consists of twophases as shown in Figure 11. In the first phase the latch activation mode t_0 , the clocked N-channel pair M_{13}/M_{14} is clocked ON, M_3/M_4 are switched ON, and M_7/M_8 are OFF. The input pairs (M_9-M_{12}) must be capable of turning ON. With the failure of either pair turning ON, the latch will be unable to generate complete logic levels. The input signal would be in the range from zero to V_{DD} . In the regenerative mode, M_9 and M_{10} are off. They will not turn ON until the pair of NMOS transistors M_1/M_2 turns ON and the voltage at the gates of M_5/M_6 is below $V_{DD} - |V_{thp}|$. M_{11}/M_{12} are used to create an imbalance in the gate-source voltage of the NMOS pair (M_1/M_2) and the input range from V_{thn} to V_{DD} . The conductance imbalance between the left and right branches (M_9/M_{11} and M_{10}/M_{12}) leads to different currents flowing through the corresponding transistors (M_1/M_2) in the circuit, the branch with the higher conductance will allow a higher current to flow through its corresponding transistor, resulting in the drain terminal of that transistor going low first. With M_5/M_6 ON, accelerating the regenerative process. After the second phase which is the latch delay t_{latch} , both outputs of the circuit (V_{outn} and V_{outp}) have reached their final values, one at V_{DD} and the other at ground. By this structure for the proposed dynamic comparator, the total latch delay is $t_{total} = t_0 + t_{latch}$ is much smaller compared with the latch time in the conventional comparator.

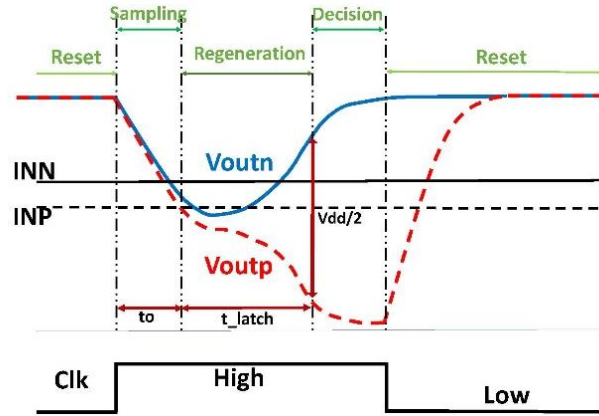


Figure 11. Conventional comparator transient simulations

2.6. Time delay analysis

For the conventional latch comparator shown in Figure 9, consider a case in which transistor M_2 discharges the voltage at node V_{outp} faster than transistor M_1 discharges the voltage at node V_{outn} . As a result, t_0 is the time delay induced between the transistors M_5 and M_6 turning on and discharging the load capacitance C_L . We can describe the discharge delay mathematically as (2):

$$t_0 = \frac{C_L |V_{thp}|}{I_2} \quad (2)$$

where C_L is the load capacitance and V_{thp} is the threshold voltage of the PMOS transistor. I_2 is equal to one-half of the current of the tail transistor and is considered to be a constant value and equal to I_1 since:

$$I_{Mtail} = I_1 + I_2 \quad (3)$$

$$t_0 = \frac{C_L |V_{thp}|}{\frac{I_{Mtail}}{2}} \quad (4)$$

$$I_2 = \frac{I_{Mtail}}{2} + \Delta I_{in} \quad (5)$$

$$I_2 = \frac{I_{Mtail}}{2} + g_{m1,2} \Delta V_{in} \quad (6)$$

where g_m is the transconductance of the input transistors M_1 and M_2 and ΔV_{in} refers to the small difference in input voltage.

Also, we can observe the second part of the time delay, which is the t_{latch} and it illustrates the delay that occurs in the two cross-coupling inverters connected in the feedback loop that formed the latch. Let's consider the difference in the initial voltage at the output end ΔV_0 results in the voltage swing being $V_{DD}/2$. Therefore, t_{latch} can be defined mathematically as (7), (8):

$$t_{latch} = \frac{C_L}{g_{m,L}} \ln \left(\frac{\Delta V_{out}}{\Delta V_0} \right) \quad (7)$$

$$t_{latch} = \frac{C_L}{g_{m,L}} \ln \left(\frac{\frac{V_{DD}}{2}}{\Delta V_0} \right) \quad (8)$$

where $g_{m,L}$ is the equivalent transconductance of the decision circuit. Moreover, it scales with the combined values of $g_{m3,4}$ and $g_{m5,6}$.

At $t=t_0$, the delay is proportional to the logarithm of the voltage difference at the output nodes, and the initial differential voltage at $t=t_0$ can be expressed using (2), (3) as (9):

$$\Delta V_0 = |V_{outn} - V_{outp}| \quad (9)$$

$$\Delta V_0 = |V_{thp}| - \frac{t_0 I_2}{C_L} \tag{10}$$

$$\Delta V_0 = |V_{thp}| \left(1 - \frac{I_1}{I_2}\right) \tag{11}$$

by introducing the term $\Delta I_{in} = |I_2 - I_1|$, and $I_2 = \frac{I_{Mtail}}{2}$ (11) becomes:

$$\Delta V_0 = |V_{thp}| \frac{\Delta I_{in}}{\frac{I_{Mtail}}{2}} \tag{12}$$

In terms of the current factor of the transistors M_1 and M_2 , which respectively is β_1, β_2 respectively, and ΔV_{in} , which is the small difference in input voltage, we can rewrite (12) as:

$$\Delta V_0 = 2|V_{thp}| \frac{g_{m1,2} \Delta V_{in}}{I_{Mtail}} \tag{13}$$

where $g_{m1,2} = \beta_{1,2}(V_{gs1,2} - V_{in1,2})$, so (13) can be written as:

$$\Delta V_0 = 2|V_{thp}| \sqrt{\frac{\beta_{1,2}}{I_{Mtail}}} \Delta V_{in} \tag{14}$$

So, the expression of the time delay of the conventional dynamic latch comparator becomes:

$$t_{delay} = t_0 + t_{latch} \tag{15}$$

$$t_{delay} = \frac{C_L |V_{thp}|}{\frac{I_{Mtail}}{2}} + \frac{C_L}{g_{m,L}} \ln \left(\frac{V_{DD}}{4|V_{thp}| \Delta V_{in} \sqrt{\frac{I_{Mtail}}{\beta_{1,2}}}} \right) \tag{16}$$

As shown in (16), the time delay of the conventional dynamic latch comparator is affected by various parameters, it is directly dependent on the load capacitance, and increasing the load capacitance drives an increase in the delay. Furthermore, the current passing in the tail transistor affects the time delay, the smaller the drain current I_{Mtail} the larger the delay time. So, the presence of the single current path through I_{Mtail} in the structure of the conventional comparator leads to a drawback in the architecture. The equivalent transconductance of the decision circuit $g_{m,L}$, which scales to the combined value of $g_{m3,4}$ and $g_{m5,6}$ is another parameter that can affect the performance of the comparator. Smaller transconductance due to the ground path impedance generally enables lower regeneration of the latch and longer operation, increasing the latch time. Based on the previous discussion, we found an effective approach for minimizing delay time by minimizing the parasitic impedance in the ground path for the decision circuit which helps to ensure efficient current flow and improve its overall performance as illustrated in Figure 12 where X, Y are V_{outn}, V_{outp} respectively, and $g_{m,x}$ is the equivalent transconductance looking to node Y, and $g_{m,y}$ is the equivalent transconductance looking to node X.

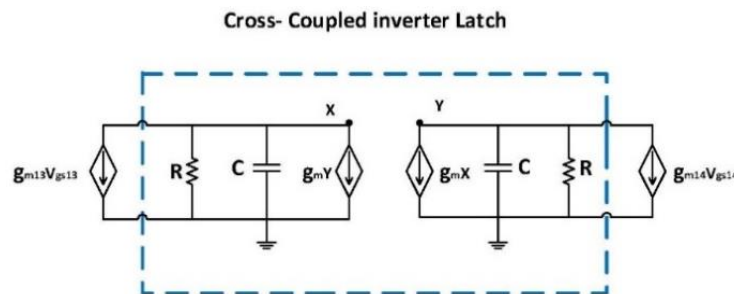


Figure 12. Schematic of the small signal model in the latch stage

Time analysis for the proposed comparator is as follows: assume a condition where $INN > INP$. In this situation, the node V_{outn} discharged faster than node V_{outp} . The delay t_0 is the time between the discharge

of the load capacitance at V_{outn} and V_{outp} nodes and either of the transistors M_5 or M_6 turning On. It can be given as (17):

$$t_0 = \frac{C_L |V_{thp}|}{I_{3,4}} \quad (17)$$

Latch, the second part of the time delay is experienced during cross-coupled latch operation. It is determined by the initial voltage difference ΔV_0 , representing the decision threshold set at one-half of V_{DD} , resulting in the expression in (18). Figure 13 indicates the transient simulation for the proposed dynamic comparator.

$$t_{latch} = \frac{C_L |V_{thp}|}{g_{m,eq} + g_{m13,14}} \ln \left(\frac{V_{DD}/2}{\Delta V_0} \right) \quad (18)$$

The total delay can be written as:

$$t_{delay} = t_0 + t_{latch} \quad (19)$$

$$t_{delay} = \frac{C_L |V_{thp}|}{I_{3,4}} + \frac{C_L |V_{thp}|}{g_{m,eq} + g_{m13,14}} \ln \left(\frac{V_{DD}}{2\Delta V_0} \right) \quad (20)$$

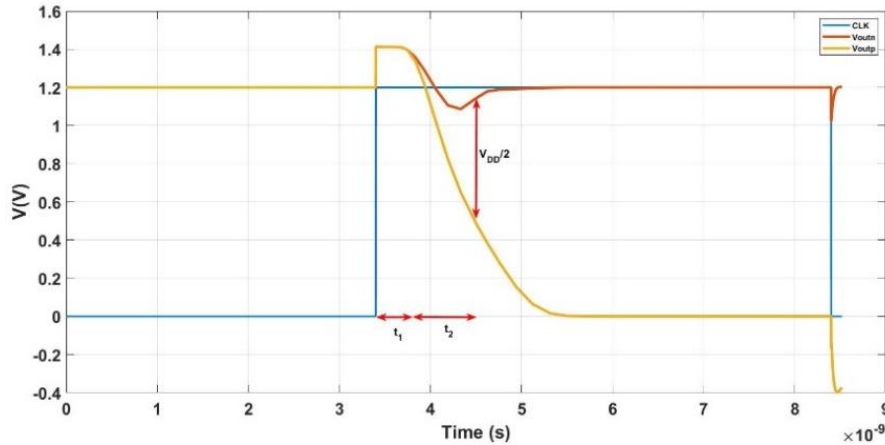


Figure 13. Transient simulation of the proposed comparator

2.7. Offset analysis

The voltage difference between the comparator's positive and negative input terminals is the offset voltage when the input signals are at the same voltage level. An ideal comparator switches its output voltage from zero to one once the positive input voltage exceeds the negative input voltage. However, in the real world, the comparators exhibit an offset voltage, which is the voltage difference needed for the output to be switched. Offset voltage minimization is important for accurate and exact comparisons. Thus, when designing a comparator to be sensitive and precise minimizing the input offset voltage is crucial. The offset voltage of the comparator is the input voltage difference required to balance the outputs resulting in no output voltage ($V_{out+} = V_{out-}$). In the beginning, it is assumed that the comparator in a balanced mode of operation maintains symmetric currents in both branches at all times. This symmetrical configuration allows for determining the bias voltages and currents for each transistor in the comparator. The input pairs transistors M_9 M_{12} are in the saturation region to select the drain current equations that will be used. For calculating the offset voltage caused by the mismatch in each input transistor pair individually by using the superposition concept. Varying the threshold voltage (ΔV_{th}) and current factor (β) for that particular pair while keeping the other transistor pairs matched. To perform the offset a voltage source ΔV_{offset} will be added to one of the comparator inputs, the input NMOS transistor pair M_{11}/M_{12} has a mismatch, while the input PMOS transistor pair M_9/M_{10} is matched. The drain current of M_{11} in the left branch is expressed as (21):

$$I_{D11} = \frac{\mu_n \cdot C_{ox}}{2} \cdot \left(\frac{W_n + \Delta W_{n11}}{L_n} \right) \left(V_{GS11} + \Delta V_{offset11,12} - (V_{thn} + \Delta V_{th11}) \right)^2 \quad (21)$$

The drain current M_{12} in the right branch is expressed as (22):

$$I_{D12} = \frac{\mu_n \cdot C_{ox}}{2} \cdot \left(\frac{W_n + \Delta W_{n12}}{L_n} \right) \cdot (V_{GS12} - (V_{thn} + \Delta V_{th12}))^2 \quad (22)$$

The output voltages of the differential input at the nodes V_{Di+} and V_{Di-} is equal, so $\Delta V_{out} = V_{Di+} - V_{Di-}$ which is equals to (23) and (24).

$$V_{Di+} = V_{DD} - V_{SD9} \quad (23)$$

$$V_{Di-} = V_{DD} - V_{SD10} \quad (24)$$

Assuming that transistors M_9 and M_{10} are in the saturation region, so ($V_{SD} = V_{SG} - V_{thp}$). The drain current of M_{11} is the same current passing through M_9 , and the drain current of M_{12} is the same current passing through M_{10} . So, the source to gate voltages of transistors M_9 and M_{10} can be identified by using (25), (26):

$$V_{SG9} = \sqrt{\frac{2I_{D11}}{\beta}} + V_{thp} \quad (25)$$

$$V_{SG10} = \sqrt{\frac{2I_{D12}}{\beta}} + V_{thp} \quad (26)$$

where the current factor β is equal to $\mu_p C_{ox} \cdot \left(\frac{W_p}{W_n} \right)$. When V_{Di+} equals V_{Di-} , the offset voltage $\Delta V_{offset11,12}$ is determined.

$$V_{Di+} - V_{Di-} = \sqrt{\frac{2I_{D11}}{\beta}} - \sqrt{\frac{2I_{D12}}{\beta}} = 0 \quad (27)$$

By substituting (21) and (22) into (27), the offset voltage can be found as (28):

$$\Delta V_{offset11,12} = \sqrt{\frac{W_n + \Delta W_{n12}}{W_n + \Delta W_{n11}}} \cdot (V_{GS12} - (V_{thn} + \Delta V_{th12}) - V_{GS11} + (V_{thn} + \Delta V_{th11})) \quad (28)$$

When the change ΔW_n in a quantity W_n is small compared to W_n itself ($\frac{\Delta W_n}{W_n} \ll 1$), the following approximations are commonly used in various mathematical calculations: $\sqrt{1 + \varepsilon}$ can be approximated as $1 + \frac{\varepsilon}{2}$, therefore $\Delta V_{offset11,12}$ becomes:

$$\Delta V_{offset11,12} = \left[1 + \frac{\Delta W_{n12}}{2W_n} \right] \cdot \left[1 - \frac{\Delta W_{n11}}{2W_n} \right] \cdot (V_{GS12} - (V_{thn} + \Delta V_{th12}) - V_{GS11} + (V_{thn} + \Delta V_{th11})) \quad (29)$$

The variations in V_{th} and W_n are represented by Gaussian random variables, the normal Gaussian distribution can be used to approximate the distributions of V_{th} and W_n . When combining the two Gaussian random variables [48]–[50], in this case, the offset voltage variance σ^2 due to M_{11} and M_{12} mismatch can be stated as (30):

$$\sigma_{\Delta V_{offset11,12}}^2 = \sigma_{thn11}^2 + \sigma_{thn12}^2 + \left[\frac{V_{GS12} - V_{thn}}{2} \right]^2 \cdot \sigma_{\frac{\Delta W_{n11}}{W_n}}^2 + \left[\frac{V_{GS12} - V_{thn}}{2} \right]^2 \cdot \sigma_{\frac{\Delta W_{n12}}{W_n}}^2 \quad (30)$$

Now ΔV_{offset} will be found due to the mismatch in the input PMOS transistor pair M_9/M_{10} , meanwhile M_{11}/M_{12} are thought to be matched. The same procedure used to find $\Delta V_{offset11,12}$ will be repeated for finding $\Delta V_{offset9,10}$:

$$I_{D11} = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W_n}{L_n} \cdot (V_{GS11} + \Delta V_{offset9,10} - V_{thn})^2 \quad (31)$$

$$I_{D12} = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W_n}{L_n} \cdot (V_{GS12} - V_{thn})^2 \quad (32)$$

The drain current of M_{11} is the same current passing through M_9 , and the drain current of M_{12} is the same current passing through M_{10} . The output voltages of the differential input at the nodes V_{Di+} and V_{Di-} are equal to (33) and (34):

$$V_{Di+} = V_{DD} - V_{SD9} \quad (33)$$

$$V_{Di-} = V_{DD} - V_{SD10} \quad (34)$$

The same assumption will be taken, that transistors M_9 and M_{10} are in the saturation region, so ($V_{SD}=V_{SG} - V_{thp}$). Where the source to gate voltages of transistors M_9 and M_{10} is:

$$V_{SG9} = \sqrt{\frac{2I_{D11}}{\frac{W_p + \Delta W_{p9}}{L_p}} \cdot \mu_p C_{ox}} + V_{thp} + \Delta V_{th9} \quad (35)$$

$$V_{SG10} = \sqrt{\frac{2I_{D12}}{\frac{W_p + \Delta W_{p10}}{L_p}} \cdot \mu_p C_{ox}} + V_{thp} + \Delta V_{th10} \quad (36)$$

V_{Di+} is set to equal V_{Di-} as (37):

$$V_{Di+} - V_{Di-} = \sqrt{\frac{2I_{D11}}{\frac{W_p + \Delta W_{p9}}{L_p}} \cdot \mu_p C_{ox}} + \Delta V_{th9} - \sqrt{\frac{2I_{D11}}{\frac{W_p + \Delta W_{p9}}{L_p}} \cdot \mu_p C_{ox}} + \Delta V_{th9} = 0 \quad (37)$$

The offset voltage $\Delta V_{offset9,10}$ can be found by substituting (31) and (32) into (37) as in (38):

$$\Delta V_{offset9,10} = \frac{(\Delta V_{th10} - \Delta V_{th9})}{\frac{\mu_n}{\mu_p} \cdot \frac{L_p}{W_n} \cdot \frac{W_p + \Delta W_{p9}}{L_p}} \cdot \sqrt{\frac{W_p + \Delta W_{p9}}{W_p + \Delta W_{p10}}} \cdot (V_{GS12} - V_{thn}) - (V_{GS11} - V_{thn}) \quad (38)$$

Rearranging (38) is as (39):

$$\Delta V_{offset9,10} = (\Delta V_{th10} - \Delta V_{th9}) \cdot \sqrt{\frac{\mu_p}{\mu_n} \cdot \frac{L_p}{W_n} \cdot \frac{W_p + \Delta W_{p9}}{L_p}} + \sqrt{\frac{1 + \frac{\Delta W_{p9}}{W_p}}{1 + \frac{\Delta W_{p10}}{W_p}}} \cdot (V_{GS12} - V_{thn}) - (V_{GS11} - V_{thn}) \quad (39)$$

With the same approximation for (29) and $\frac{\Delta W_p}{W_p} \ll 1$, (39) becomes:

$$\Delta V_{offset9,10} = (\Delta V_{th10} - \Delta V_{th9}) \cdot \sqrt{\frac{\mu_p}{\mu_n} \cdot \frac{L_p}{W_n} \cdot \left(1 + \frac{\Delta W_{p9}}{2W_p}\right)} + (V_{GS12} - V_{thn}) \cdot \left(1 + \frac{\Delta W_{p9}}{2W_p}\right) \cdot \left(1 - \frac{\Delta W_{p10}}{2W_p}\right) - (V_{GS11} - V_{thn}) \quad (40)$$

The offset voltage variance σ_2 due to M_9 and M_{10} mismatch can be stated as (41):

$$\sigma_{\Delta V_{offset9,10}}^2 = \left[\frac{\mu_p}{\mu_n} \cdot \frac{L_p}{W_n} \cdot \frac{W_p}{L_n} \right] \cdot \sigma_{\Delta V_{th9}}^2 + \left[\frac{\mu_p}{\mu_n} \cdot \frac{L_p}{W_n} \cdot \frac{W_p}{L_n} \right] \cdot \sigma_{\Delta V_{th10}}^2 + \left[\frac{V_{GS12} - V_{thn}}{2} \right]^2 \cdot \sigma_{\frac{\Delta W_{p9}}{W_p}}^2 + \left[\frac{V_{GS12} - V_{thn}}{2} \right]^2 \cdot \sigma_{\frac{\Delta W_{p10}}{W_p}}^2 \quad (41)$$

The overall variance in input offset voltage is described as (42):

$$\sigma_{\Delta V_{offset}}^2 = \sigma_{\Delta V_{offset11,12}}^2 + \sigma_{\Delta V_{offset9,10}}^2 \quad (42)$$

2.8. Gain analysis

Analyzing each stage of the comparator circuit for gain is a usual approach for simplifying and recognizing its behavior. The comparator often consists of multiple stages, the most common stages are the pre-amplifier stage, the differential input stage, and the regenerative latch stage (decision-making stage). The initial stage in the comparator circuit is the pre-amplifier stage, then the differential input stage, its role is to amplify the slight voltage difference between input signals, ensuring the comparator operates effectively by

providing the required gain. The pre-amplifier featuring symmetrical halves allows the application of the Bisection theorem for circuit analysis. Figure 14 illustrates the half circuit of the pre-amplifier stage shown in Figure 14(a) alongside its small-signal equivalent circuit schematic shown in Figure 14(b) [19]. In the case of both M_9 and M_{11} , this circuit functions as a push-pull amplifier. To find the gain of the push-pull amplifier, the input and output voltages should be defined. The output voltage can be described as (43), (44):

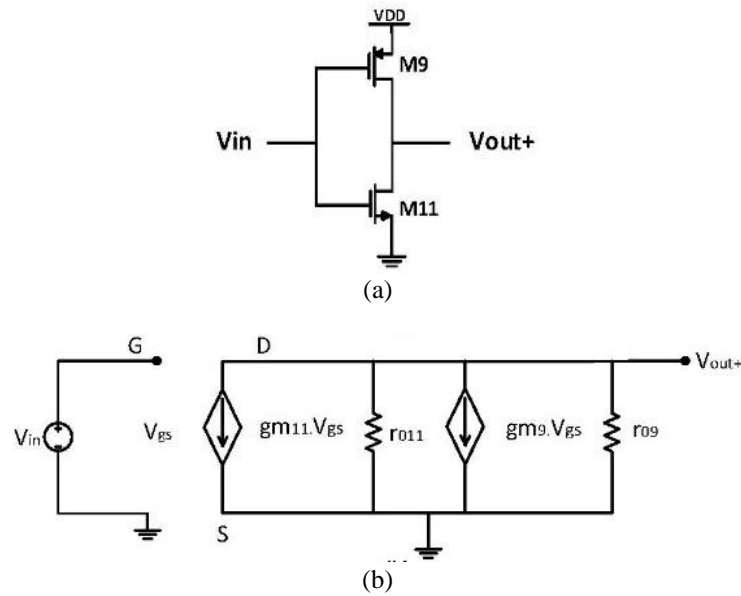


Figure 14. Illustration of the half circuit for the pre-amplifier stage (a) push-pull amplifier and (b) small-signal equivalent circuit for the push-pull amplifier

$$V_{out+} = -(g_{m11}V_{gs} + g_{m9}V_{gs}) \cdot r_{09} || r_{011} \tag{43}$$

$$V_{out+} = \frac{-(g_{m11}V_{gs} + g_{m9}V_{gs})}{g_{ds11} + g_{ds9}} \tag{44}$$

and $V_{in} = V_{gs}$, the gain of the push-pull inverter:

$$A = \frac{V_{out+}}{V_{in}} = -\frac{g_{m11} + g_{m9}}{g_{ds11} + g_{ds9}} \tag{45}$$

The differential input stage typically consists of two transistors configured differentially, often as a differential pair. It amplifies the voltage difference between the inverting and non-inverting inputs. This amplification is essential for driving the subsequent stages of the comparator. The schematic of the differential input stage is shown in Figure 15. The differential input has two symmetrical halves; thus, the Bisection theorem can be used to analyze the circuit.

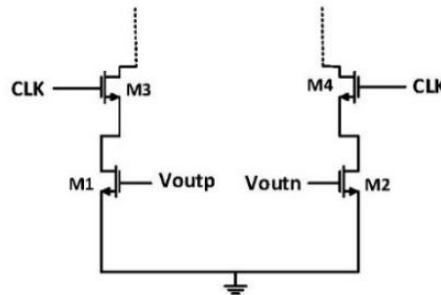


Figure 15. Differential input stage circuit schematic

In the differential input stage, under common-mode conditions, the decision circuit exhibits symmetrical characteristics. Both inputs share identical magnitudes and phases, resulting in equal values for V_{gs3} and V_{gs4} . The bisected small-signal equivalent circuit represented in Figure 16, employing Thevenin equivalence, the determination of the output impedance is illustrated in Figure 17.

$$V_T = (I_T + g_{m3}V_{gs3})r_{o3} \tag{46}$$

$$V_{gs} = -V_T \tag{47}$$

$$V_T = (I_T + g_{m3}V_T)r_{o3} \tag{48}$$

By dividing V_T by I_T , the value of R_0 is given out as:

$$R_0 = \frac{V_T}{I_T} = \frac{r_{o3}}{1 + g_{m3}r_{o3}} = \frac{1/g_{m3}r_{o3}}{\frac{1}{g_{m3}} + r_{o3}} \tag{49}$$

$$R_0 = r_{o3} \parallel \frac{1}{g_{m3}} \tag{48}$$

The differential input gain is expressed as (51),

$$A_v = -g_{m1} \cdot [R_0 \parallel r_{o1}] \tag{51}$$

$$A_v = -g_{m1} \cdot \left[r_{o3} \parallel \frac{1}{g_{m3}} \parallel r_{o1} \right] \tag{52}$$

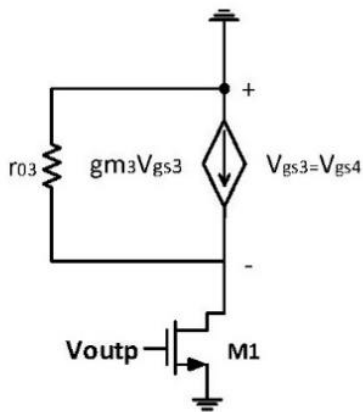


Figure 16. Bisected equivalent circuit for the differential input stage

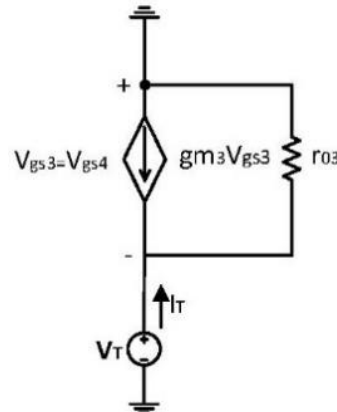


Figure 17. Equivalent circuit to find R_0

The regenerative stage is the heart of the comparator, performing a comparison between both of its inputs, terminal one is connected to the input signal, and terminal two is connected to the reference voltage. It offers positive feedback to enhance speed and accuracy. This circuit, prevalent in latch design, features two symmetrical halves and cross-coupled loads Figure 18, making it analyzable via the Bisection theorem. The small-signal equivalent circuit for the decision stage is illustrated in Figure 19.

In the common mode, the decision circuit exhibits symmetrical features. Both inputs share the same magnitude and phase, leading to $V_{gs3}=V_{gs4}$. This balanced behavior results in the transfer of M_3 's dependency to the left circuit half and M_4 's dependency to the right. The bisected small-signal equivalent circuit, illustrated in Figure 20, resembles a common-source amplifier. The dependent current source, controlled by V_{gs3} , can be substituted with a resistor equal to $1/g_{m3}$. Utilizing Thevenin equivalence, we determine the drain resistance R_{D5} of M_5 , as depicted in Figure 21.

$$V_T = (I_T - g_{mb3}V_{bs3}) \left[r_{o3} \parallel \frac{1}{g_{m3}} \right] \tag{53}$$

Since $g_{mb3} \ll g_{m3}$, (53) can be simplified to:

$$V_T = (I_T) \left[r_{o3} \parallel \frac{1}{g_{m3}} \right] \tag{54}$$

By dividing V_T by I_T , the value of R_{D5} is given out, and the resistance is connected to M_5 's drain:

$$R_{D5} = \frac{V_T}{I_T} = r_{o3} \parallel \frac{1}{g_{m3}} \tag{55}$$

The single-ended common mode gain is expressed as (56).

$$A_{cm,se} = -g_{m5} \cdot [R_{D5} \parallel r_{o5}] \tag{56}$$

For the differential mode analysis, the source terminals of M_5 and M_3 are linked to virtual ground, so there is no body effect. The equivalent circuit for the regenerative stage in the differential mode is shown in Figure 22 and used to find M_3 impedance.

$$R_{intoM3} = \frac{V_T}{I_T} = - \frac{V_{gs3}}{V_{gs3} \cdot g_{m3} - \frac{V_{gs3}}{r_{o3}}} = - \frac{1}{g_{m3}} \parallel r_{o3} \tag{57}$$

The circuit in Figure 23 depicts the resulting small-signal equivalent-circuit schematic for the bisected circuit. The single-ended output's differential-mode gain is:

$$A_{dm,se} = -\frac{1}{2} \cdot g_{m5} \left[r_{o3} \parallel -\frac{1}{g_{m3}} \right] \parallel r_{o5} \tag{58}$$

The gain of the differential output differential mode is:

$$A_{dm,do} = -g_{m5} \left[r_{o3} \parallel -\frac{1}{g_{m3}} \right] \parallel r_{o5}. \tag{59}$$

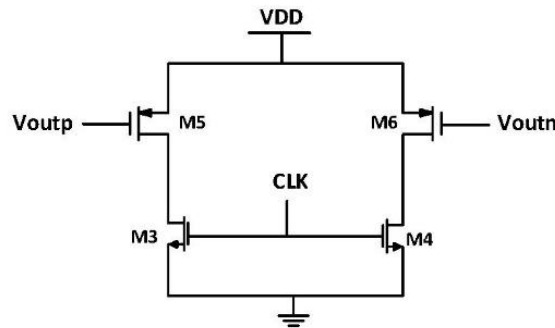


Figure 18. Decision stage circuit schematic

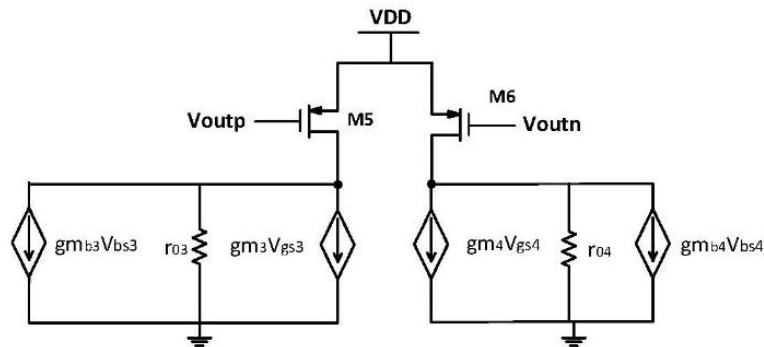


Figure 19. Small-signal equivalent circuit for the decision stage

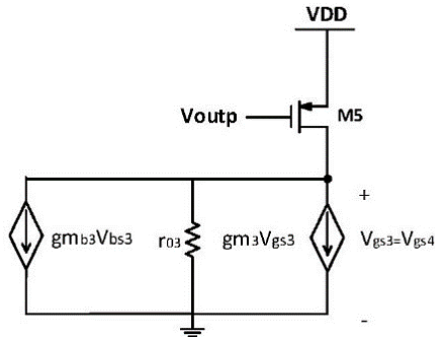


Figure 20. Bisected equivalent circuit for the decision stage

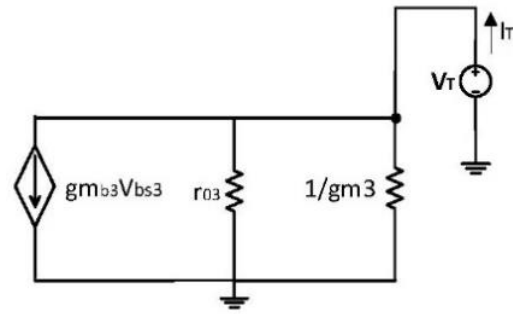


Figure 21. Equivalent circuit to find R_{D5}

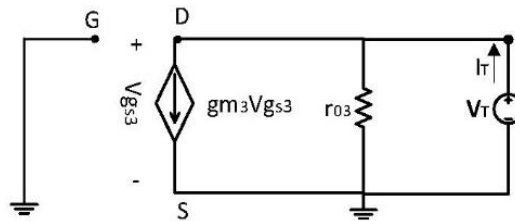


Figure 22. Small signal equivalent circuit in differential mode

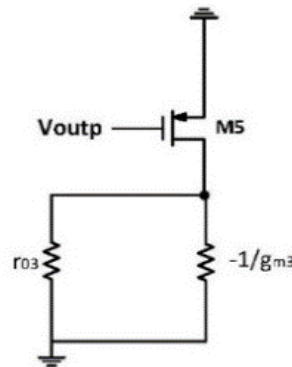


Figure 23. Bisected small signal equivalent circuit in differential mode

3. RESULTS AND DISCUSSION

A spice simulator with a 180 nm technology model file is used to simulate the SAR ADC with a power supply voltage set to 1.2 V. The SAR logic and control circuit was driven by a single clock of 1 MHz. therefore, the period of each conversion cycle is 1 μ s, implying a conversion rate of 125K samples per second for an 8-bit ADC. Figure 24 shows the result of the sample and hold circuit when applying a ramp input test. Figure 25 depicts the conversion cycle for the DAC output for an input voltage of 0.8 V.

The output and input waveforms of the proposed dynamic latch comparator are shown in Figure 26. The voltages at the input and reference are compared, where INP is set as the reference voltage. When $INN > INP$, the value at the output is high, and when $INN < INP$, the value at the output is low. The conventional dynamic latch comparator in [51] is implemented with the same procedure for the proposed comparator. A performance comparison between the conventional and proposed comparator is given in Table 1. The latch time delay of the conventional comparator is 983 ps compared to 159 ps for the proposed comparator. Table 1 presents a detailed performance comparison, highlighting the proposed comparator's favorable attributes, including reduced time delay and lower power consumption 9.2 mW when compared to alternative designs. This side-by-side evaluation emphasizes the practical benefits and efficiency gains achieved by our proposed SAR ADC.

To determine the input offset voltage of the comparator a Monte Carlo analysis is employed. A simple test setup is created shown in Figure 27. The test uses a ramp input voltage applied to one comparator input, while a constant DC voltage equal to the common mode voltage $V_{CM} = V_{DD}/2$ is provided to the other comparator input. The Monte Carlo simulation is run iteratively for a total of 300 trials. The results of the simulation are saved in a file and recorded in MATLAB to determine the input offset voltage.

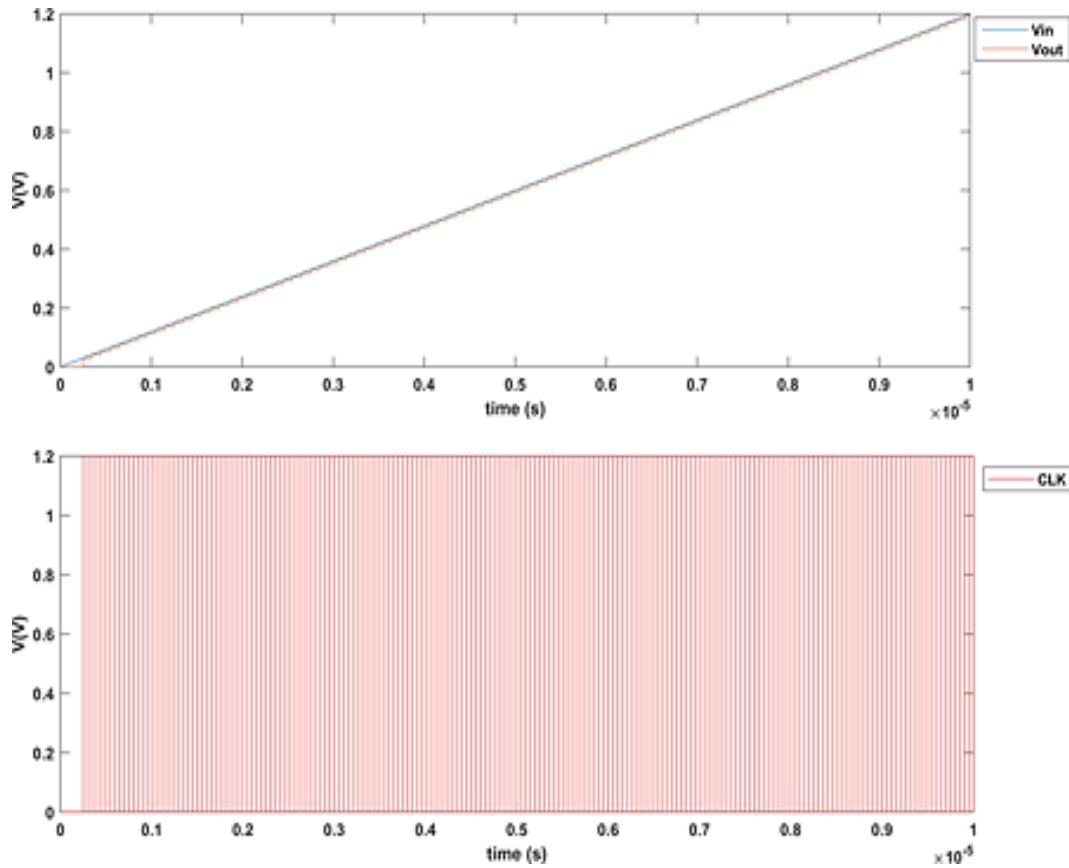


Figure 24. Sample and hold ramp test

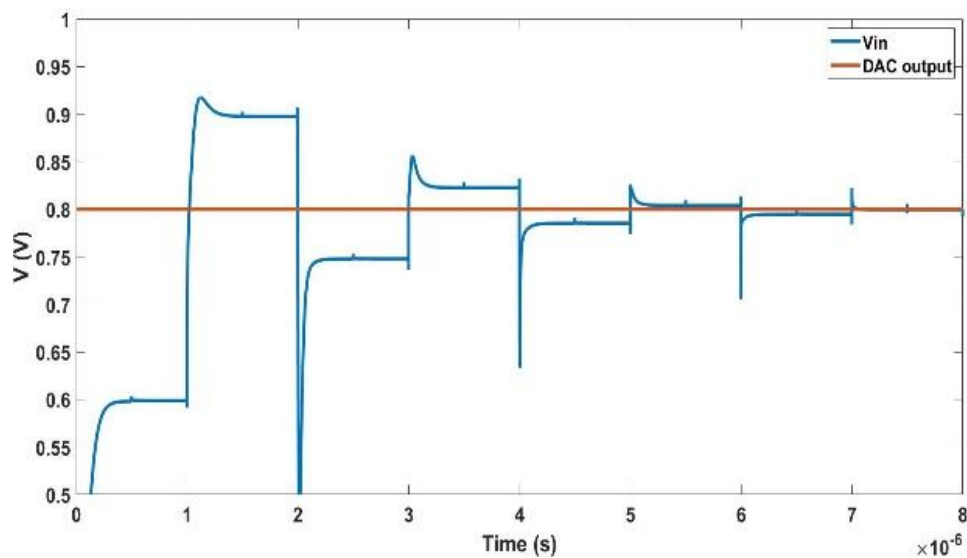


Figure 25. DAC output during a conversion

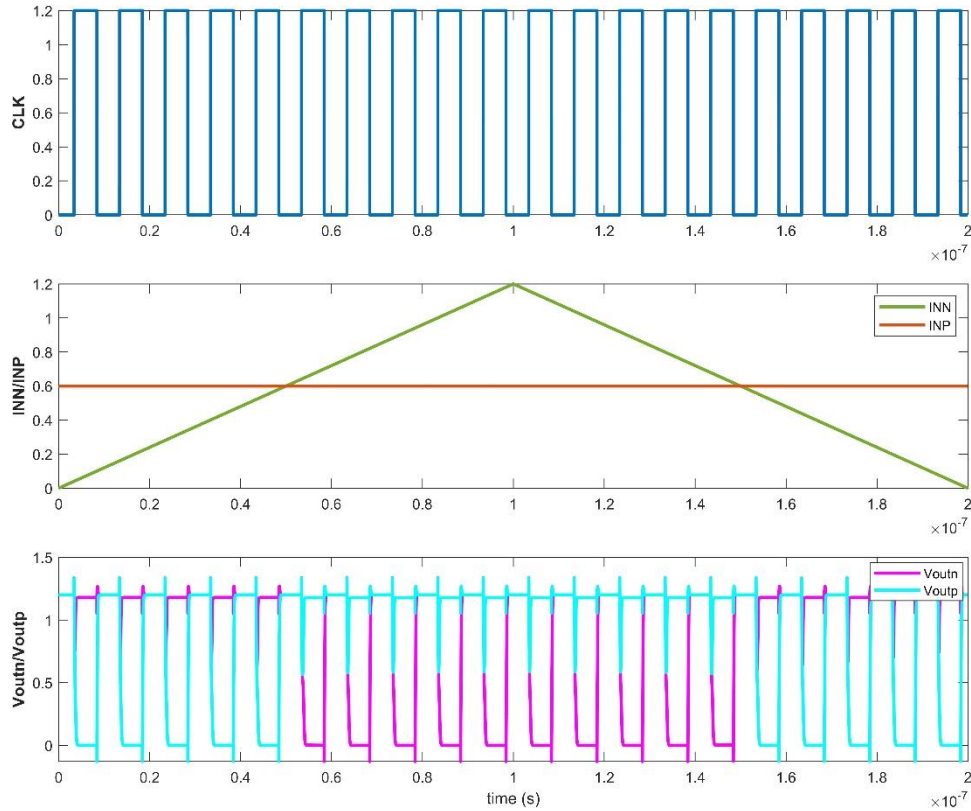


Figure 26. Transient response of the proposed comparator

Table 1. Performance summary and comparison

Specification (unit)	Conventional dynamic latch comparator [52]	modified strong-arm latch comparator [53]	Proposed comparator in this work
Technology(nm)	180	180	180
Supply voltage (V)	1.2	1.2	1.2
Resolution (bit)	8	8	8
Sampling rate (S/s)	125K	125k	125k
Power consumption (mW)	12	30	9.2
Time delay (ps)	983	1730	159

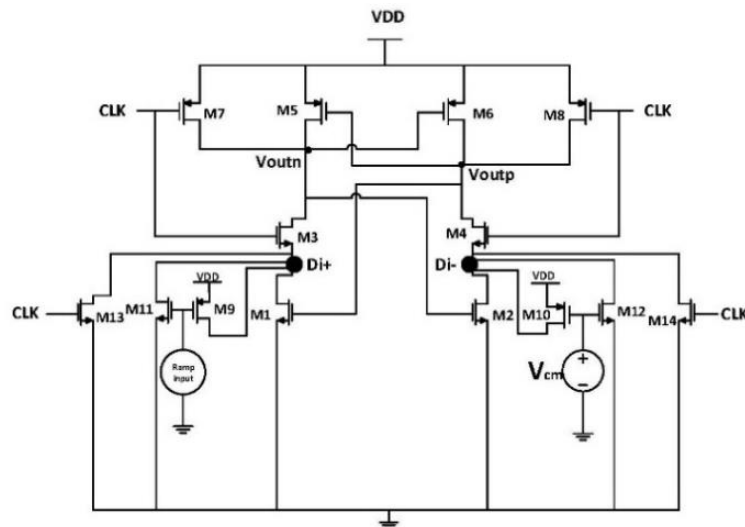


Figure 27. Offset simulation test

The Monte Carlo analysis for input offset voltage yields a standard deviation of $\sigma_{\Delta V_{offset}}^2 = 55 \text{ mV}$ shown in Figure 28. The results emphasize the reliability and consistency of the proposed comparator. The comparison of our SAR ADC with previous works interprets the significant enhancements in resolution, sampling rate, and technology, reinforcing the potential impact of our design on precision ADC technology.

An 8-bit SAR ADC based on the proposed comparator is simulated, SAR's sub-modules are all implemented in 180 nm technology and its performance is tested. For 8-bit SAR ADC and V_{ref} are set to 1.2 V, and $V_{in} = 0.895 \text{ V}$, the output will turn out to be ≈ 191 according to the equation $V_{in} * 2^N / V_{ref}$. The 8-bit binary equivalent digital code of the ADC of 191 is 10111111. Figure 29 demonstrates the digital output corresponding to the input of 0.895 V.

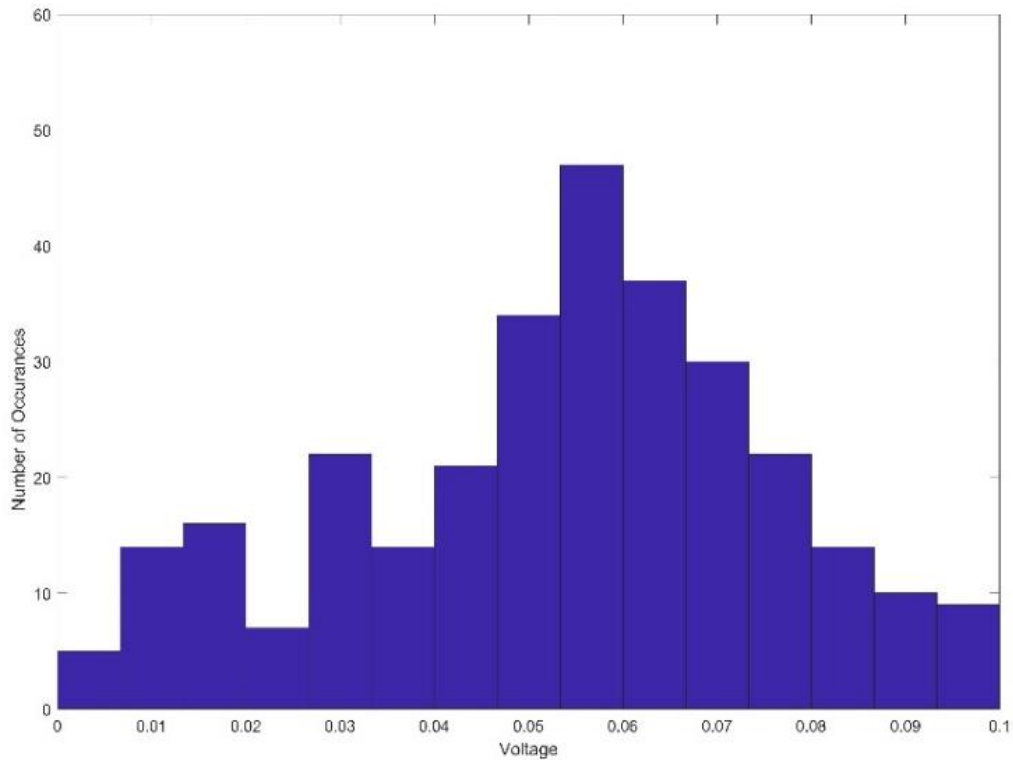


Figure 28. Histogram test of Monte Carlo simulation due to offset voltage

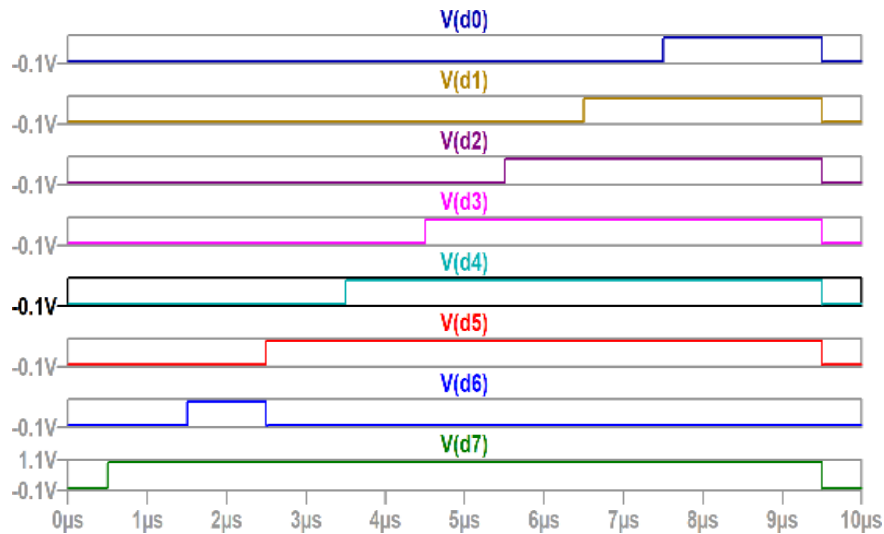


Figure 29. Digital output for $V_{in} = 0.895 \text{ V}$

The voltage difference between code transitions can deviate from one LSB, which is measured as DNL. It can be calculated using (60):

$$DNL = \frac{(V_{i+1} - V_i) - LSB}{LSB} \quad (60)$$

where V_i is the voltage of the i^{th} code transition, V_{i+1} is the voltage of the next code transition, and LSB is the nominal width of the digital output codes. The INL is determined by measuring the voltage at which each code transition occurs in the ADC's output and comparing it to the ideal voltage for that code transition. By comparing the actual voltage at each code transition to the ideal voltage, it is possible to determine the deviation of the ADC's response from linearity, and it is expressed in units of LSB or percent of the full-scale range. It can be calculated using (61):

$$INL = \frac{V_i - V_{zero}}{V_{LSB}} - i \quad (61)$$

where V_i is the input voltage at i^{th} code transition, V_{min} is the minimum analog voltage that can be represented by the ADC, V_{LSB} is the least significant bit of the ADC, and i is the index of the current sample, $\in [0, 2^N - 1]$. To calculate the DNL and INL errors, a Monte-Carlo simulation with 2,561 samples was used in the transient analysis. Figure 30 and Figure 31 show the performance results. Where the maximum DNL is (+0.6/-0.8) LSB and INL is (+0.4/-0.7) LSB. Table 2 compares the proposed SAR ADC with previous works showcasing a significant enhancement in precision. Figure 32 depicts the layout of the SAR ADC with the proposed comparator occupying a core area of 351.35 μm by 771 μm .

In this study, the implementation of the novel dynamic comparator design has yielded significant improvements in the INL and DNL of the SAR ADC. The enhanced precision, speed characteristics of the comparator have played a pivotal role in achieving commendable results. The achieved INL and DNL characteristics shown in Table 2 are a showcase the success of the proposed approach in mitigating errors during the conversion process. Importantly, the improvements in the comparator have not only led to superior INL and DNL but have also contributed to enhancing the overall precision efficiency and performance of the SAR ADC. This accomplishment stands out in comparison to solutions proposed by other authors. Unlike some existing methods that introduce additional complexity, calibration requirements, or trade-offs, the implemented dynamic comparator design manages to achieve improved performance without such drawbacks. The novel approach presented in this study demonstrates its efficacy in optimizing SAR ADC performance, offering a promising alternative that combines enhanced precision with operational simplicity and efficiency.

Table 2. Comparison designs of SAR ADC

Specification (Unit)	[20]	[21]	[22]	[23]	[24]	This work
Year	2019	2018	2022	2018	2022	2023
Architecture	SAR	SAR	SAR	SAR	SAR	SAR
Process technology (nm)	65	65	65	180	65	180
Resolution (bit)	13	11	10	10	14	8
Sampling rate (S/s)	20M	80M	1K	50K	20M	125K
Supply voltage (Volts)	0.6	1.2	0.2	0.6	1.2/3.3	1.2
DNL (LSB)	+0.72/-0.74	+1.66/-0.97	+0.46/-0.95	+0.65/-0.77	+0.88/-0.57	+0.6/-0.8
INL (LSB)	+1.31/-1.03	+0.97/-1.62	+2.54/-2.74	+0.89/-0.67	+0.9/-0.87	+0.4/-0.7

The comprehensive analysis of the proposed SAR ADC, guided by the innovative comparator, reveals a series of advancements. The critical examination extends to the comparison with conventional dynamic latch comparators, showcasing superior performance metrics in terms of latch time delay. The latch time delay is substantially reduced in our proposed design 159 ps compared to the conventional counterpart 983 ps.

The presented findings have far-reaching ramifications for the field of ADC technology. The reduction in time delay, enhanced precision, and lower power consumption contribute to the evolution of SAR ADCs. The design choices and innovations presented in this study pave the way for more efficient and high-performance ADCs in various applications, particularly in energy-efficient and time-sensitive systems. The proposed SAR ADC design and its comparator offer a promising avenue for future research and practical applications. The efficiency gains in power consumption and response time are particularly valuable for the development of ADCs in emerging technologies, where energy efficiency is crucial. The innovative features introduced in this work serve as a benchmark for researchers and engineers seeking optimized ADC solutions, indicating a direction for future advancements in precision analog-to-digital conversion.

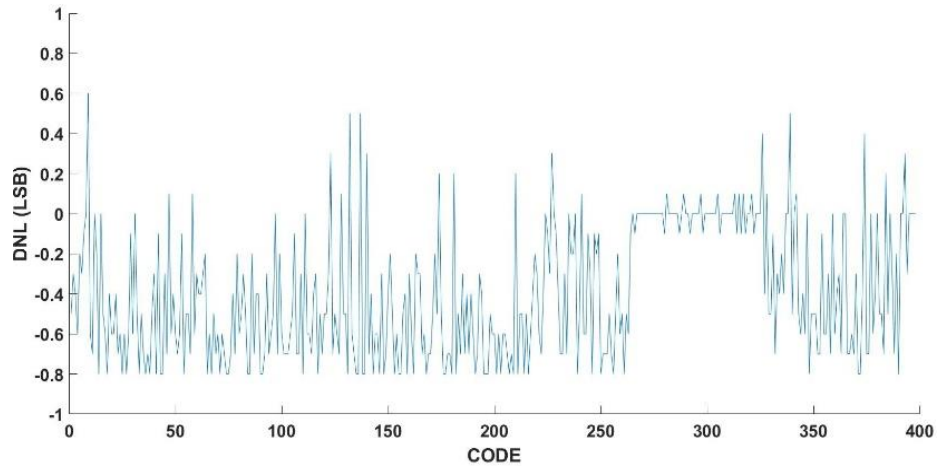


Figure 30. DNL of the SAR ADC

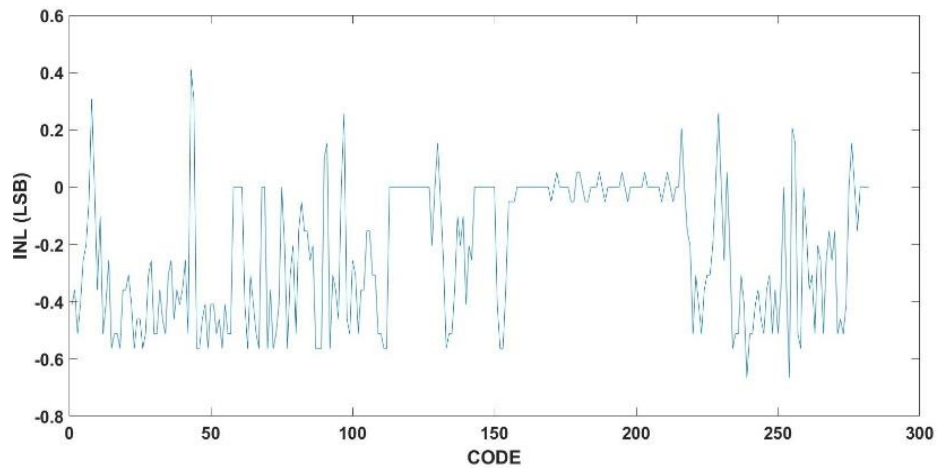


Figure 31. INL of the SAR ADC

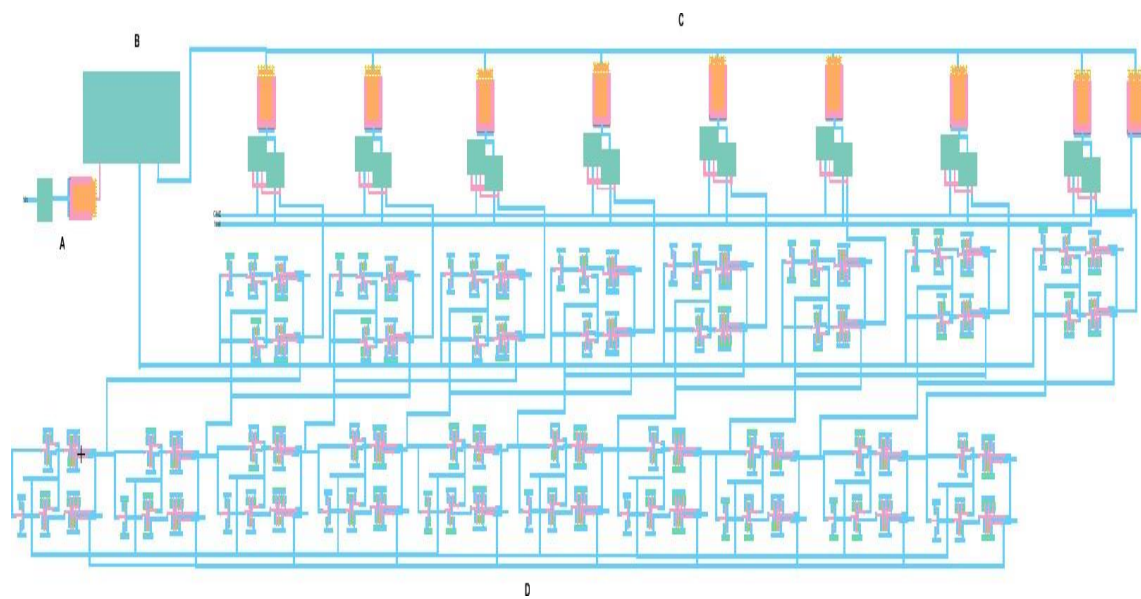


Figure 32. Layout for the SAR ADC

4. CONCLUSION

The presented SAR ADC, complemented by a novel comparator design, demonstrates notable improvements in response time, conversion times, power consumption, and accuracy. Upon thorough analysis, our findings suggest that our design offers advantages over existing solutions, providing a viable option for high-speed, high-accuracy applications. The reduction in response time by 37% and the achievement of lower power consumption at 9.2 mW with a 1.2 V supply voltage presents practical benefits for energy-efficient and time-sensitive systems. In comparison to conventional dynamic latched comparators, our proposed approach indicates promising performance metrics, suggesting potential efficacy in real-world applications. The Monte-Carlo simulations, yielding DNL and INL errors of +0.6/-0.8 and +0.4/-0.7 respectively at a sampling rate of 125 kS/s. Respectively, point towards the reliability of our design. Looking ahead, our findings hold implications for the future of ADC technology. Our research modestly contributes to the evolution of SAR ADCs, paving the way for enhanced designs that strike a balance between speed, accuracy, and power efficiency. The novel comparator design introduced here offers a starting point for further investigations by researchers and engineers seeking optimized ADC solutions. The insights derived from this study, while contributing to the current understanding, lay a foundation for potential future innovations, with potential applications in diverse fields.




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BIOGRAPHIES OF AUTHORS






Fadi Nessir Zghoul    received M.S. and Ph.D. degrees in electrical engineering from University of Idaho, Idaho, USA, in 2003, 2007 respectively. In 2007, he joined the Hashimite University, Jordan, as an assistant professor. After that he joined Yarmouk University, Jordan, in 2008, also as an assistant professor. In 2009, he has been appointed as the dean assistant at Hijjawi Faculty for Engineering Technology at Yarmouk University, Irbid, Jordan. Since 2010 he has been an associate professor at Jordan University for Science and Technology. In 2014, he has been appointed as the dean assistant at the Faculty of Engineering at the Jordan University for Science and Technology, Irbid, Jordan. In 2019 he spent one academic year at the University of Texas, Austin as a visiting scholar, sponsored by Fulbright. His current research interests include mixed signal circuit design, power management systems, and improving simulation techniques for nonlinear circuits. He can be contacted at email: FRNessirZghoul@just.edu.jo.






Yusra Hussein Al-Bakrawi    received B.C., and M.S. degrees in electrical engineering/power and control from Jordan University of Science and Technology, Jordan, in 2014, and 2023 respectively. Her current research interests include electrical circuit design, electric circuit analysis, and electronic circuit design. She can be contacted at email: yhalbakrawi19@eng.just.edu.jo.



Issa Etier    is currently working as a professor in the Electrical Engineering Department at Hashemite University. He joined the Electrical Engineering Department in 2005. He has 18 years of teaching/research experience. He received his master's and PhD Degrees in electrical engineering from Institute of Energy and Automation Technology from T.U. Berlin in 1996 and 2005, respectively. 2014-2015 Chair and establishment of the Department of Energy Engineering at the Zarqa University. 2019-2020 associate professor in the Department of Electrical Engineering, Faculty of Engineering, King Abdulaziz University, KSA. His research interests include power systems, renewable energy systems, energy conversion, and photovoltaic systems. He has 44 research papers in the reputed international journals and conferences. He can be contacted at email: etier@hu.edu.jo.



Nithiyananthan Kannan    is currently working as a professor in the Department of Electrical Engineering, Faculty of Engineering, King Abdulaziz University, Rabigh branch, KSA. He has 23 years of teaching/research experience. He completed his Ph.D. in the area of Power system engineering from the College of Engineering Guindy campus, Anna University, India in the year 2004. He had published books in the area of electrical and electrical engineering. His area of interest is computer applications for online power system analysis and modeling of power systems. He published more than 90 research papers in the reputed international journals. He can be contacted at email: nmajaknap@kau.edu.sa.