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An on-chip soft-start pseudo-current hysteresis-controlled buck converter for automotive applications

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ABSTRACT

This paper introduces a novel direct current to direct current (DC-DC) buck converter that uses a pseudo-current hysteresis controller and an on-chip soft start circuit for improved transient performance in automotive applications. The proposed converter, implemented with Taiwan semiconductor manufacturing company (TSMC) 0.18 µm complementary metal oxide semiconductor (CMOS) one-poly-six-metal (1P6M) technology, includes a rail-to-rail current detection circuit and an on-chip soft start circuit to handle transient responses and improve efficiency. Transient response analysis shows fast settling times of 28 µs for both load current changes from 100 mA to 1 A and reversals with consistent transient voltages of approximately 190 mV and peak power efficiency of 99.32% at 5 V output voltage and 100 mA load current. Additionally, the converter maintains a constant output voltage of approximately 5 V across the entire load current range with an average accuracy of 90.41%. A comparative analysis with previous work shows superior performance in terms of figure of merit (FOM). Overall, the proposed pseudo-current hysteresis controlled buck converter exhibits remarkable transient response, load regulation and power efficiency, positioning it as a promising solution for demanding applications, particularly in automotive systems where precise voltage regulation is crucial.

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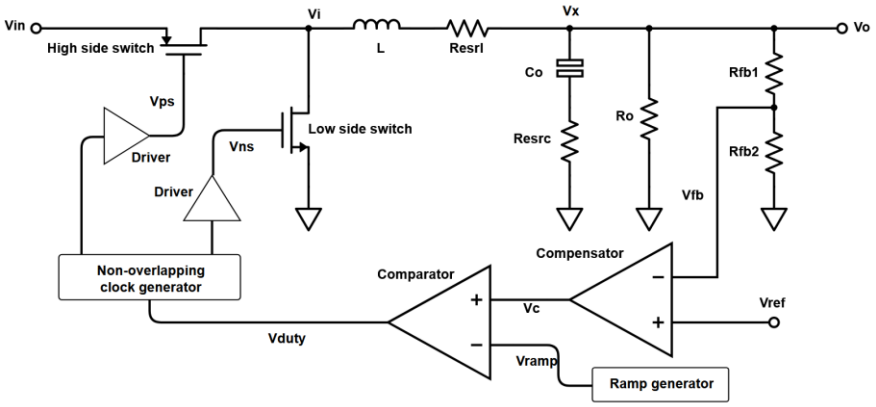
1. INTRODUCTION

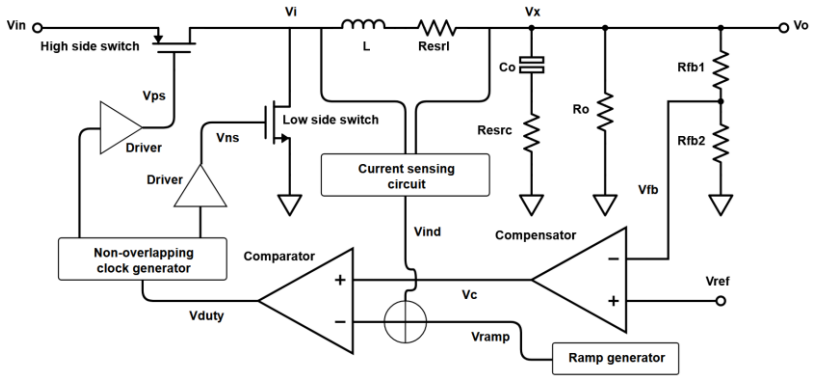
Given the rapid advancement of portable electronics devices and the automotive industry's drive for energy efficiency, power management systems are essential. Requirements for these systems include reducing design complexity, reducing costs, increasing conversion efficiency, and achieving fast transient responses in energy management systems [1]–[3]. Direct current to direct current (DC-DC) converters come in two main varieties: switching and linear. Despite their simplicity, linear converters are not suitable for high-power applications due to their low efficiency. Conversely, switching converters provide better efficiency and can handle higher power levels because [4]. Modern electronic products and automotive electric vehicles have come to rely heavily on the DC-DC switching power supplies [5]–[14]. These include the buck converter, which uses a feedback system to control its output voltage and is known to effectively step down the direct current voltage while minimizing power loss [15]–[17]. The main methods that DC-DC power converters typically use to regulate the output voltage are voltage mode control and current mode

control, as shown in Figures 1(a) and 1(b). In voltage mode control, the reference voltage V_{ref} is compared to the power stage's scaled output voltage V_{fb} to generate a compensation voltage V_c through a compensator. This ensures precise maintenance of the regulated power stage's output voltage by the voltage mode controller [18]. A ramp generator circuit creates a sawtooth signal V_{ramp}, which, compared with the error voltage V_c through a comparator. This generates a clock signal, V_{duty}, controlling the switching of power transistors with a suitable duty cycle to compensate for the voltage gap between the targeted and actual output voltage of the power converter. Current mode control involves a current-sensing loop passing through the inductor, allowing quick transient response and accurate output voltage regulation. Although, duty cycles exceeding 50% may lead to sub-harmonic oscillations [19], [20]. Addressing this issue, several trans-conductance compensation techniques based implementations have been suggested, although with increased circuit complexity [21]. During start-up, the error amplifier becomes unbalanced due to the fully discharged output capacitor, and the voltage gap between the feedback and reference voltages is quite large. Consequently, this leads to a nearly 100% duty ratio of the created pulse-width-modulation (PWM) signal [22]. Therefore, it is possible that the inductor current will be higher than the equilibrium value. We call this strong current inrush current. The inductor's current exceeds the allowable maximum current limit for a brief time because it cannot change instantly. This is called “overshoot” [23] and results in an abrupt rise in the output voltage above the desirable value. By providing a reference voltage in a staircase-type form, the duty cycle gradually decreases to the appropriate ratio, minimizing output voltage overshoot and maintaining the inductor current within permissible limits during the starting phase [24]. Soft-start circuits have gradually become an essential part of modern power supply designs due to their ability to limit inrush currents and protect electronic systems during transient starts. Various soft-start methods have been developed [22]–[28], such as duty cycle-based soft-start circuits. This method causes the error amplifier to suffer with a longer soft start time, which affects the load on the controller.

$$V_{fb} = \left(\frac{R_{fb2}}{R_{fb1}+R_{fb2}}\right) \times V_o \quad (1)$$



(a)



(b)

Figure 1. Major types of control implementations (a) voltage mode and (b) current mode

Regardless of the control method employed, usage and environmental factors impact the power management integrated circuits (PMICs) performance. PMICs are subject to load fluctuations, that result in transient voltages during the transient time needed for the output voltage to stabilize within the transient range. Overshoot voltage may give rise to high currents, posing chip damage risks, whereas undershoot voltage could result in significant power loss. For optimal converter performance, it is critical to keep the transient voltage within an appropriate range relative to the circuit supply voltage. Transient time and transient voltage serve as critical indicators for PMICs [29], [30]. This study presents a buck converter that uses a pseudo-current hysteresis controller, allowing a rapid response to load changes, thus providing the possibility of a fast transient response [31]. In addition, the incorporation of an efficient, low-power on-chip soft start circuit limits the inductor current, mitigating over-voltage and over-current damage while maintaining efficiency during the start-up phase of the buck converter to prevent inrush voltage overshoot and saving power after the start-up phase is completed.

The upcoming sections of this work are organized as follows: section 2 deals with the proposed buck converter architecture and describes the operating modes and circuit implementation of the different blocks in detail. Section 3 provides simulation results and stimulates a comprehensive discussion, culminating in section 4 with concluding remarks and implications. The aim of this research is to overcome the limitations of traditional control techniques and meet the requirements for highly efficient, stable and responsive energy management systems in modern automotive applications. The aim is also to stimulate innovative strategies such as pseudo-current hysteresis control while integrating advanced features such as a power-saving soft-start circuit on the chip.

2. METHOD

The proposed buck converter architecture and pseudo-current hysteresis controller are shown in Figure 2 [32], [33], and include driver circuits, a non-overlapping clock generator, a soft start circuit, a current sensor, and a hysteresis voltage controller. The loop response prevents the output from being established instantly during the initial start-up phase of the DC-DC power converter, necessitating loop operation at 100% duty cycle. As a result, both the output voltage and the inductor current may exceed their specified limits. The power switches of the buck converter are controlled by a clock signal via a soft-start circuit, which reduces overshoot. Equation (1) calculates the feedback voltage V_{fb} by scaling the output voltage V_o with the resistors R_{fb1} and R_{fb2}. To save energy, the soft start circuit should be turned off when the error signal V_c approaches the desired reference value V_{ref}. To enable the soft start circuit during the start-up phase of the power stage.

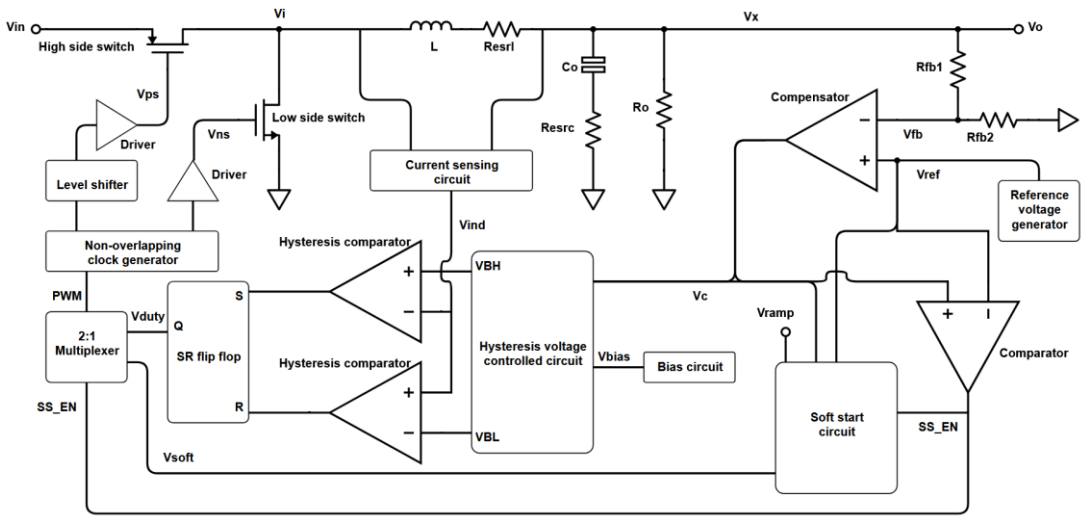


Figure 2. Proposed PCHC with on-chip soft-start buck converter

As shown in Figure 3(a), a comparator is used to generate a voltage signal SS_EN by comparing the voltage levels of V_c and V_{ref} for this function. When V_c falls below V_{ref} during the start-up phase, the comparator generates a low voltage level, enabling the soft-start circuit and selecting the soft-start switching

clock to drive the power stage switches via a 2:1 multiplexer. When V_c exceeds V_{ref} at the end of the start-up phase, the signal SS_EN changes from low to high. The soft-start circuit will be deactivated, and the current-mode PWM switching clock will be used to drive the power stage switches via the multiplexer. Figure 3(b) shows the implementation of the multiplexer circuit. The transient waveforms of the power-saving circuit and multiplexer operation are shown in Figure 3(c). When the power stage's start-up phase is complete, the compensator generates a voltage V_c to compensate. This voltage is determined by comparing the reference voltage and the feedback voltage. The hysteresis controller is biased by a voltage bias to match the compensation voltage V_c in order to create lower and upper voltage limits, referred to as V_{BH} and V_{BL}, which follow the compensation voltage. The inductor current is directly sensed by a current sensor, which delivers a voltage signal V_{ind} to the hysteresis-controlled circuit via a rail-to-rail operational trans-conductance amplifier (OTA), constituting the pseudo-current hysteresis-controlled method (PCHC) [34]. By comparing V_{ind} with the limit voltages, the appropriate duty cycle is determined and then supplied to the non-overlapping clock generator circuit, with V_{duty} interleaved to separate the on-times of the two power switches with proper dead time.

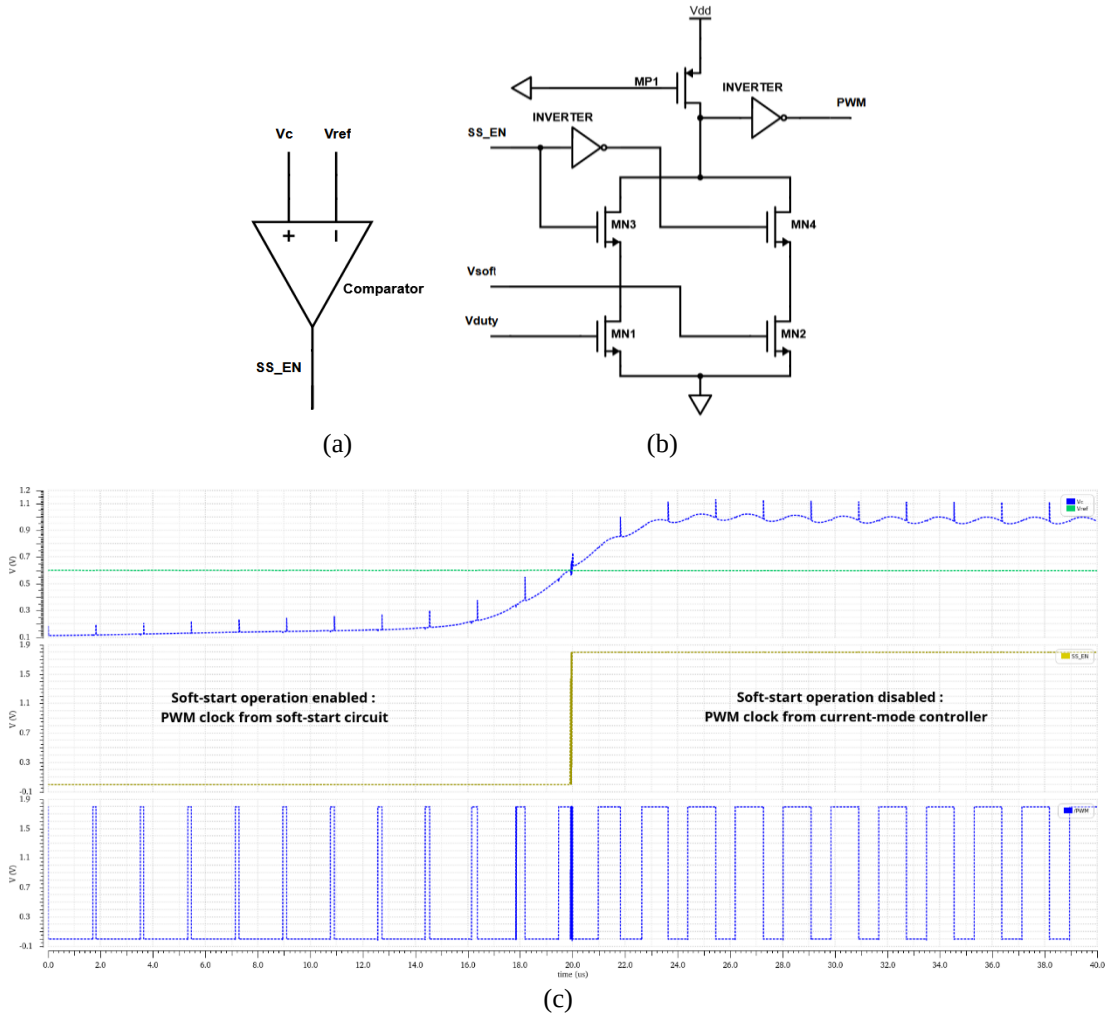
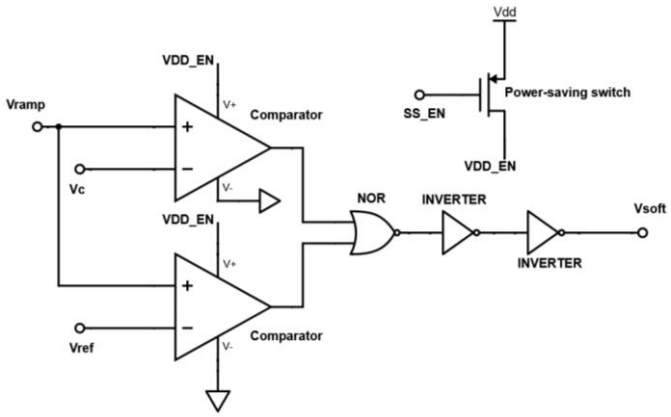


Figure 3. Circuit implementation of (a) soft-start detection comparator and (b) multiplexer and (c) the corresponding transient waveforms

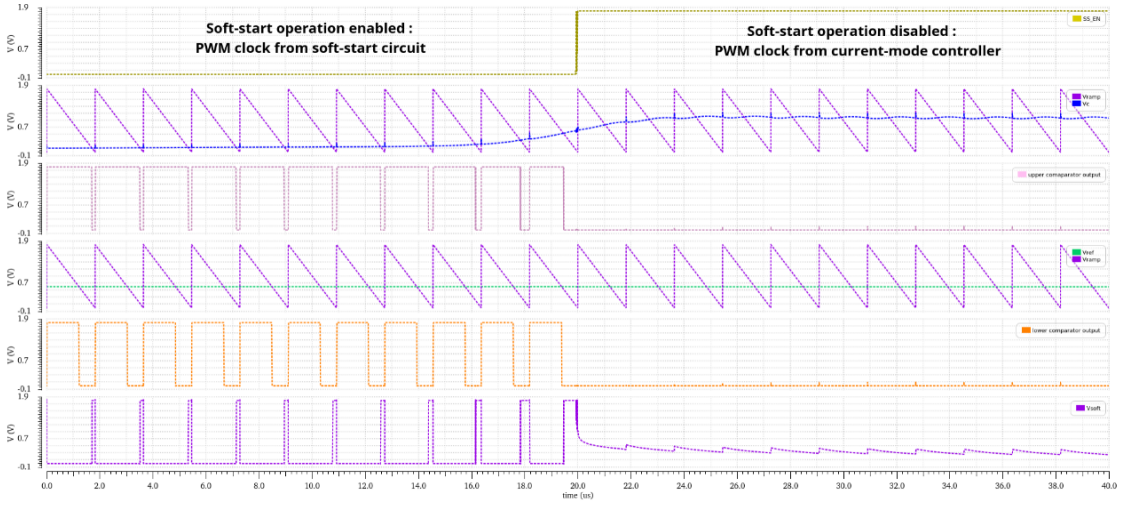
2.1. Soft-start circuit

To overcome the inrush current problem and protect electronic systems during transient start-up, an on-chip soft start circuit is used. Figure 4(a) shows the circuit implementation. This circuit consists of two comparators that serve to limit the peak current and avoid surge currents to achieve an almost linear increase in the voltage signal. This can be achieved by comparing a ramp signal, V_{ramp}, with the error signal from the

compensation circuit. Meanwhile, a second comparator, illustrated in Figure 4(b), compares V_{ramp} with the reference voltage, V_{ref}, and produces a clock signal, V_{soft}, with a decreasing duty cycle whenever the error signal, V_c, increases. Concurrently, by adjusting the size of the high-side power transistor, the maximum values of the output voltage and inductor current are restricted. For power-saving reasons, the soft start circuit should be switched off as soon as the error signal V_c reaches the desired reference value V_{ref}. Therefore, a p-channel transistor-based power-saving switch is integrated, allowing the soft start circuit to function solely during the power stage's start phase and in accordance with the logic level of the SS_EN signal. The soft start circuit is connected to the power supply during the starting phase, when V_c is less than V_{ref} and the comparator generates a low voltage level that activates the power-saving switch. When the start-up phase comes to an end, the comparator goes from low to high if V_c exceeds V_{ref}. This causes the power saving switch to become inactive. The power saving mode of the soft start circuit is then activated and the circuit is disconnected from the power supply.



(a)



(b)

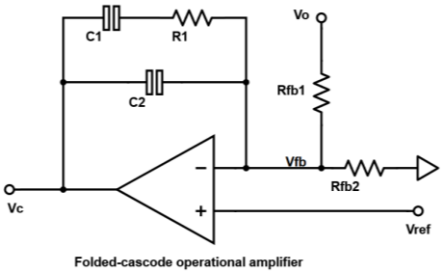
Figure 4. Circuit implementation of (a) soft-start and (b) the corresponding transient waveforms

2.2. Compensator circuit

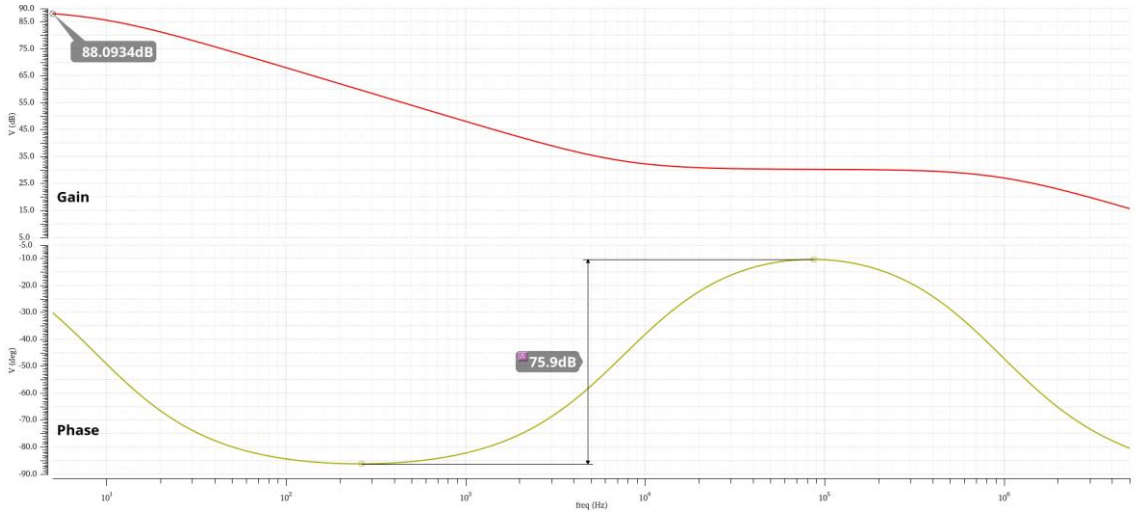
The Type II compensator circuit, which is crucial for control gain, phase margin and stability, consists of a folded cascode operational amplifier, resistors and a capacitor as illustrated in Figure 5(a). The reference voltage and the feedback path of the output voltage feed the compensator to generate a voltage compensation V_c. The Type II compensator supplies the system with two poles and a zero. Figure 5(b) shows the Bode graphs of the compensation components. The corresponding equations are contained in (2) and (3).

$$\left|\frac{V_c}{V_o}\right| = \frac{1+sC_1R_1}{sR_{fb1}(C_1+C_2)+s^2R_{fb1}C_1R_1C_2} \quad (2)$$

$$f_{z1} = \frac{1}{2\pi R_1 C_1} ; \; f_{p1} = \frac{1}{2\pi \times R_1 C_1 C_2/(C_1+C_2)} \quad (3)$$



(a)



(b)

Figure 5. Implementation of type II compensation (a) circuit and (b) Bode diagram

2.3. Rail-to-rail current sensing circuit

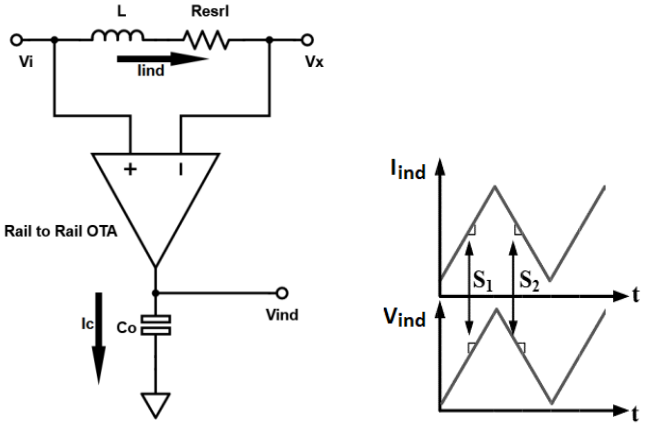
Inductor current detection is accomplished as presented in Figure 6(a), using a rail-to-rail current sensor placed between V_i and V_x with the inductor in parallel [35]. Using voltage-current characteristic of the rail-to-rail operational transconductance amplifier, a current I_c is generated. As illustrated in Figure 6(b), the voltage signal V_{ind} is generated by the integration of the current I_c through the capacitor C_c to feed the following level control circuit and has a slope analogous to the inductor current. Through the use of this architecture, the transient response and stability of the presented converter can be accelerated under changing load conditions. Equations (4) and (5) define the expressions for the current I_c and the voltage V_{ind}. Figure 7 presents the used rail-to-rail OTA. This circuit achieves improved input voltage range. It is therefore no longer necessary to use the usual external resistors for this purpose. By combining a P-type and an N-type OTA, the functionality of the rail-to-rail OTA is increased. Equations (6) and (7) are the corresponding equations. Compared to a folded cascode op-amp, this rail-to-rail OTA has a smaller gain, but it also uses less power and has a wider bandwidth.

$$I_c = Gm \times (V_i - V_x) \quad (4)$$

$$V_{ind} = \frac{1}{C_c} \times \int I_c \, dt \quad (5)$$

$$Gm_N = gm_N \; ; \; Gm_P = gm_P \; ; \; Z_{out} = \frac{1}{sC_c} \quad (6)$$

$$A_v = Gm \times Z_{out} = \frac{gm_N + gm_P}{sC_c} \quad (7)$$



(a) (b)

Figure 6. Inductor current sense (a) circuit and (b) signals

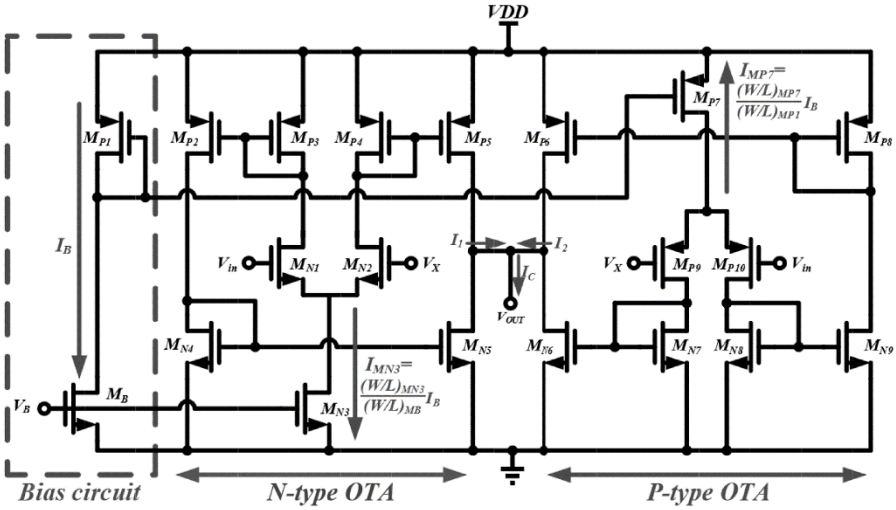


Figure 7. Rail-to-rail OTA circuit

2.4. Hysteresis-controlled circuit

The hysteresis-controlled circuit shown in Figure 8(a) uses a bias voltage V_{bias} matched to the compensator's output voltage V_c to control its transistors current. A hysteresis comparator compares the upper and lower limit voltages V_{BH} and V_{BL} formed by the resistors R_{BH} and R_{BL} with the voltage signal V_{ind}. To change the duty cycle, the comparison signal is received from the set-reset (SR) flip-flop. Figure 8(b) shows the transient waveforms of the voltage-controlled hysteresis circuit. A key component of the hysteresis controller circuit is the hysteresis comparator, shown in Figure 9. The corresponding is represented by (8) and (9).

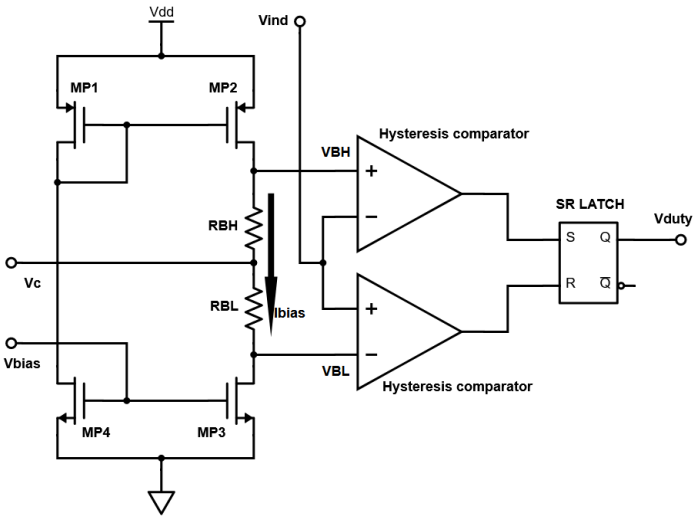
$$V_{BH} = V_c + I_{bias} \times R_{BH} \;\; ; \;\; V_{BL} = V_c - I_{bias} \times R_{BL} \tag{8}$$

$$\Delta V = V_{BH} - V_{BL} \tag{9}$$

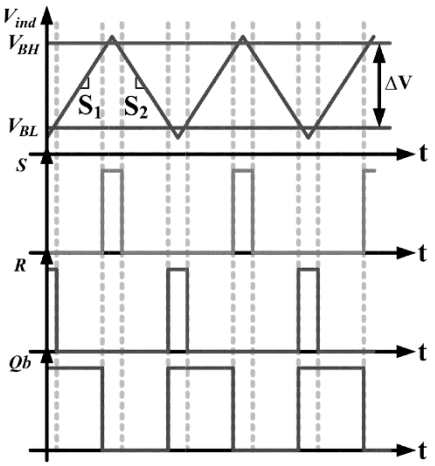
2.5. Non-overlapping clocks generator and driver circuits

The circuit depicted in Figure 10 serves as a non-overlapping clock generator, and its main purpose is to prevent the power switches from being switched at the same time. Such simultaneous switching could result in a short circuit between the voltage source and ground. To ensure that the system operates properly, a delay circuit is used to manage the dead time between switching events. The resulting clocks drive the power switches via the drivers to achieve the buck effect [36]. The driver circuit, depicted in Figure 11, generates

V_{PS} and V_{NS} to drive the excessive gate capacitance induced by the size of the power switches. This circuit is necessary to manage the large currents and low on-resistance required by the buck converter's switching transistors and improve overall efficiency [37], [38].



(a)



(b)

Figure 8. Hysteresis-voltage control (a) circuit and (b) signals

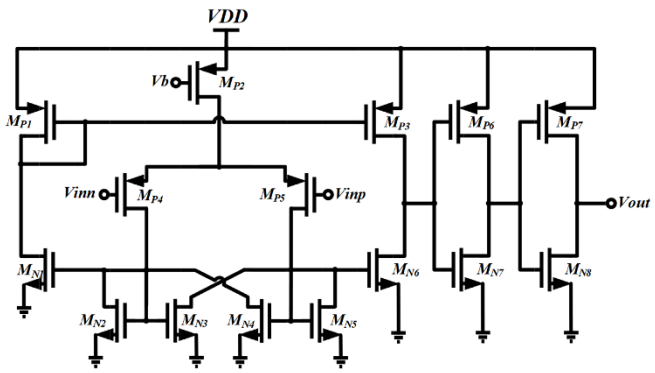


Figure 9. Hysteretic comparator

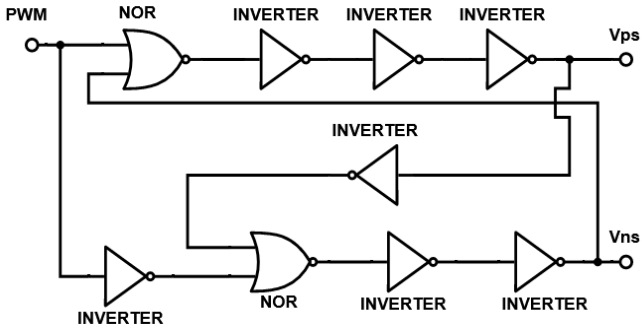


Figure 10. Non-overlapping clocks generator circuit

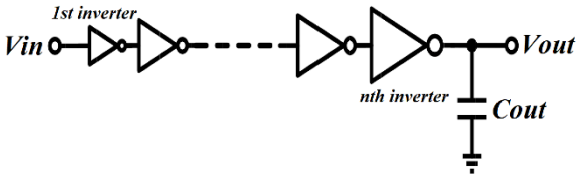
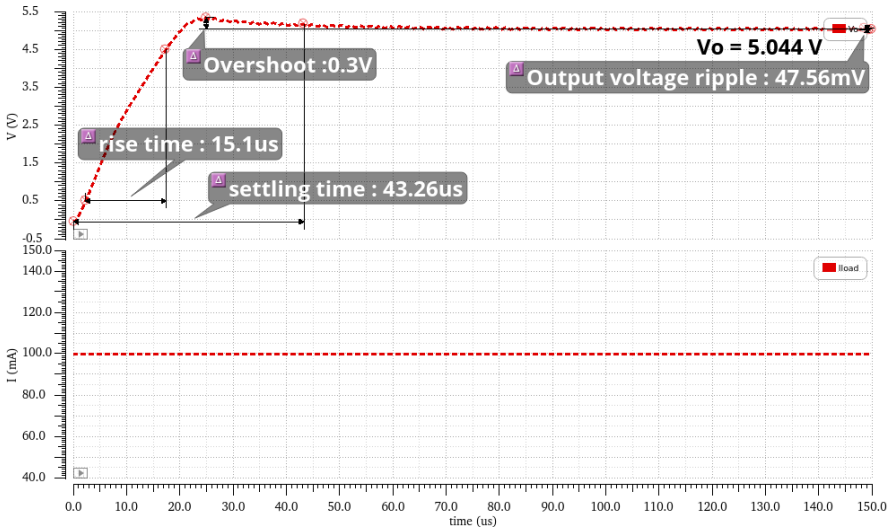


Figure 11. Driver circuit

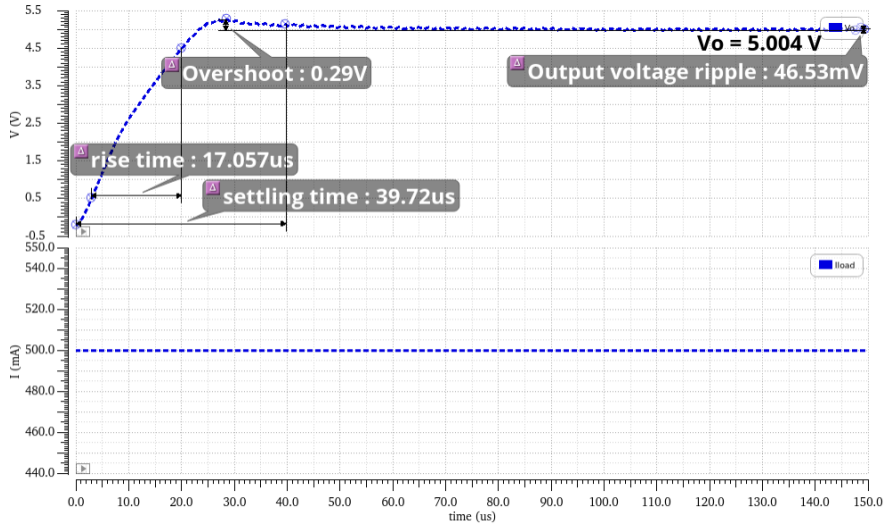
3. RESULTS AND DISCUSSION

The PCHC buck power converter was realized with Taiwan semiconductor manufacturing company (TSMC) 0.18 µm complementary metal oxide semiconductor (CMOS) one-poly-six-metal (1P6M) technology. This in-depth analysis compares the converter's transient response, load control, power efficiency, and performance to its predecessors. The converter's transient response is critical for its capacity to handle dynamic load variations. Figure 12 shows the output voltage transient responses obtained using the analog design environment (ADE) simulator in Cadence Virtuoso software for an input voltage of 12 V and load currents of 100 mA, 500 mA, and 1 A, respectively. These results show that the converter maintains a consistent output voltage of roughly 5 V with a low ripple voltage V_{ripple} of less than 47.56 mV across all load currents. Figure 12(a) depicts the system's output voltage transient response with a load current of 100 mA. With a rising time of 15.079 µs and an output voltage ripple of 47.56 mV, the output voltage settles to its steady state value of 5.044 V in 43.26 µs. There is an overshoot at the output voltage of 300 mV at the start. The system's efficiency was 99.32%. Figure 12(b) depicts the system's output voltage response with a load current of 500 mA. With a rising time of 17.57 µs and an output voltage ripple of 46.53 mV, the output voltage settles to its regulated value of 5.004 V in 39.72 µs. During the initial start, the output voltage overshoots by 260 mV. The system's efficiency was 86.04%. Figure 12(c) depicts the system's output voltage response with a load current of 1 A. With a rising time of 20.66 µs and an output voltage ripple of 44.51 mV, the output voltage settles to its regulated value of 4.96 V in 41.66 µs. During the start-up phase, there is a 190 mV overshoot. The system's efficiency was 78.17%. A closer look of the transient responses during load fluctuations, as shown in Figure 13, reveals the converter's quick recovery. The output voltage settles in 28 µs for a 100 mA to 1A step load current change with a 190 mV undershoot. Reversely, the output voltage settles in 28 µs with 180 mV overshoot when changing the load current from 1 A to 100 mA.

Load regulation is a key indicator of the converter's stability under varying load conditions. The resulting output voltage is extremely close to the target output voltage. At a load current of 100 mA, the steady-state error is -44 mV, while at a load current of 500 mA, the steady-state error is -4 mV. At 1 A load current, the steady-state error is 40mV. Thus, the output error voltage remains below 84 mV as the load current ranges from 100 mA to 1 A, as shown in Figure 14. According to these results, the average accuracy is 99.41%. In addition, the load regulation rate is 1.87%/A. The proposed converter power efficiency at various load currents is depicted in Figure 15. Notably, the peak power efficiency reaches 99.32% at 5 V output voltage and 100 mA load current. A comprehensive comparison with previous works, as summarized in Table 1, demonstrates that the proposed buck power converter outperforms other designs in terms of the figure of merit (FOM) as written in (10), with an accurate transient response with minimal overshoot, undershoot, and rapid recovery, validating the effectiveness of the pseudo-current hysteresis control, especially when combined with the soft start circuit.



(a)



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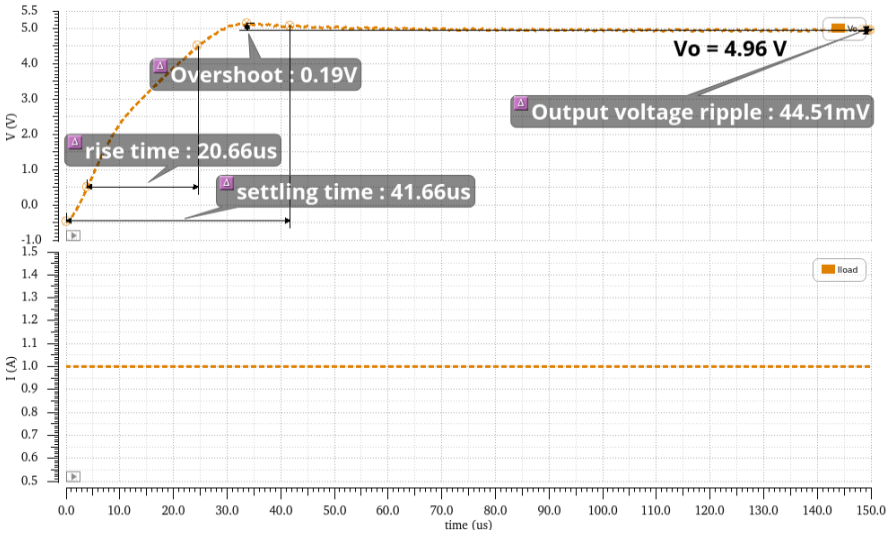

(c)

Figure 12. Transient response under load currents (a) 100 mA (b) 500 mA and (c) 1 A

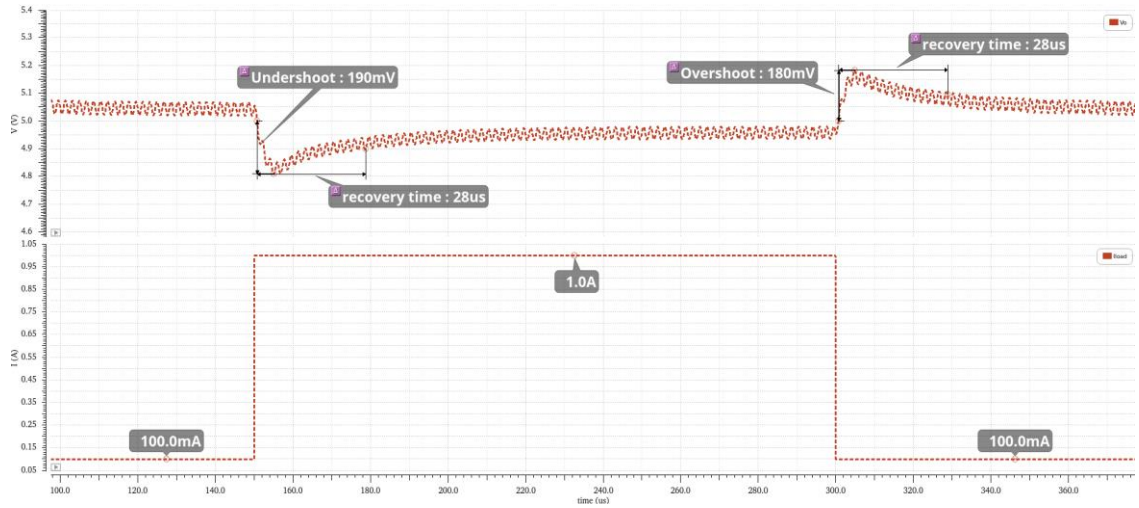

Figure 13. Transient response to step load current change from 100 mA to 1 A and back to 100 mA

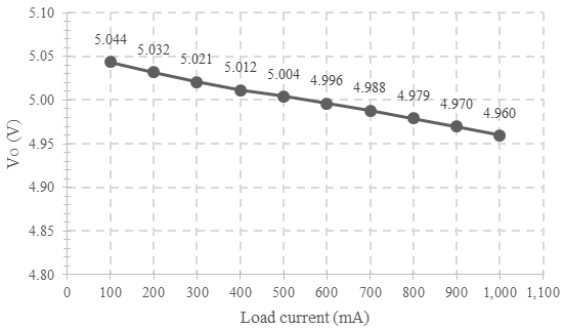

Figure 14. Load regulation

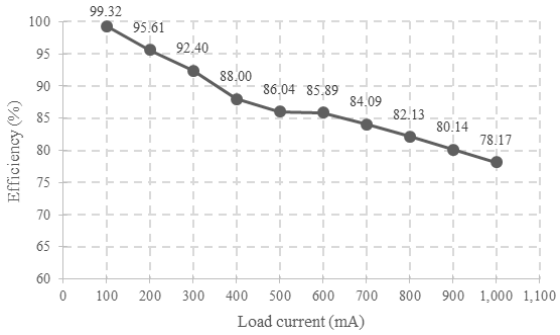

Figure 15. Efficiency through load current range

$$FOM = \frac{Step\ Load\ Change\ (mA) \times Peak\ Efficiency\ (\%)}{Max.\ Transient\ Response\ (\mu s) \times Max.\ Transient\ Voltage(mV)} \times 10^{-2} \quad (10)$$

Table 1. The comparison of the performance of the proposed buck converter with previous works

References		[39]	[40]	[41]	[42]	[43]	This work
Input voltage range		14 V	12 V	12 V	12 V	12 V	12 V
Output voltage		6 V	5 V	5 V	5 V	3.3 V	5 V
Load current range		240 mA – 1.2 A	1 A – 2 A	400 mA – 2 A	1 A – 2 A	0 A – 18 A	100 mA – 1 A
Switching frequency		N/A	400 kHz	100 kHz	400 kHz	267 kHz	550 kHz
Inductor		N/A	12 µH	72 uH	12 uH	1 uH	2 µH
Capacitor		N/A	10µF	10 uF	10 uF	330uF	12µF
Maximum overshoot at start-up phase		N/A	0 V	750 mV	315 mV	40 mV	300 mV
Maximum steady-state error		70 mV	10 mV	70 mV	20 mV	N/A	44 mV
Step load change		960 mA	1 A	1.6 A	1 A	18 A	900 mA
Transient response	Light to heavy	5 ms	1 ms	N/A	N/A	80 us	28 µs
Transient response	Heavy to light	5 ms	N/A	500 us	200 us	80 us	28 µs
Transient voltage	Undershoot	600 mV	700 mV	N/A	N/A	233 mV	190 mV
Transient voltage	Overshoot	600 mV	N/A	300 mV	380 mV	233 mV	180 mV
Peak efficiency		98.83%	99.83%	99.29%	99.61%	98.48%	99.32%
FOM		0.0003	0.0014	0.0106	0.013	0.095	0.168

4. CONCLUSION

The application of pseudo-current hysteresis-controlled techniques has led to the development of an enhanced buck power converter with notable advantages in transient voltage suppression and rapid transient response. Utilizing TSMC 0.18 µm CMOS 1P6M technology, the designed buck converter incorporates both pseudo-current hysteresis control and a soft-start circuit, leading to significant improvements in transient

performance. The observed transient times during load transitions, from 100 mA to 1 A and back to 100 mA, is 28 µs which is impressively short compared to previous works, with consistent transient voltages of around 190 mV. Moreover, the buck converter achieves a peak power efficiency of 99.32%. These findings underscore the effectiveness of the proposed DC-DC buck converter, demonstrating its capability to maintain the output voltage value across the given load current range, with an average accuracy of 99.41%. The chip area is an aspect that should be taken care of in future studies. It may be possible to conduct designing the converter at the layout level in TSMC 0.18 µm CMOS 1P6M technology to determine the full chip area.

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