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Design and implementation of a low-cost circuit for medium-speed flash analog to digital conversions

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ABSTRACT

Despite the considerable advancements in analog-to-digital conversion (ADC) circuits, many papers neglect several crucial considerations: Firstly, it does not ensure that ADCs work well in the software or hardware. Secondly, it is not certain that ADCs have a wide range of amplitude responses for the input voltages to be convenient in many applications, especially in electronics, communications, computer vision, CubeSat circuits, and subsystems. Finally, many of these ADCs need to look at the suitability of the proposed circuit to the most extensive range of frequencies. In this paper, a design of a low-cost circuit is proposed for medium-speed flash ADCs. The proposed circuit is simulated based on a set of electronic components with specific values to achieve high stability operation for a wide range of frequencies and voltages, whether in software or hardware. This circuit is practically implemented and experimentally tested. The proposed design aims to achieve high efficiency in the sampling process over a range of amplitudes from 10 mV to 10 V. The proposed circuit operates at a bandwidth of frequencies from 0 Hz to greater than 10 kHz in the simulation and hardware implementation.

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1. INTRODUCTION

Nowadays, the trend of industrial electronics [1] tends to monitor, sense, and control everything around us. Because of significant advances in digital signal processing and its many applications [2]–[11] [12], improving the design of analog-to-digital converters (ADC) [13]–[16] is a priority for the scientific community. The output from the attitude determination and control subsystem (ADCS), the CPU's temperature reading, and the payload output of CubeSats will all be sampled using the ADC. A truly digital signal has two primary advantages. First, the signal changes at discrete time intervals. Second, the amplitude changes in discrete values; the signal can only contain certain finite values at specific times. In turn, the analog signal can change infinitely in time and amplitude. The amplitude values are innumerable, even within a specified analog signal range. Hence, two main steps should be achieved to implement the conversion from an analog signal to a digital signal. The first step is sampling [17], [18], which converts the analog signal into continuous values at discrete times.

The second step is the quantization process [19], [20], which is dedicated to making it discrete in amplitude. Moreover, it is essential to improve analog to digital conversion techniques. However, there are three problems with these techniques; the first problem is that there needs to be a guarantee that ADCs work well, whether in the software or hardware. The second problem is that it needs to ensure that the ADCs have a wide range of amplitude responses for the input voltages to be suited in many applications. The last problem that many of these ADCs overlooked was the suitability of the proposed circuit to the most extensive range of frequencies, "wide frequency response".

The paper's primary goal is to solve the three problems mentioned above. In this paper, a simulation design and hardware implementation of a low-cost circuit for medium speed (ADCs) is developed. The proposed circuit is experimentally implemented and tested based on a set of electronic components that have suitable values to achieve the required design. The proposed design includes an adaptive amplifier controlled with adapted voltage gain Av to expand the analog input signal amplitude range. The design also includes a crystal oscillator operating at a sampling rate of 11 MHz.

The paper is structured as follows: Section 2 presents the theoretical background for the analog-to-digital conversion process. Section 3 introduces the proposed design of the flash ADC. Section 4 discusses the simulation results and hardware implementation for testing the proposed design. Section 5 presents the conclusion and future work of the paper.

2. THE PROCESS OF ANALOG TO DIGITAL CONVERSION

Figure 1 shows the procedure of an analog to digital-conversion. The conversion flow starts with a filtering process, followed by three processes: sampling, quantizing, and encoding. The output of the sampling process is a discrete signal in the time domain, while the output of the quantizing process is still a signal with multi-level changes at specific intervals. The encoding process is to convert the quantizing output values to binary values. Figure 2 illustrates the output signal from each output stage for the ADC process. A continuous analog input signal is applied to a filter to prevent interference with other signals. The output of the filtering process is a smooth signal as input to the sampling process; the output signal from the sampling process is called a sampled signal, while the output from the quantizing process is called a quantized signal, while the output signal of the encoding process represented as a bit stream and is called a digital signal.

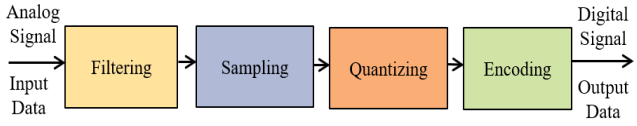


Figure 1. Analog to digital conversion process

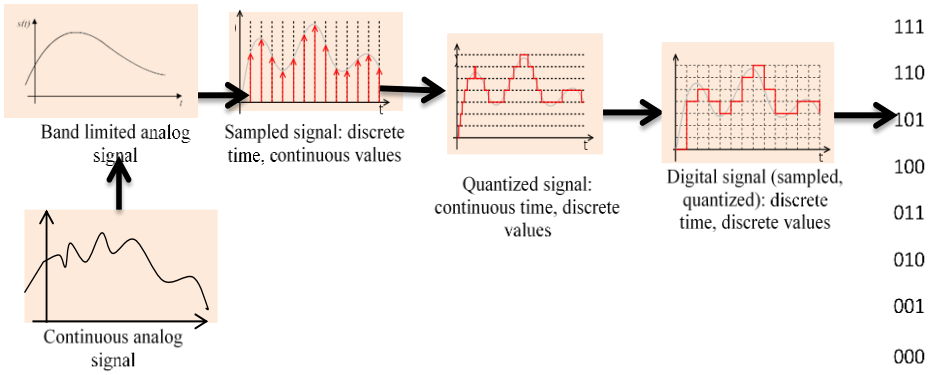


Figure 2. The output signal for each stage in the ADC's process

3. THE PROPOSED DESIGN OF THE FLASH ADC

Figure 3 demonstrates the circuit diagram of the proposed sampler technique of the flash ADC. It consists of three main parts: an adaptive amplifier, crystal oscillator with dynamic switch, and amplifier. In the following, an explanation of each of the three parts will be presented.

3.1. The sampler technique

Figure 3(a) shows that the sampler technique's adaptive amplifier has two magnification ranges based on whether the input voltage is very high or very low. In case the input voltage is very high, the adaptive amplifier automatically applies the extent of the magnification Av1. In case the input voltage is very low, the adaptive amplifier applies the extent of the magnification Av2 according to mathematical expressions (1) and (2) [21].

$$A_{V1} = \left(1 + \frac{R_4 + R_5}{R_6}\right) \quad (1)$$

$$A_{V2} = \left(1 + \frac{R_4}{R_6}\right) \quad (2)$$

The extent of the magnification of AV1 is greater than that of AV2 due to the presence of a resistance R5. An auxiliary circuit is developed for the sampling amplification circuit. This circuit separates and connects the resistance R5 based on the strength and weakness of the input signal. The auxiliary circuit consists of a step-up transformer and a transistor as a switch Q2 as in Figure 3(a); the transistor is connected in parallel with the resistance R5 as in Figure 3. An explanation of the theoretical operation of the adaptive amplifier is written in the following two points: The cut-off state of the transistor is realized when VB < 0.7 (OFF-stat) and at this case the step-up transformer is unable to sense the weak input signal so resistance R5 is conductive. The amplifier is working in a high range, according to Av1. The saturation state of the transistor is realized when VC < VE (ON-stat), and in this case, the step-up transformer can sense the strength input signal, so the resistance Rs is shorted and is not present, and the amplifier is working in a low range according to AV2.

3.2. The crystal oscillator with dynamic switch and second amplifier

As shown in Figures 3(b) and 3(c), the circuit's oscillation frequency is decided by the series resonant frequency of the crystal. The series resonant frequency, fs, occurs when the series capacitance CS resonates with the series inductance LS. At this stage, the crystal impedance will be the least; hence, the amount of feedback will be the largest. Mathematical expression for the same is given as [22].

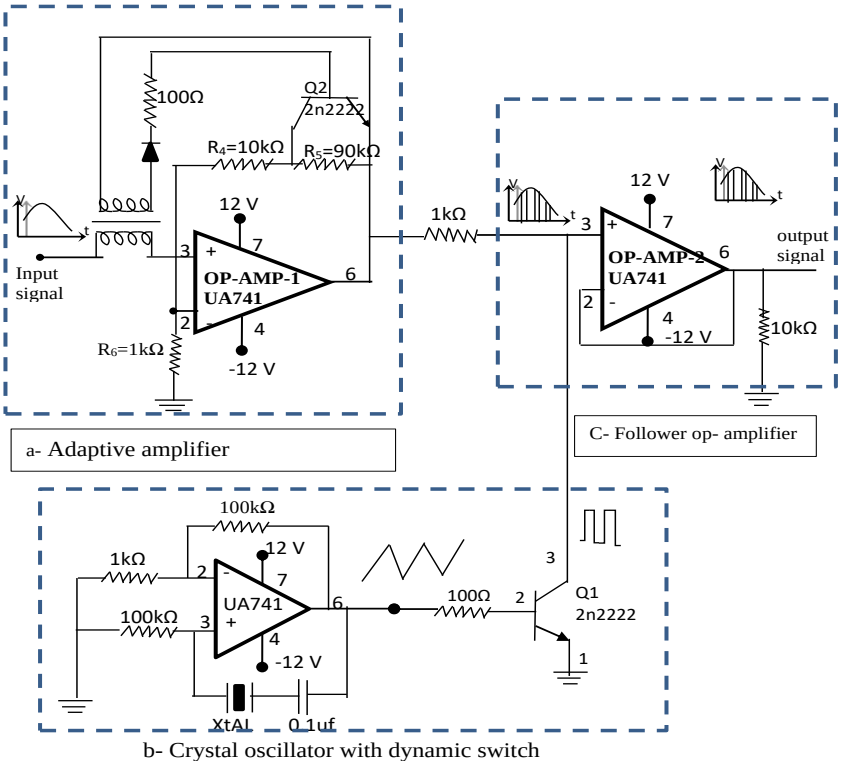


Figure 3. Circuit diagram of the sampler technique: (a) adaptive amplifier, (b) crystal oscillator with dynamic switch, and (c) follower op-amplifier

$$f_s = \frac{1}{2\pi\sqrt{L_s C_s}} \quad (3)$$

where Ls and Cs are the parameters of series circuit equivalent circuit of crystal oscillator [23] LS: A large-valued inductor, CS: A small-valued capacitor

The typical operating range of the crystal oscillators is from 40 kHz to 100 MHz wherein the low-frequency oscillators are designed using Op-Amps while the high-frequency ones are designed using transistors. The circuit includes a bipolar junction transistor Q1, which operates as a dynamic switch to organize the sampling frequency of the sampler. In this circuit, if the dynamic switch is closed "transistor ON", the input analog signal does not pass to the output of the second amplifier. When the switch is open, "transistor OFF", the input analog signal passes to the output of the follower operational amplifier.

3.3. Quantizer and encoder

Figure 4 shows the circuit diagram of the quantizer and encoder. The circuit consists of seven voltage comparators whose inverting inputs are connected to a voltage divider. These voltage comparators are operational amplifiers used without feedback [24].

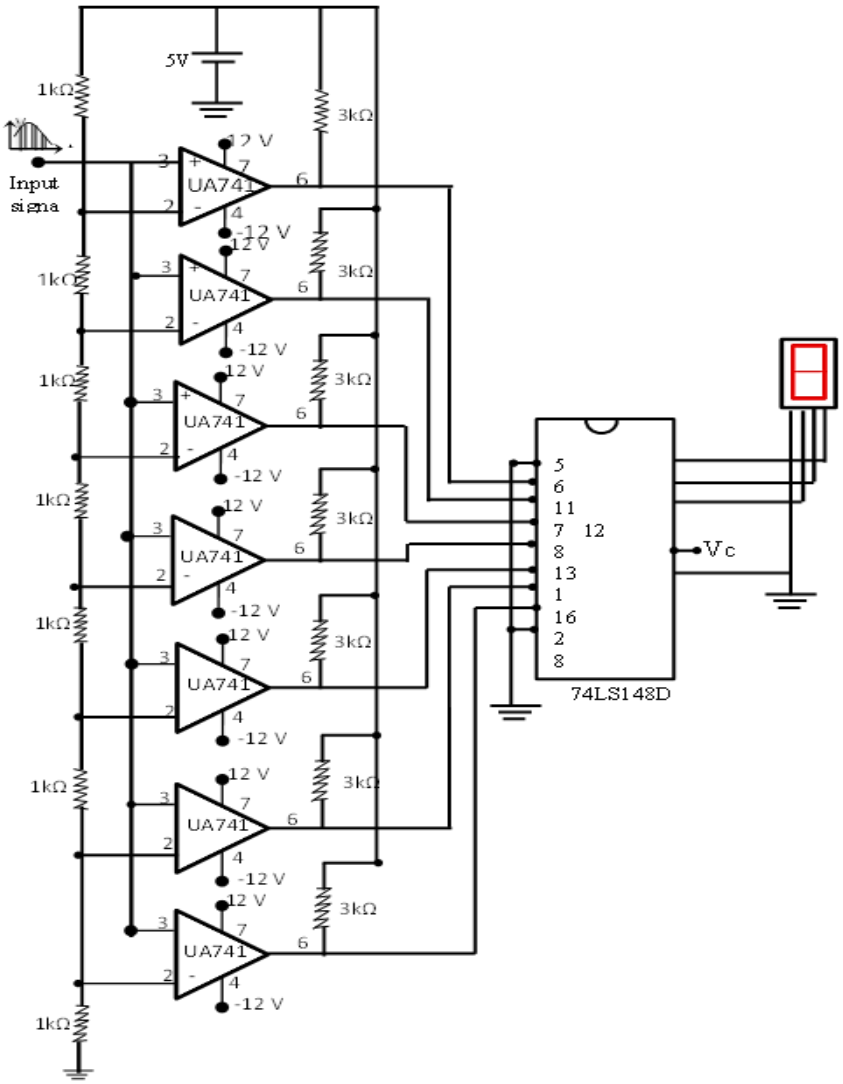


Figure 4. Circuit diagram of the quantizer and encoder

This figure calculates the number of comparators N using (4), where n is the resolution of the ADC, i.e., in this case, $n = 3$ [25], [26].

$$N = 2^{n-1} \quad (4)$$

Moreover, the comparisons encode the analog inputs as a digital word on three bits. All comparators run in parallel, which makes this ADC very fast. For this reason, it is called a flash adapter. Seven resistors of 1 k Ohm are connected between the 5 V power supply and the comparator output. The comparator outputs are connected to a 74LS148D encoder to generate a binary output signal. Therefore, for an analog signal above 0 V, this signal is separated into eight separate states via the (Q) quantization size, calculated by mathematical expression (5).

$$Q = \frac{V_{max} - V_{min}}{N} \quad (5)$$

where V_{max} is the maximum input voltage, V_{min} is the minimum input voltage and N is the number of levels.

4. SIMULATION RESULTS AND HARDWARE IMPLEMENTATION

4.1. Realization of the experimental and simulation of the sampler technique

In this section, the experimental and simulation realization of the proposed design is presented. Where, Figure 5 shows the experimental realization of the proposed design of the sampler technique. The figure shows the different components that were used in the proposed design.

Figure 6 demonstrates waveforms of the proposed sampler technique for both experimentally realization as shown in Figure 6(a) and simulation as shown in Figure 6(b). The measured voltage of the input signal waveform is 0.8 Vp-p, and the measured voltage of the output signal waveform is 2 Vp-p. Many results were taken, and the similarity of the waveforms with different values was recorded in Table 1.

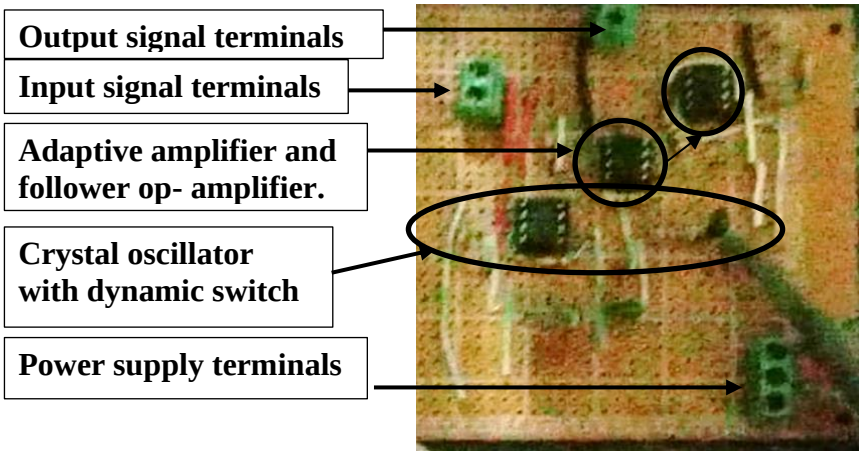
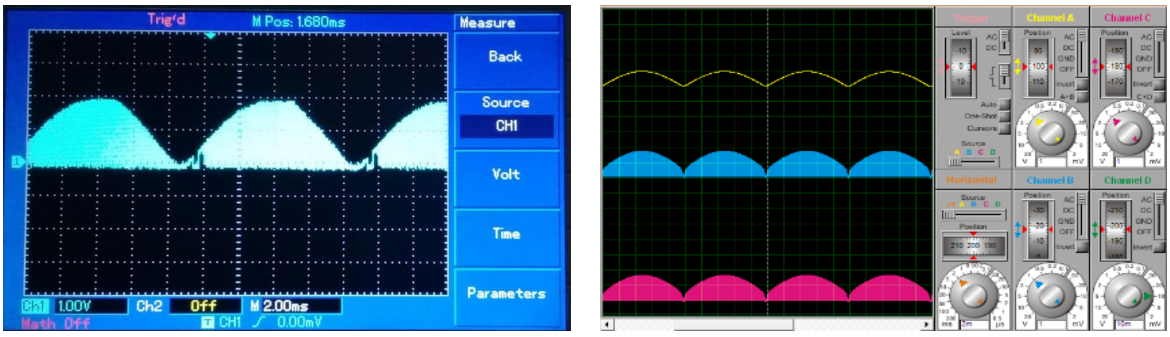


Figure 5. Circuit diagram of the sampler technique



(a) (b)

Figure 6. Waveform of sampler technique (a) experimentally and (b) simulation

Table 1 shows the results of the input and output signal of the adaptive amplifier circuit with different gain values. The results show that when the input signal is 0.02 V, the voltage gain AV reaches 10. Each time the input signal increases, the voltage gain AV decreases gradually. When the input signal is more than 1.5 V, the voltage gain AV keeps constant at 1.1 until 10 V. This adaptation expands the voltage response of the proposed ADC circuit. The results demonstrate an excellent efficiency for automatic control of the voltage gain of the amplifier circuit, which is realized.

Table 1. Results of the output signal with changing voltage gain of the adaptive amplifier circuit

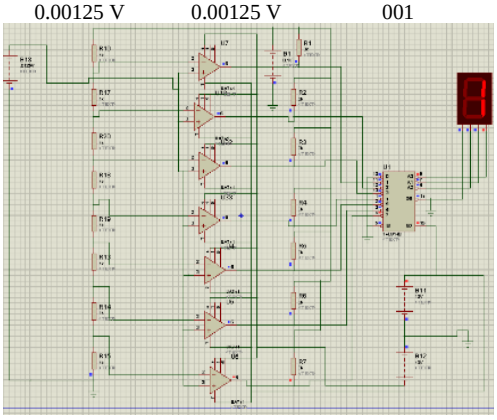
Input signal (V)	Voltage gain (A_V)	Output signal (V)
0.02	10	0.2
0.075	6.5	0.49
0.156	4	0.63
0.266	3	0.798
0.44	2.2	1
1.4	1.5	2.2
2.1	1.1	2.24
3	1.1	3.5
4.48	1.1	5.12
5.44	1.1	7.14

4.2. Experimental and simulation results of the quantizing and encoding circuit

Table 2 shows the results of the quantizer and encoder circuit at a very low signal from 0 V to 10 mV. The obtained results confirm the efficiency of our circuit in converting an analog signal that takes values from 0 V to 10 mV into eight digital values from 0 to 7. Conversely Table 3 shows the results of testing the circuit at a range of voltages from 0 to 10 V. The results show no problem in converting an analog signal from 0 to 10V into eight digital values from 0 to 7.

Table 2. Shows the results of the quantizer and encoder circuit

Ref. voltage (1)	V_{in} (1)	V_{out} (1) in binary	Ref. voltage (7)	V_{in} (7)	V_{out} (7) in binary
0.00125 V	0.00125 V	001	0.00875 V	0.00875 V	111



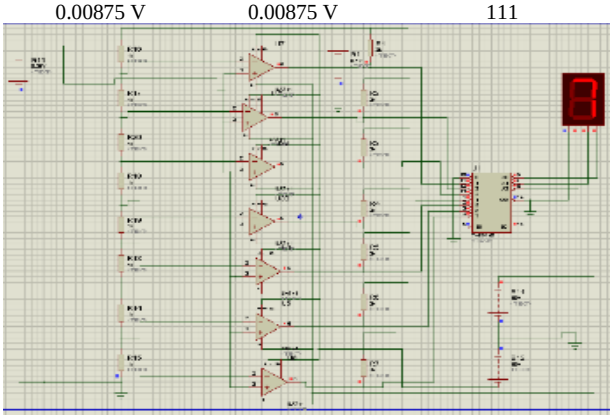


Table 3. Digital values in the range from 0 to 7 of analog signal varies from 0 V to 10 mV

Ref. voltage (1)	V_{in} (1)	V_{out} (1) in binary	Ref. voltage (3)	V_{in} (3)	V_{out} (3) in binary
0.00125 V	0.00125 V	001	0.00375 V	0.00375 V	011

Ref. voltage (5)	V_{in} (5)	V_{out} (5) in binary	Ref. voltage (7)	V_{in} (7)	V_{out} (7) in binary
0.00625 V	0.00625 V	101	0.00875 V	0.00875 V	111

Tables 3 and 4 show the results of the quantizer and encoder circuit. In Table 3, the results confirm the efficiency of this circuit in converting an analog signal that takes values in deficient voltage levels (from 0 V to 10 mV) into eight digital values from 0 to 7. Table 4 shows the results of testing the encoder circuit at various voltages in high voltage levels (from 0 to 10 V).

Table 4. Digital values in the range from 0 to 7 of analog signal varies from 0 to 10 V

Ref. voltage (0)	V_{in} (0)	V_{out} (0) in binary	Ref. voltage (2)	V_{in} (2)	V_{out} (2) in binary
Less than 1 V	1 V	000	2.5 V	2.5 V	010
Ref. voltage (4)	V_{in} (4)	V_{out} (4) in binary	Ref. voltage (6)	V_{in} (6)	V_{out} (6) in binary
5 V	5 V	100	7.5 V	7.5 V	110

5. CONCLUSION AND FUTURE WORK

In this paper, a flash ADC circuit is designed with low cost and high efficiency. Experimentally, a hardware implementation of the ADC circuit is realized. The proposed ADC is tested to suit a broad band of magnitude for the amplitude and frequency of analog input signals. The proposed ADC is based on selected components to achieve the desired target. The ADC circuit has an adaptive amplifier to expand the range of an analog input signal magnitude. Also, the ADC includes a sampler with a sampling rate of 11 MHz. The proposed ADC works with high efficiency and is low cost, with a range of magnitudes that expands from 10 mV to 10 V. The proposed ADC operates at a bandwidth of frequencies expanded from 0 Hz to more than 10 kHz. Experimentally, the Flash ADC circuit is tested to verify its performance. The ADC works efficiently and cheaply and gives 12×106 samples per second. Also, 3 bits are used to digitally represent the sampled values (with a quantization error of 0.125 for each 1 V). Therefore, the ADC gives a data rate of 36 Mb/s, whether in the simulation or hardware implementation. In future work, the proposed flash ADC circuit can be designed in nano-scale CMOS technologies. One could also design and implement new analog-to-digital converters with different resolutions.

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