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Design and analysis of 7-stage MOS current mode logic power gated MOSFETs in current starved voltage-controlled oscillator for the phase locked loop application

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ABSTRACT

This paper presents a new process, voltage and temperature (PVT) tolerant 7-stage ring type current starved voltage-controlled oscillator (CS-VCO). In this, a 7-stage ring VCO is proposed using power gated technique for phase locked loop (PLL) application. PLL plays a major role in clock and data recovery, Global Positioning System (GPS) system and satellite communications. For the high-speed application of PLL it is designed using 7-stage inverter delay cell with MOS current mode logic (MCML) technique. The circuit undergoes process, voltage and temperature variations with different parameters such as average power, oscillation frequency, phase noise, tuning range and output noise. The Monte-Carlo analysis justifies the proposed design provides better results. The circuit is simulated under 45 nm CMOS technology using cadence virtuoso. The average power consumption of the proposed circuit is 29.368 µW with the oscillation frequency of 3.06 GHz. The output noise and the phase noise of the proposed VCO are -161.55 dB and -125.92 dBc/Hz respectively. It achieves the frequency tuning range (FTR) of 95.09 %. The obtained simulation results are highly robust with PVT making the circuit suitable for PLL application.

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1. INTRODUCTION

The voltage-controlled oscillator (VCO) is an important component in various electronic circuits and communication systems, including phase locked loop (PLL) and clock data recovery (CDR). It generates an output signal whose frequency can be controlled by an input voltage. Inductor-capacitor (LC) oscillator operates based on an LC resonant network. It provides several advantages, including low noise and high-frequency operation but the major drawback of LC oscillators is that they require inductors, which increases the complexity of the circuit. A ring oscillator is another type of oscillator which is used due to its simple and digital nature, a ring oscillator can be easily integrated into IC designs with minimal additional complexity and cost [1]. The design of ring and LC oscillator using current mode logic and tank resonator for the space fiber application provide better analysis on the performance [2]. The advancement of rapid and effective technology heavily depends on high-speed devices. However, in mixed-signal systems, the design of analog circuits faces challenges due to switching noise. As a result, current mode logic (CML) is used to mitigate these issues. CML is widely used because of its inherent resistance to noise. This characteristic also

contributes to the popularity of MOS current mode logic (MCML) as a preferred choice among CML variants [3], [4]. The voltage-controlled oscillator commonly employs a complementary metal–oxide–semiconductor (CMOS) inverter as the delay unit. However, there is a possibility to substitute with stack, sleep, or sleepy stack inverters. By using these alternative delay types, it becomes feasible to minimize leakage power. The VCO typically consists of multiple delay cells arranged in a ring oscillator configuration. These delay cells can be either single-ended or differential. In both cases, their behavior and timing are controlled by a voltage referred to as the control voltage.

The actual oscillation frequency achieved by this method did not meet the initially anticipated expectations [5]. Through the modification of the approach, it becomes possible to increase the frequency of oscillation. However, this improvement comes with high power and minimum range of tuning [6], [7]. A new technique has emerged that attains the highest possible oscillation frequency while maintaining the quality of phase noise [8], [9]. In PLL, the control voltage plays an important role to modify the VCO's oscillation frequency, ensuring that it either rises or falls as needed. This adjustment aims to achieve synchronization between the feedback signal and the input signal, establishing a stable and coherent relationship between the two [10]. Prior research has focused on optimizing the oscillator circuit to improve PLLs performance using different methods. However, employing positive feedback offers an advantage as it helps to adjust the frequency tuning range effectively [11], [12]. To achieve the frequency tuning range appropriately different methods are employed [13]. A technique which has less phase noise but with more power consumption using a differential VCO [14]. The low noise circuits are designed with higher performance to improve the signal integrity [15], [16]. A bulk driven keeper technique based current starved ring VCO is introduced to minimize phase noise and power consumption [17].

A new dual threshold MOS technique is used with current starved voltage-controlled oscillator (CSVCO) for the maximum oscillation frequency and efficient switching [18]. A differential VCO design with minimum phase noise but it does not achieves good figure of merit (FOM) [19]. By the addition of feedback circuit, the complexity of the circuit may increase but it reduces the issue of non-linearity [20], [21]. Now-a-days resistive circuits are also used to achieve circuit linearity [22]. A new method of differential VCO achieves wider frequency tuning range, but suffers from maximum power consumption and high phase noise [23]. A new design of oscillator with process, voltage and temperature tolerant circuit achieves goof frequency of oscillation but it has very less FOM [24]. In the differential CSVCO circuit, achieves better oscillation frequency but suffers from maximum leakage power [25], [26]. A dual mode time interleaved ring VCO is utilized for high performance radio frequency (RF) systems. A pseudo-differential circuit is used as a ring oscillator for serial interfaces. In this, most updated M-PHY serial interface is used for high speed operation but it affects with maximum phase noise [27]. A new three stage oscillator is designed to achieve better oscillation frequency [28]. A differential CMOS ring VCO is designed with low noise for short range application, but it achieves only less frequency tuning range [29]. The frequency of oscillation is,

$$f = \frac{1}{2nt} \tag{1}$$

where n and t represent the stages of VCO and time delay respectively.

Phase noise affects signal quality, especially in high-precision applications, and overall system performance. To address this issue, a new 7-stage VCO has been developed with a focus on reducing phase noise and improved FOM. The proposed VCO circuit undergone different analysis using various process corners. These evaluations were conducted using the cadence virtuoso tool with 45 nm gpdk library. This paper is organized as: section 2 explains about the proposed technique with operation, section 3 discusses simulation results with various process, voltage and temperature tolerant, and section 4 presents the conclusion.

2. PROPOSED 7-STAGE VCO TECHNIQUE

The proposed 7-stage ring VCO mitigates phase noise and oscillation frequency. To minimize leakage in the proposed circuit, pull-up sleepy and power gated techniques are incorporated which depicted in Figure 1 and Figure 2. In this, power gated inverter with MCML is used shown in Figure 3. In an ideal CMOS inverter design, an approach is used to minimize subthreshold leakage by incorporating two additional transistors. These additional components include a PMOS transistor at the top called pull-up sleepy transistor and a combination of P-channel MOS (PMOS) and P-channel MOS (NMOS) transistor at the bottom known as the power gated inverter design. When the sleep input is set to 0 and the sleep bar is 1, transistors M_1, M_4 and M_5 are turned ON, causing nodal voltages V_a and V_b to become Vdd and ground potential respectively. In this state, transistors M_2 and M_3 function as a regular inverter, producing an output based on the input signal V_{in}. On the other hand, when sleep and sleep bar become 1 and 0 respectively, M_1, M_4 and M_5 are in a cutoff condition. This effectively puts the circuit in a "sleep" mode, reducing the voltage at V_a and increasing the voltage at V_b.

As a consequence of this change, the V_{SB} of M_1 increases, resulting in a higher threshold voltage for M_1 and subsequently reduces subthreshold leakage in the CMOS inverter, making it more power-efficient when in sleep mode. To ensure a stable and controlled oscillation, specific adjustments are required in each delay stage. In the proposed VCO design in Figure 3, the PMOS transistors M_4, M_{11}, M_{18}, M_{25}, M_{32}, M_{39} and M_{46} acts as the sleep transistors called pull-up sleepy approach. Because of using sleep transistor only at the top of the inverter design it reduces area consumption. The transistors M_2, M_9, M_{16}, M_{23}, M_{30}, M_{37}, M_{44} and M_{51} acts as the control logic. The power gated technique is applied at the bottom of the inverter stage. The transistors with sleep bar inputs such as M_7, M_{14}, M_{21}, M_{28}, M_{35}, M_{42}, M_{49} and the transistors with sleep inputs such as M_8, M_{15}, M_{22}, M_{29}, M_{36}, M_{43}, M_{50} acts as power gated transistors. By incorporating sleep transistors leads to power off the circuit during idle conditions, specifically when "SLP" signal is set to 1. This implementation minimizes leakage and enables the operation of high speed. When PLL is synchronized, the inverter switches to the idle condition, causing the circuit to cut off the power supply. Consequently, this action reduces the subthreshold current and hence the overall performance gets improved.

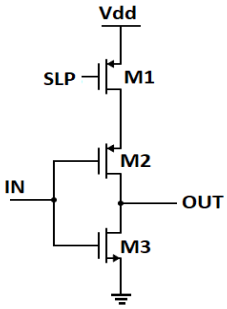

Figure 1. Pull-up sleepy technique

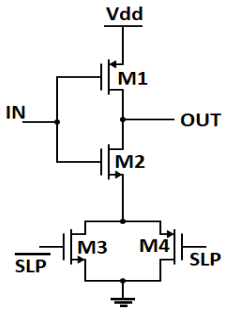

Figure 2. Power gated technique

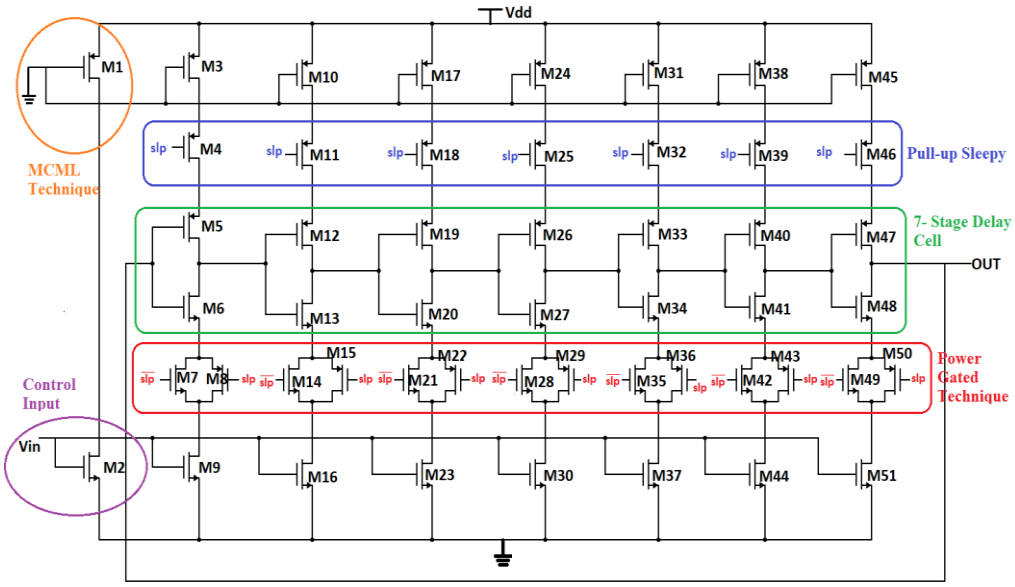

Figure 3. Proposed 7-stage pull-up sleepy CS ring VCO using power gated technique

3. RESULTS AND DISCUSSION

3.1. Average power and frequency tuning range analysis

The values of average power are tabulated in Table 1. It is evaluated at 27 ˚C with 1 V supply. The average power at tt process corner is 29.36 µW with the oscillation frequency of 3.06 GHz. The frequency tuning range is determined by [30],

$$FTR = \frac{f_h - f_l}{f_h} \quad (2)$$

where f_h and f_l represents the higher and lower frequency respectively.

Table 1. Performance of the proposed 7- stage VCO at different process corners

Parameters	Different process corners				
	TT	FF	SS	FS	SF
Average power (µW)	29.36	40.16	20.01	22.83	29.56
Oscillation frequency (GHz)	3.06	4.02	2.07	2.43	2.81
Output noise (dB)	-161.55	-156.71	-154.4	-159.15	-162.9
Phase noise (dBc/Hz)	-125.92	-125.58	-126.32	-125.79	-125.98

3.2. Analysis of phase noise

The phase noise of the proposed VCO is analyzed as [31],

$$Phase\ noise, L(\Delta f) = \frac{8}{3\eta}\frac{KT}{P_t}\frac{\gamma V_{dd}}{V_{ov}}\frac{f_{osc}^2}{\Delta f^2} \quad (3)$$

where η is characteristic constant, K is Boltzmann constant, T is absolute temperature, P_t is total power dissipated, V_{ov} is overdrive voltage, V_{dd} is supply voltage and Δf is frequency offset, f_{osc} is frequency of oscillation, and γ is device co-efficient. The average phase noise of the proposed VCO is -125.92 dBc/Hz.

3.3. Analysis of figure of merit

The FOM is used to analyze the performance of the circuit [32].

$$FOM = L(\Delta f) - 20\log\left(\frac{f}{\Delta f}\right) + 10\log\left(\frac{P_{avg}}{1mW}\right) \quad (4)$$

where $L(\Delta f)$ is the phase noise, f represents frequency of oscillation, P_{avg} is the average power. The FOM of the proposed VCO achieves -191.53.

3.4. Monte Carlo analysis

The Monte-Carlo analysis of the proposed 7-stage VCO technique shown in Figure 4. It involves simulation run with 200 samples. Figure 4(a) depicts the histogram plot of average power; Figure 4(b) illustrates oscillation frequency and Figure 4(c) depicts the phase noise.

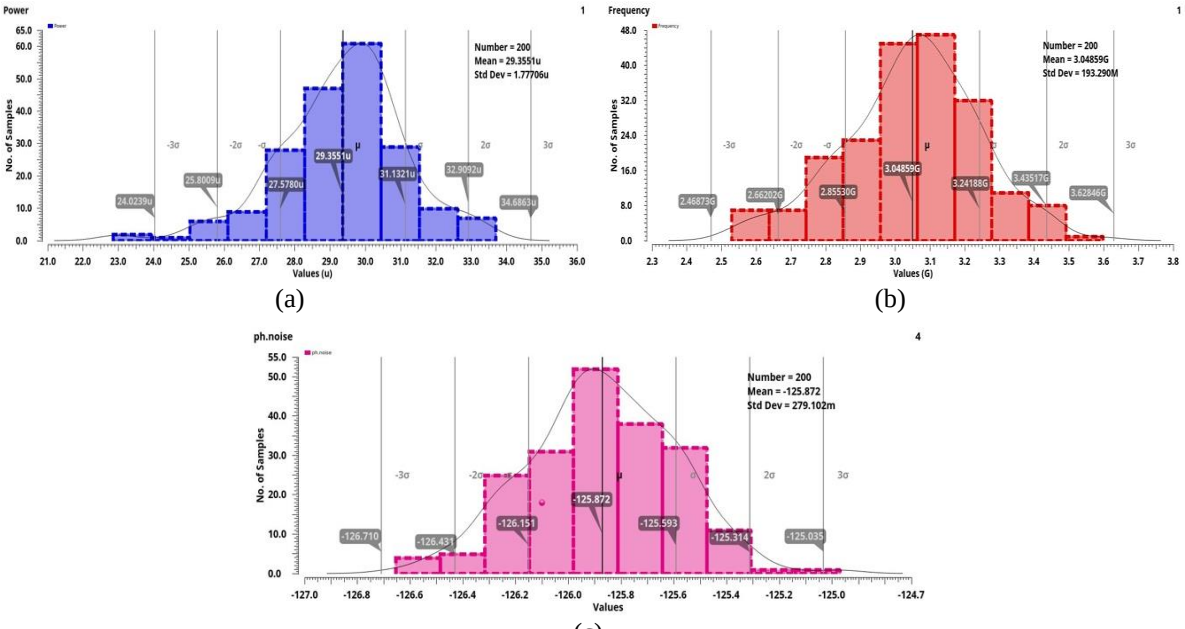

Figure 4. Monte-Carlo analysis of the proposed 7-stage VCO technique (a) average power (b) oscillation frequency (c) phase noise

3.5. Effect of control voltage on proposed VCO

Parametric analysis with different control voltages of the proposed VCO are tabulated in Table 2. The graphical representations are depicted in Figure 5. Figure 5(a) illustrates the analysis of average power at different supply voltages, Figure 5(b) represents oscillation frequency, Figure 5(c) illustrates phase noise, and Figure 5(d) represents output noise.

Table 2. Performance of power, frequency and noise at different control voltages

Vdd (V)	Control Voltage (V)	Different parameters of the proposed VCO @ different control voltage			
		Power (µW)	Frequency (GHz)	Output noise (dB)	Phase noise (dBc/Hz)
0.8	0.6	2.46	0.625	-157.72	-121.89
	0.8	8.61	1.28	-157.72	-125.89
	1	9.86	0.662	-157.72	-125.72
	1.2	10.68	0.705	-157.72	-125.63
	1.4	11.43	0.986	-157.72	-125.58
1	0.6	4.67	0.892	-161.55	-123.24
	0.8	18.71	2.59	-161.55	-125.62
	1	29.36	3.06	-161.55	-125.92
	1.2	32.91	3.16	-161.55	-125.79
	1.4	34.49	3.29	-161.55	-125.73
1.2	0.6	7.57	1.04	-162.78	-122.54
	0.8	32.67	3.47	-162.78	-124.9
	1	52.25	3.965	-162.78	-126.14
	1.2	60.24	4.231	-162.78	-126.08
	1.4	66.87	4.88	-162.78	-126.02

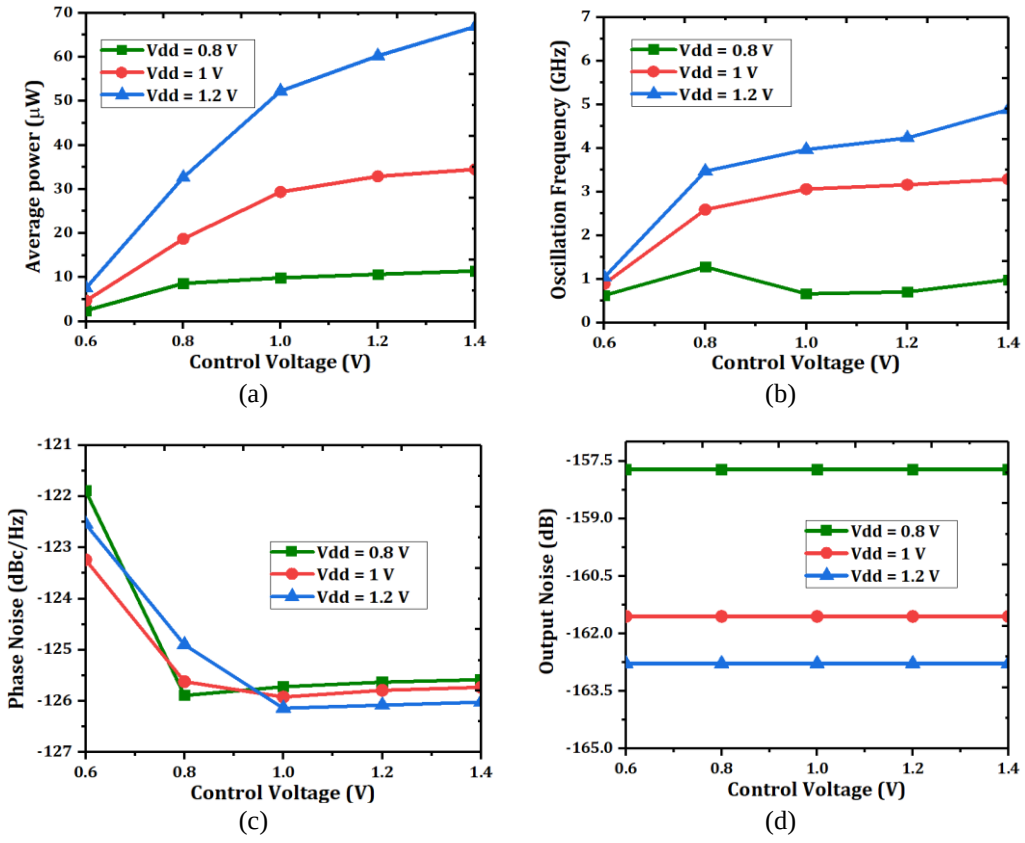

Figure 5. Parametric analysis with different control voltages of the proposed VCO with (a) average power, (b) oscillation frequency, (c) phase noise, and (d) output noise

3.6. Effect of temperature on proposed VCO

Parametric analysis with different temperatures of the proposed VCO is tabulated in Table 3. The graphical representations are depicted in Figure 6. Figure 6(a) illustrates the analysis of average power,

Figure 6(b) represents oscillation frequency, Figure 6(c) depicts the phase noise, and Figure 6(d) shows the output noise.

Table 3. Performance of power, frequency and noise at different temperatures

Vdd (V)	Temperature (^{0}C)	Different parameters of the proposed VCO @ different temperatures			
		Power (µW)	Frequency (GHz)	Output noise (dB)	Phase noise (dBc/Hz)
0.8	-90	14.24	2.17	-155.65	-125.52
	-40	12.11	1.12	-153.46	-125.57
	0	10.62	0.768	-154.36	-125.62
	27	9.865	0.662	-157.72	-125.71
	90	8.95	0.889	-157.74	-125.86
1	-90	31.02	4.96	-165.11	-125.47
	-40	36.23	3.94	-159.94	-125.62
	0	26.05	3.105	-160.89	-125.79
	27	29.36	3.06	-161.55	-125.91
	90	22.18	0.463	-158.78	-126.19
1.2	-90	63.94	6.92	-168.28	-125.75
	-40	67.74	5.74	-164.57	-125.86
	0	59.41	4.94	-163.73	-126.02
	27	52.25	3.21	-162.78	-126.14
	90	45.82	1.43	-158.88	-126.41

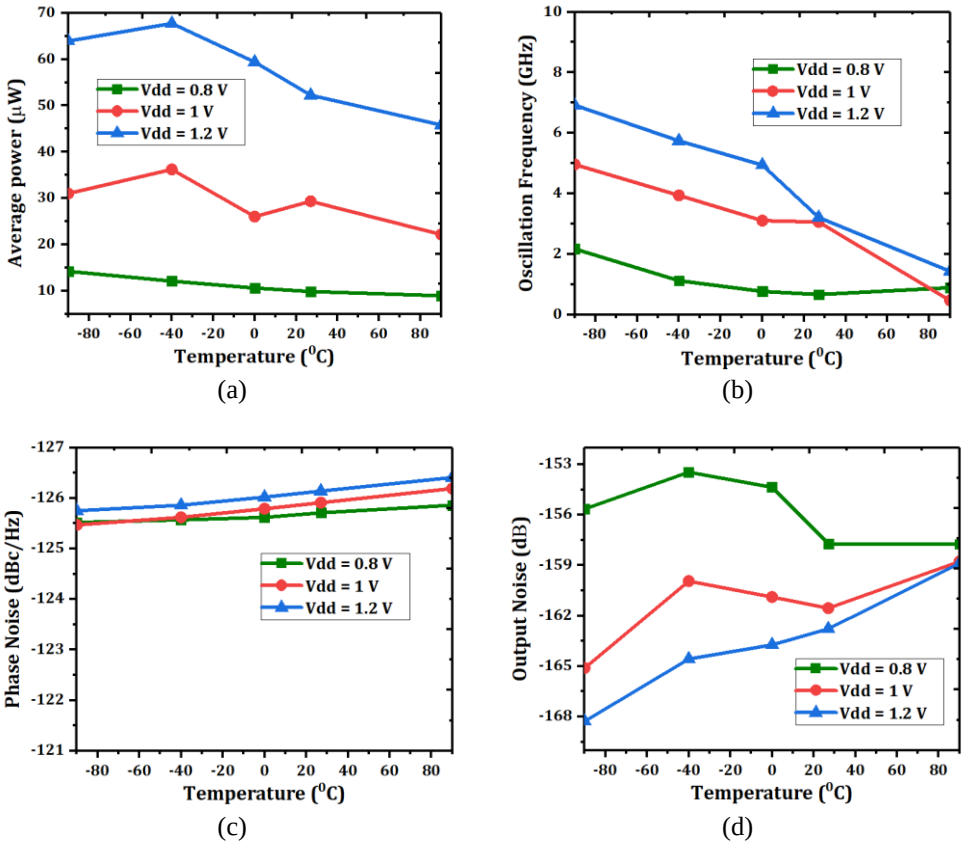

Figure 6. Parametric analysis with different temperatures of the proposed VCO with (a) average power, (b) oscillation frequency, (c) phase noise, and (d) output noise

3.7. Performance comparison

Table 4 represents the performance comparison of the proposed ring VCO with the recent works. The existing few works achieved better figure of merit with the cost of low tuning range, high power and achieves maximum phase noise. The table illustrates clearly that the proposed result provides better performance when compared to the existing works with higher oscillation frequency, better phase noise, minimum power consumption and with higher FOM.

Table 4. Performance comparison of proposed work with existing works

Parameters	[8][a]	[10][a]	[18][b]	[28][a]	[13][b]	[22][b]	Proposed work[b]
Technology (nm)	180	180	45	65	90	90	45
Supply voltage (V)	1	1.8	1.2	0.75	1	1.2	1
Average power (mW)	2.5	10.8	0.053	15.45	0.046	0.0446	0.0293
Oscillation frequency (GHz)	1.03	20.7	1.33	5.5	1.57	1.78	3.06
Tuning range (%)	53	8.6	98	22.8	*	95.48	95.09
Phase noise (dBc/Hz)	-105.5	-108.03	*	-103.2	-78.28	-95.15	-125.92
Figure of Merit (dBc/Hz)	*	-184	*	-186	-91.75	-173.6	-191.53
Structure	Ring	Ring	Ring	Ring	Ring	Ring	Ring

**Not reported [a] Measurement results [b] Simulation results*

4. CONCLUSION

A new PVT tolerant current starved 7-stage ring VCO is proposed for high frequency PLL application. In this pull-up sleepy and power gated inverter techniques are used in the proposed design to enhance the frequency of oscillation and minimize phase noise. The simulation is performed with 45 nm gpdk library using cadence virtuoso tool. The performance of the proposed VCO is analyzed using the histogram plot of Monte-Carlo simulations with 200 samples. To verify the robustness of the proposed design, parametric analysis is performed with different temperatures and control voltages and also with different process corners. The proposed circuit achieves 71.9% improvement in oscillation frequency and 51.87% improvement in average power. It also has the percentage improvement of 32.3%, 11.7% and 10.28% in phase noise, output noise and FOM against the existing 7-stage ring VCO. The above results proves that the proposed circuit is highly tolerant with the process, voltage and temperature and hence it can be widely used in the PLL applications.

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