International Journal of Electrical and Computer Engineering (IJECE)
Vol. 14, No. 2, April 2024, pp. 1390~1397
ISSN: 2088-8708, DOI: 10.11591/ijece.v14i2.pp1390-1397

A proposal and simulation analysis for a novel architecture of gate-all-around polycrystalline silicon nanowire field effect transistor

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Article Info

Article history:

Received Jul 17, 2023
Revised Nov 17, 2023
Accepted Nov 29, 2023

Keywords:

Corner effect
Density of states
Field effect transistor
Microelectronics
Numerical simulation
Polysilicon nanowires

ABSTRACT

A proposal for a novel gate-all-around (GAA) polycrystalline silicon nanowire (poly-SiNW) field effect transistor (FET) is presented and discussed in this paper. The device architecture is based on the realization of poly-SiNW in a V-shaped cavity obtained by tetra methyl ammonium hydroxide (TMAH) etch of monocrystalline silicon (100). The device's behavior is simulated using Silvaco commercial software, including the density of states (DOS) model described by the double exponential distribution of acceptor trap density within the gap. The electric field, potential, and free electron concentration are analyzed in different nanowire regions to investigate the device's performance. The results show good performance despite the high density of deep states in poly-SiNW. This can be explained by the strong electric field caused by the corner effect in the nanowire, which favors the ionization of the acceptor traps and increases the free electron concentration.

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1. INTRODUCTION

Polycrystalline silicon nanowires (poly-SiNWs) have attracted considerable attention in the last decades as an active element for the new generation of electronic devices, such as thin film transistors (TFT) [1]–[3] and biochemical sensors [4], [5]. The electrical properties of poly-SiNWs as well as their realization technique have rendered these nanowires potentially promising candidates for overcoming several obstacles, such as the short channel effects encountered in fin-shaped field effect transistors (FinFETs) [6], owing to their sensitivity to chemical and biological species. Different techniques have been implemented to realize poly-SiNWs [7], [8], and the top-down approach affords an important advantage due to its compatibility with the concept of miniaturization. The planar technology is commonly used in the very large-scale industry to produce reliable and low-cost devices. More precisely, for low-temperature technologies, polycrystalline silicon is a widely used material.

Although the operating of devices based on poly-SiNWs has been demonstrated [9], [10] and their performance has been encouraging, they are still being researched to better understand and identify the properties of poly-SiNWs for integration in commercial devices. Furthermore, the electrical properties of poly-SiNWs are closely linked to their production processes, their diameter [11], and their architecture. More precisely, their crystalline quality plays a decisive role in the device performance. Thus, poly-SiNWs with a

good crystalline quality will afford high-performance devices such as poly-SiNW based transistors with a high I_{ON}/I_{OFF} ratio, reduced threshold voltage, and small subthreshold swing [12]. In contrast, a low or even highly disordered crystalline quality is advantageous for sensors owing to the interaction of the electrical defects on the surface with the surrounding chemical species [13].

Thanks to planar microelectronic technology, several poly-SiNW field effect transistors (FETs) architectures have been developed, such as back-gate [14], dual gate [15], and gate-all-around [16]–[18]. Compared to the back gate and dual gate, the gate-all-around FET shows a particular advantage due to the channel modulation by gate voltage over the entire surface of the nanowire, increasing the ON current and decreasing the subthreshold swing and the threshold voltage. According to the realization process of gate-all-around poly-SiNW FETs reported in the literature, the sections of these SiNWs have a quasi-circular shape or square shape with rounded edges. Previous work [19]–[21] showed that the shape of SiNW significantly affects the device's performance. Particularly when the SiNW shape is triangular, where the free electron concentration increases near the corners.

In our previous study, we demonstrated the feasibility of poly-SiNW in a V-shaped cavity obtained by tetra methyl ammonium hydroxide (TMAH) etching of Si-mono (100) [11]. This method allows the elaboration of a SiNW with a triangular cross-section. This technique is fully compatible with planar microelectronics technology, allowing the SiNW to be integrated as an active element in various devices such as transistors and biochemical sensors.

In this work, we propose a novel poly-SiNW gate-all-around (GAA) FET architecture based on the realization of poly-SiNW in a V-shaped cavity. The paper is organized as: the proposition of key process steps to realize the device is presented in section 2. The 3D technology computer aided design (TCAD) model of the device is performed using the Silvaco TCAD commercial software [22] including DOS, which is presented in section 3. Section 4 presents the results and discussion. Section 5 concludes this work.

2. METHOD

2.1. Key process steps proposition

In Figure 1, we report a technological steps proposition for the realization of the device in low-temperature planar technology. i) On a mono-Si wafer (100), a photolithography is performed to create a rectangular opening; ii) A TMAH etching is realized to create a V-shaped cavity on the substrate; iii) N-type doping by ion implantation is performed to activate the upper surface of the substrate; iv) Low-temperature oxidation or silicon oxide deposit (or another insulator) is realized to form the gate insulator; v) A double layer of un-doped polysilicon followed by in-situ doping (N-type) is deposited by chemical vapor deposition (CVD); vi) A reactive ion etching (RIE) etching of the polysilicon is performed where a poly-Si residue is formed in the cavity, as shown in Figure 2. Then, this residue corresponds to the poly-SiNW and forms the channel of our device; vii) A second insulator is deposited and patterned to create the contact's access; and viii) metallization, patterning, and etching are realized to create the device contacts: gate, drain, and source.

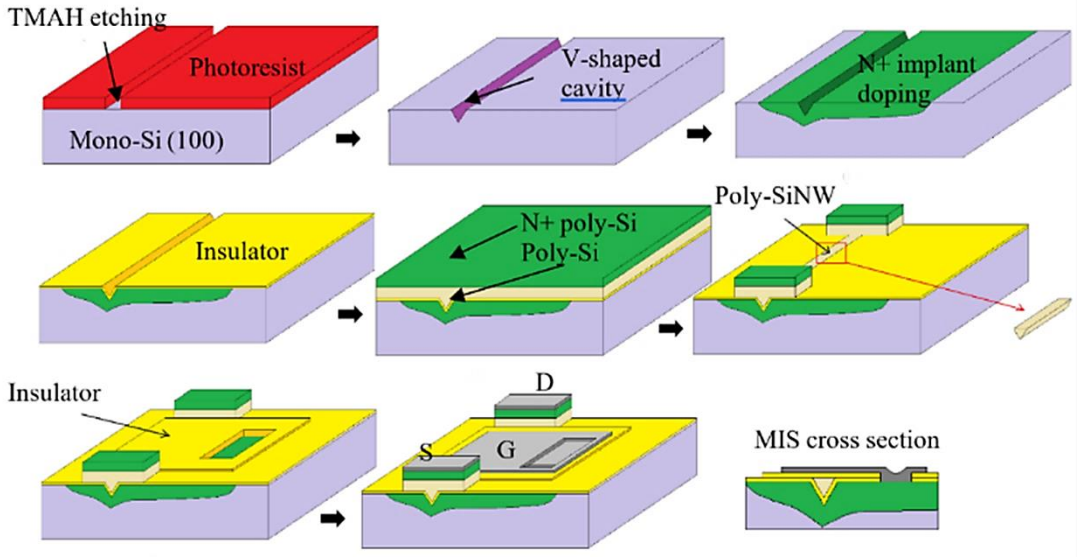


Figure 1. Process steps proposition for the realization of GAA poly-SiNW FET

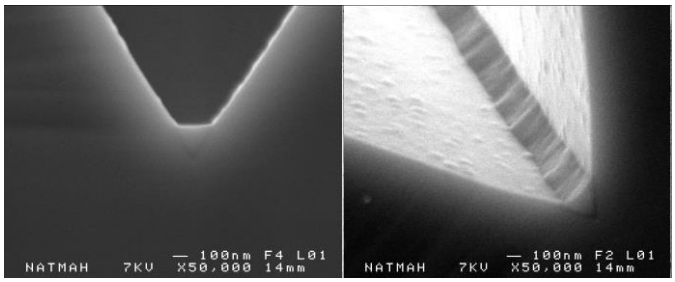


Figure 2. MEB micrograph from [11]

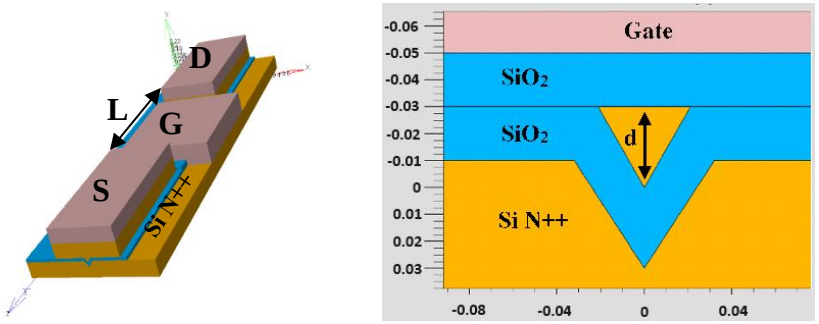
2.2. TCAD model of proposed device

In a previous study [23], we examined the electrical properties of poly-SiNWs realized by the spacer method. It was found that when the section was less than 50 nm, the conduction mechanism operated through variable-range hopping (VRH). This is because of the high density of electric traps, which is due to the disordered structure of the undoped poly-Si layer from which these nanowires are obtained. The V-shaped cavity poly-SiNW is also an etching residue of the undoped poly-Si layer, and it has similar crystalline quality to the poly-SiNW obtained using the spacer method. As a result, we can use the density of states (DOS) model [24] to express the distribution of defects within the gap. This distribution can be expressed as (1) and (2):

$$g_{TA}(E) = N_{TA}\, exp\left(\frac{E-E_C}{w_{TA}}\right) \quad (1)$$

$$g_{DA}(E) = N_{DA}\, exp\left(\frac{E-E_C}{w_{DA}}\right) \quad (2)$$

Here, $g_{TA}(E)$ and $g_{DA}(E)$ are two exponential densities that correspond to the densities of the acceptor's tail and deep states, respectively. E is the trap energy; E_C is the conduction band energy. For tail distribution, DOS is described by the conduction band edge intercept density N_{TA} and the characteristic decay energy W_{TA}. For deep distribution, DOS is described by the conduction band edge intercept density N_{DA} and the characteristic decay energy W_{DA}. Figures 3(a) and 3(b) show the 3D view and cross-sectional view, respectively, of simulated device performed using Silvaco TCAD commercial software. The device sizes and simulation parameters are listed in Table 1.



(a) (b)

Figure 3. Simulated GAA poly-SiNW FET device (a) 3D TCAD view and (b) cross-sectional view

Table 1. Simulation parameters

Parameter	Value
tox	20 nm
L	1µm
SiNW depth (d)	30 nm
N_{TA}	1,2.10^{21} $cm^{-3}.eV^{-1}$
N_{DA}	2.10^{20} $cm^{-3}.eV^{-1}$
W_{TA}	0.06 eV
W_{DA}	0.1 eV

3. RESULTS AND DISCUSSION

Figure 4 shows the simulated transfer characteristic of our device for V_{DS} values of 0.1, 1, and 3 V. For comparison, Figure 4 includes a simulated transfer characteristic of the device without DOS. Table 2 shows device performances with and without DOS.

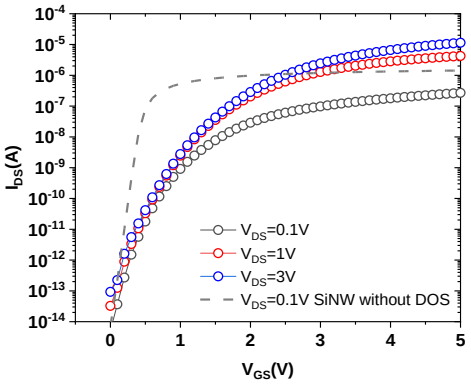


Figure 4. Transfer characteristics for simulated device. symbol: including DOS, dash line: without DOS

Table 2. Device performances (V_{DS}=0.1 V)

Parameter	With DOS	Without DOS
I_{ON}/I_{OFF}	3.4 10^7	2 10^8
SS	262 mV/dec	80 mV/dec
V_{th}	1.5 V	0.87 V

From Figure 4, a field effect is observed indicating an N-channel transistor behavior for a positive gate voltage. The performance of the device is degraded when compared to SiNW without DOS. This results in increased threshold voltage (V_{th}) and subthreshold swing (SS), as well as a decreased I_{ON}/I_{OFF} ratio. Our previous study of poly-SiNW FET performances [25] highlights this degradation, which is explained by the high density of deep states and their effects on the drain current below the threshold region. According to the literature [25], we can consider the drain current model of poly-SiNW FET.

$$I_{DS} = \frac{W}{L}\frac{q\mu_0 N_0}{\sqrt{\frac{2kT}{\varepsilon_{si}}N_{02,3}}}\frac{2W_{T,DA}.kT}{2W_{T,DA}-kT}\left(\frac{V_{GS}-V_{FB}}{\frac{\sqrt{\varepsilon_{si}2kT}}{C_{ox}}\sqrt{N_{02,3}}}\right)^{\frac{2W_{T,DA}}{kT}-1} V_{DS} \quad (3)$$

where all model parameters values are listed in the reference [25].

The model refers to a poly-SiNW FET, where the gate controls the channel on only one face (known as the side gate). However, in the proposed device, the gate coats the entire nanowire, as shown in Figure 5. The width of the gate corresponds to:

$$W = W_{sup} + 2 * W_{ob} \quad (4)$$

In Figure 6, the transfer characteristic of (3) model is compared to the simulated transfer characteristic for $V_{DS} = 1\,V$. The comparison highlights a significant difference between the two as the drain current according to the model is lower than the simulated drain current. To better understand this difference, we will analyze the electric field profile, electric potential, and free electron concentration of our simulated device compared to that of a simulated side-gate poly-SiNW FET [25].

Figures 7 and 8 show a cross-sectional view of the side-gate FET and our device, respectively. Figures 7(a) and 8(a) indicate the cutting directions for probing the electric field E, the potential $q\psi$, and the free electron concentration for the two devices. Figures 7(b), 7(c), and 7(d) show a decrease in the electric field, potential, and free electron concentration along the x direction for various cutting directions y_i $(i = 1,2,3)$ in a simulated poly-SiNW side-gate FET. These quantities decay homogeneously, indicating the charge sheet model for a classic MOSFET structure. For $V_{GS} = 3\,V > V_{th}$, the free electron concentration near the SiO_2/poly-SiNW interface is relatively low (10^{15} cm^{-3}) compared to the free electron concentration

commonly observed for MOSFET structures [26]. This is caused by the high density of acceptor traps (deep states) [25], which are not sufficiently ionized ($q\psi << E_F = 0.56\,eV$) despite the device operating above the threshold.

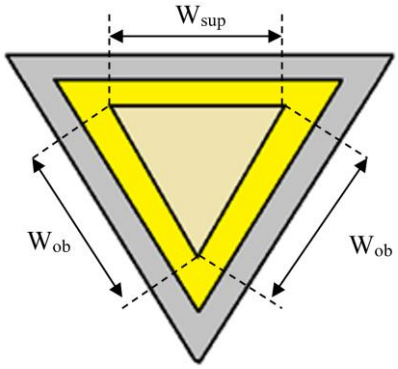


Figure 5. Width size of considered MIS structure following (4)

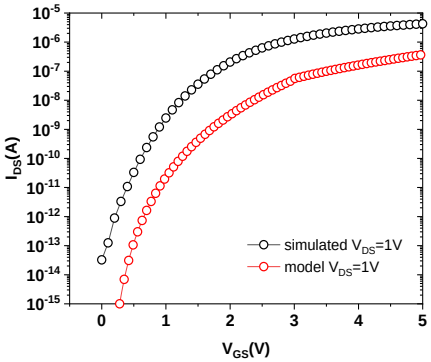
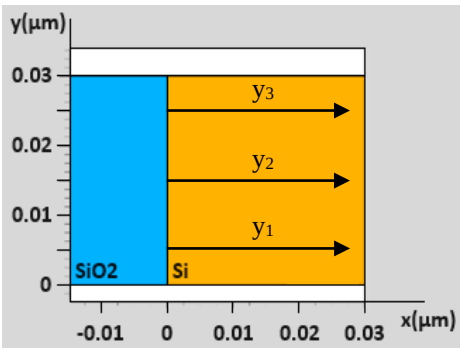
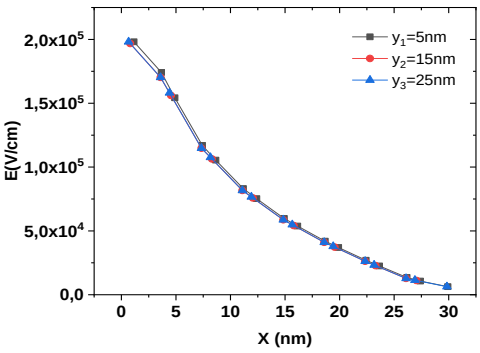


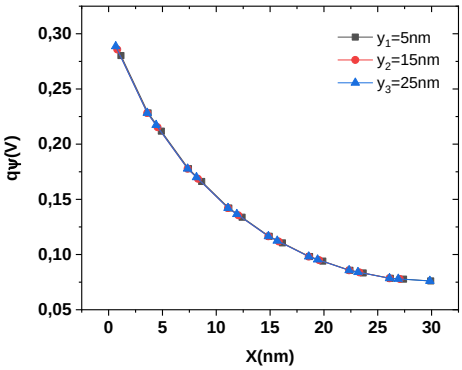
Figure 6. Model (W=117 nm) and simulated transfer characteristics



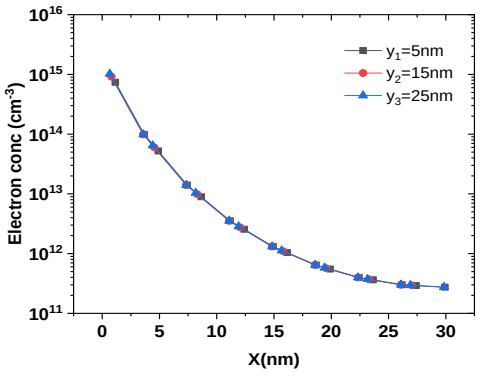
(a)



(b)



(c)



(d)

Figure 7. Cross-sectional view of poly-SiNW side-gate FET: (a) cutting axis y_i $(i = 1,2,3)$ along x direction, (b) electric field, (c) potential, and (d) free electron concentration for ($V_{GS} = 3\,V$ and $V_{DS} = 0\,V$)

Figures 8(b), 8(c), and 8(d) illustrate a decrease in the electric field, potential, and free electron concentration, respectively, for the simulated poly-SiNW GAA FET, along cutting directions $u_i(i = 1,2,3)$. Compared to the poly-SiNW side-gate FET, non-uniformity is visible depending on the u_i directions. These quantities exhibit the same values observed for the poly-SiNW side-gate FET near the SiO_2/poly-SiNW interface when measured along the u_2 direction. However, the values are visibly higher when measured along

the u_1 and u_3 directions as compared to u_2. This is due to the corner effect [20], which is a consequence of the strong electric field in the corners of the nanowire. Near these corners, the top gate TG and the bottom gate BG become very close (see dash circles in the cross-sectional view of Figure 8(d)) and can be viewed as a double-gate MOSFET structure. Tsai *et al.* [27] demonstrated that a double-gate MOSFET structure exhibits a strong electric field for very thin channels (a few nanometers). In the corners, the electric field is strong, which results in an electric potential that is close to E_F (at the SIO_2/poly-SiNW interface, $q\psi = 0.45\ V$ for u_1 and $q\psi = 0.5\ V$ for u_3). This allows the acceptor traps to ionize sufficiently and increases the free electron concentration. Previous studies [19]–[21] have shown that triangular nanowires also have an increase in the free electron concentration. The corner effect is primarily responsible for the high performance of device, which is relatively higher than the performance reported in the literature [16], as shown in Table 3. However, the subthreshold slope (SS) and threshold voltage (V_{th}) remain high and can be improved by NH_3 [16] treatment, which reduces defects density in the nanowire.

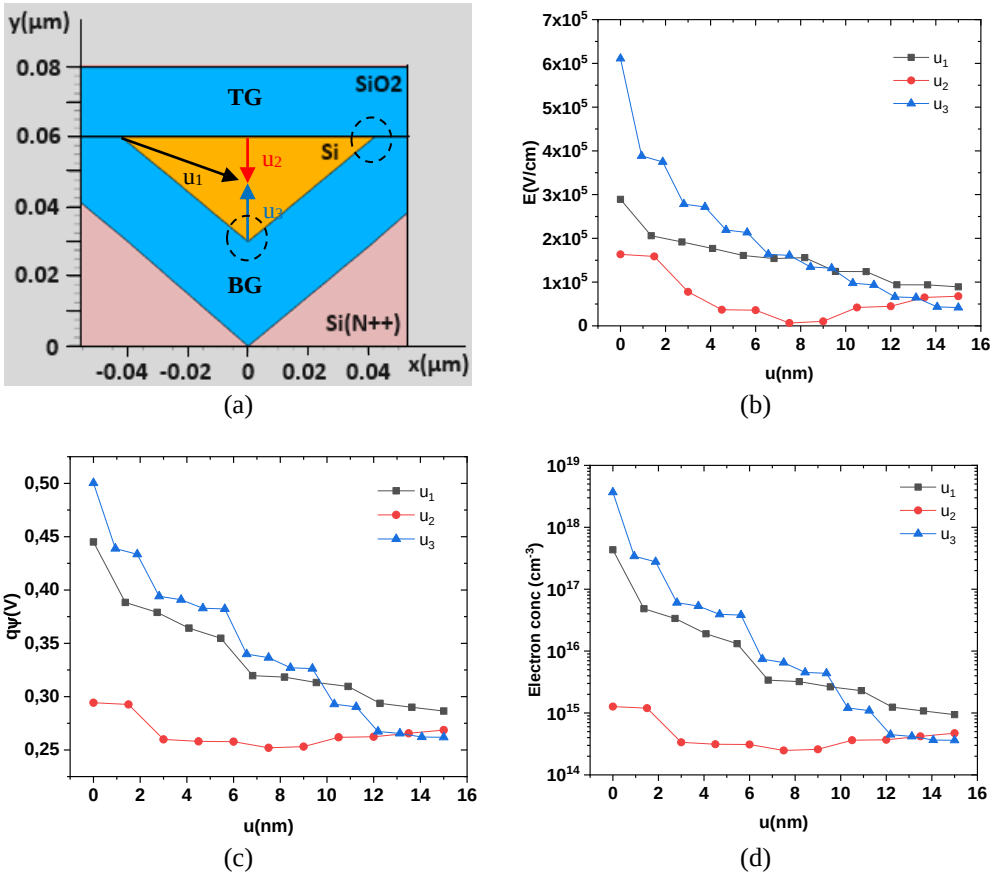


Figure 8. cross-sectional view of GAA poly-SiNW FET: (a) cutting directions $u_i (i = 1,2,3)$, (b) electric field, (c) potential, and (d) free electron concentration for ($V_{GS} = 3\ V$ and $V_{DS} = 0\ V$)

Table 3. Device performances comparison

Parameter	Our device	(without NH_3 treatment) [16]
I_{ON}/I_{OFF}	3.4 10^7	~2.10^7
SS	262 mV/dec	353 mV/dec
V_{th}	1.5 V	2.87 V

4. CONCLUSION

In this study, we have proposed a new architecture for GAA FET that can be realized using low temperature technology. The architecture is based on poly-SiNW elaborated in a V-shaped cavity obtained by TMAH etching of Si-mono (100). Despite the high density of acceptor traps, the simulated device showed remarkable performance when compared to the drain current model established in the literature. Our analysis of the electric field and potential enabled us to understand the origin of the device's performance. We

observed that the corner effect enhances the ionization of acceptor traps and increases free electron concentration near SiNW corners. Our device exhibits good performance compared to the GAA FETs mentioned in the literature, which can be further enhanced by reducing defect density through NH_3 treatment.

REFERENCES

[1] T.-Y. Liu, F.-M. Pan, and J.-T. Sheu, "Characteristics of gate-all-around junctionless polysilicon nanowire transistors with twin 20-nm gates," *IEEE Journal of the Electron Devices Society*, vol. 3, no. 5, pp. 405–409, Sep. 2015, doi: 10.1109/jeds.2015.2441736.

[2] M. Xu *et al.*, "High performance transparent in-plane silicon nanowire Fin-TFTs via a robust nano-droplet-scanning crystallization dynamics," *Nanoscale*, vol. 9, no. 29, pp. 10350–10357, 2017, doi: 10.1039/c7nr02825c.

[3] Y.-H. Chen, W. Cheng-Yu Ma, and T.-S. Chao, "High-performance poly-Si TFT with ultra-thin channel film and gate oxide for low-power application," *Semiconductor Science and Technology*, vol. 30, no. 10, p. 105017, Sep. 2015, doi: 10.1088/0268-1242/30/10/105017.

[4] S. Tang *et al.*, "Fabrication of low cost and low temperature poly-silicon nanowire sensor arrays for monolithic three-dimensional integrated circuits applications," *Nanomaterials*, vol. 10, no. 12, p. 2488, Dec. 2020, doi: 10.3390/nano10122488.

[5] L.-C. Yen, T.-M. Pan, C.-H. Lee, and T.-S. Chao, "Label-free and real-time detection of ferritin using a horn-like polycrystalline-silicon nanowire field-effect transistor biosensor," *Sensors and Actuators B: Chemical*, vol. 230, pp. 398–404, Jul. 2016, doi: 10.1016/j.snb.2016.02.095.

[6] A. Gill, C. Madhu, and P. Kaur, "Investigation of short channel effects in Bulk MOSFET and SOI FinFET at 20 nm node technology," Dec. 2015, doi: 10.1109/indicon.2015.7443263.

[7] F. Demami, L. Pichon, R. Rogel, and A. C. Salaün, "Fabrication of polycrystalline silicon nanowires using conventional UV lithography," *IOP Conference Series: Materials Science and Engineering*, vol. 6, Nov. 2009, doi: 10.1088/1757-899x/6/1/012014.

[8] M. Im *et al.*, "Multiple-gate CMOS thin-film transistor with polysilicon nanowire," *IEEE Electron Device Letters*, vol. 29, no. 1, pp. 102–105, Jan. 2008, doi: 10.1109/led.2007.911982.

[9] M. Oda, K. Sakuma, Y. Kamimuta, and M. Saitoh, "Carrier transport analysis of high-performance poly-Si Nanowire transistor fabricated by advanced SPC with record-high electron mobility," *2015 IEEE International Electron Devices Meeting (IEDM)*, Washington, DC, USA, 2015, pp. 6.1.1-6.1.4, doi: 10.1109/iedm.2015.7409637.

[10] H.-H. Hsu, T.-W. Liu, L. Chan, C.-D. Lin, T.-Y. Huang, and H.-C. Lin, "Fabrication and characterization of multiple-gated poly-si nanowire thin-film transistors and impacts of multiple-gate structures on device fluctuations," *IEEE Transactions on Electron Devices*, vol. 55, no. 11, pp. 3063–3069, Nov. 2008, doi: 10.1109/ted.2008.2005161.

[11] F. Demami, "Synthesis of silicon nanowires by spacers formation technique for electronic devices (France)," Universite de Rennes 1, 2011.

[12] Y.-C. Wu *et al.*, "High-performance polycrystalline silicon thin-film transistor with multiple nanowire channels and lightly doped drain structure," *Applied Physics Letters*, vol. 84, no. 19, pp. 3822–3824, Apr. 2004, doi: 10.1063/1.1745104.

[13] L. Pichon, A.-C. Salaün, G. Wenga, R. Rogel, and E. Jacques, "Ammonia sensors based on suspended silicon nanowires," *Procedia Engineering*, vol. 87, pp. 1003–1006, 2014, doi: 10.1016/j.proeng.2014.11.329.

[14] P. Dai, A. Gao, N. Lu, T. Li, and Y. Wang, "A back-gate controlled silicon nanowire sensor with sensitivity improvement for DNA and pH detection," *Japanese Journal of Applied Physics*, vol. 52, no. 12R, Art. no. 121301, Nov. 2013, doi: 10.7567/jjap.52.121301.

[15] O. Knopfmacher, D. Keller, M. Calame, and C. Schönenberger, "Dual gated silicon nanowire field effect transistors," *Procedia Chemistry*, vol. 1, no. 1, pp. 678–681, Sep. 2009, doi: 10.1016/j.proche.2009.07.169.

[16] C.-M. Lee and B.-Y. Tsui, "A high-performance 30-nm gate-all-around Poly-Si nanowire thin-film transistor with NH_3 plasma treatment," *IEEE Electron Device Letters*, vol. 31, no. 7, pp. 683–685, Jul. 2010, doi: 10.1109/led.2010.2049564.

[17] B. Le Borgne, A.-C. Salaün, and L. Pichon, "Electrical properties of self-aligned gate-all-around polycrystalline silicon nanowires field-effect transistors," *Microelectronic Engineering*, vol. 150, pp. 32–38, Jan. 2016, doi: 10.1016/j.mee.2015.11.001.

[18] T.-C. Liao *et al.*, "Novel gate-all-around Poly-Si TFTs with multiple nanowire channels," *IEEE Electron Device Letters*, vol. 29, no. 8, pp. 889–891, Aug. 2008, doi: 10.1109/led.2008.2001176.

[19] T. Thingujam, Q. Dai, E. Kim, and J.-H. Lee, "A simulation study on the effects of interface charges and geometry on vertical GAA GaN nanowire MOSFET for low-power application," *IEEE Access*, vol. 9, pp. 101447–101453, 2021, doi: 10.1109/access.2021.3097367.

[20] S. Sato *et al.*, "Effects of corner angle of trapezoidal and triangular channel cross-sections on electrical performance of silicon nanowire field-effect transistors with semi gate-around structure," *Solid-State Electronics*, vol. 65–66, pp. 2–8, Nov. 2011, doi: 10.1016/j.sse.2011.06.011.

[21] M. Najmzadeh, M. Berthomé, J.-M. Sallese, W. Grabinski, and A. M. Ionescu, "Electron mobility extraction in triangular gate-all-around Si nanowire junctionless nMOSFETs with cross-section down to 5nm," *Solid-State Electronics*, vol. 98, pp. 55–62, Aug. 2014, doi: 10.1016/j.sse.2014.04.007.

[22] SILVACO, "ATLAS user's manual," *SILVACO International*, 2004. Accessed: May 12, 2023. [Online], Available: https://www.eng.buffalo.edu/~wie/silvaco/atlas_user_manual.pdf

[23] L. Pichon, E. Jacques, R. Rogel, A. C. Salaun, and F. Demami, "Variable range hopping conduction in N- and P-typein situdoped polycrystalline silicon nanowires," *Semiconductor Science and Technology*, vol. 28, no. 2, p. 25002, Dec. 2012, doi: 10.1088/0268-1242/28/2/025002.

[24] T.-K. A. Chou and J. Kanicki, "Two-dimensional numerical simulation of solid-phase-crystallized polysilicon thin-film transistor characteristics," *Japanese Journal of Applied Physics*, vol. 38, no. 4S, p. 2251, Apr. 1999, doi: 10.1143/jjap.38.2251.

[25] F. Demami, "Polycrystalline silicon nanowire FET performance depending on density of states," *Journal of Computational Electronics*, vol. 22, no. 4, pp. 946–953, May 2023, doi: 10.1007/s10825-023-02034-8.

[26] M. Gritsch, H. Kosina, T. Grasser, and S. Selberherr, "Revision of the standard hydrodynamic transport model for SOI simulation," *IEEE Transactions on Electron Devices*, vol. 49, no. 10, pp. 1814–1820, Oct. 2002, doi: 10.1109/ted.2002.803645.

[27] C.-C. Tsai *et al.*, "High-performance short-channel double-gate low-temperature polysilicon thin-film transistors using excimer laser crystallization," *IEEE Electron Device Letters*, vol. 28, no. 11, pp. 1010–1013, Nov. 2007, doi: 10.1109/led.2007.908473.

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