International Journal of Electrical and Computer Engineering (IJECE)
Vol. 15, No. 2, April 2025, pp. 2513~2522
ISSN: 2088-8708, DOI: 10.11591/ijece.v15i2.pp2513-2522

Efficient power optimized very-large-scale integration architecture of proportionate least mean square adaptive filter

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Article Info

Article history:

Received Jul 7, 2024
Revised Nov 25, 2024
Accepted Dec 2, 2024

Keywords:

Delayed least mean square algorithms
Delayed wavelet μ-law proportionate least mean square
Field-programmable gate array
Filter
Least mean square
Proportionate least mean square
Very-large-scale integration

ABSTRACT

The focus on power optimization in embedded systems is especially important for embedded applications since it has brought in many methods and factors that are necessary for developing systems that are both power- and area-efficient. In contrast to the current delayed wavelet μ-law proportionate least mean square (DWMPLMS) and delayed least mean square (DLMS) algorithms, this work offers the development of adaptive filters based on the least mean square (LMS) method, which improves power and timing performance. In order to improve area and time efficiency, the proportionate least mean square (PLMS) algorithm's architecture has been modified to remove delay, add a proportionate gain block, design for a fixed length, include an approximate multiplier block, and swap out standard blocks for floating-point adder and divider blocks. According to a power and temporal comparison with the DWMPLMS and DLMS algorithms, field-programmable gate array (FPGA) synthesis reduces power usage by 95% for a 32-bit filter length in PLMS when compared to the above methods.

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1. INTRODUCTION

Adaptive filters adjust their transfer functions based on optimization algorithms to adapt to changes in the operating environment, making them effective for sparse system identification. Among these, the least mean square (LMS) adaptive filter is widely used due to its simplicity, avoiding correlation functions and matrix inversions while offering good convergence performance. However, LMS has limitations, including a feedback error time lag that hinders pipeline implementation at high sampling rates and sensitivity to input scaling, complicating learning rate selection.

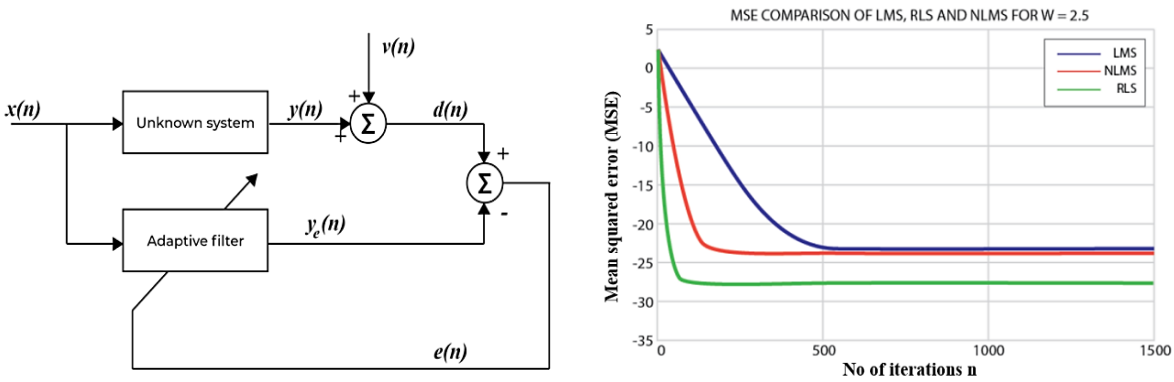
The delayed least mean square (DLMS) architecture in [1] demonstrated effective error convergence through MATLAB® Simulink modeling. The proportionate least mean square (PLMS) architecture in [2] further clarified PLMS fundamentals, enabling enhanced simulations. Although the novel design in [3] achieved power and timing efficiency, it required more area. This inspired our design, which optimizes area at a slight timing complexity cost.

Replacing multipliers with logarithmic and anti-logarithmic computations, as discussed in [4], improved time efficiency but increased power consumption. Thus, we adopted an 8-bit Vedic multiplier from [5]–[12] for better latency and power performance. Adder selection, informed by [13]–[20], and insights from systolic architectures in [21]–[29] contributed to our design's faster convergence. Studies [30], [31] highlighted the accuracy and wide range benefits of floating-point arithmetic, guiding the efficient implementation of floating-point operations in our design.

2. RESEARCH METHOD

The block diagram shown in Figures 1 (a) and 1(b) represents the block diagram of the adaptive filter as an unknown system identifier and convergence graph for different algorithm respectively. Both the adaptive filter as well as the unknown system are given the same inputs. The output that occurs across the unknown system will be the desired signal $d(n)$.

The input vector $U(n)$ is the result of further encoding the input provided by the adaptive filter into digital binary data. In the filter, the tap length determines the filter's order. Simple convolution is used to calculate the adaptive filter's output, which will initially have some unknown weights. If there is a discrepancy between this output and the intended output, it is passed back to the weight update block to provide new coefficients.



(a) (b)

Figure 1. Analysis and performance evaluation of the adaptive filter system: (a) block diagram of the adaptive filter illustrating the key components and signal flow and (b) convergence graph comparing the performance of different algorithms in terms of error reduction over iterations

This process continues to happen till the error signal ideally goes down to zero. If the error signal is zero it implies that:

a. The output of the adaptive filter is same as that of the output of the unknown system, *i.e.* $Y(n) = d(n)$ (because $e(n) = Y(n) - d(n)$).
b. If $Y(n) = d(n)$ it suggests that the adaptive filter is producing the same output as the unknown system for a given input and hence the coefficients of both the unknown system and the adaptive filter are the same. So therefore, the adaptive filter is said to have identified the unknown system under test.

The mathematical equations that will be used to find out the filter output, the error signal and the updated weights are as given in Table 1.

Table 1. Adaptive filter equations

Function	Equation
Input vector	$X(k) = [x(k), x(k-1), \ldots, x(k-L+1)]T$
Filter output	$Y(k) = xT(k)W(k)$
Error signal matrix	$E(k) = d(k) - Y(k)$
Updated weights	$W(k+1) = W(k) + \beta g(k)X(k)E(k)$
Identity matrix	$g(k) = I$

Note: $w(k)$ is set of current weights, β is adaptive step size, and $g(k)$ is gain matrix

The novel implementations on our design would be: i) A proposed floating point module approach for the PLMS register transfer level implementation and ii) Implementing an area efficient architecture for PLMS algorithm based adaptive filter implementation on FPGA's. The PLMS update equation is given by (1):

$$w(n+1) = w(n) + G(n)u(n)e(n) \tag{1}$$

The Pt-NLMS family of algorithms iteratively estimate the filter weights

$$w(n) = [w0(n), w1(n), \dots, w(L-1)(n)]^T \tag{2}$$

The Gain matrix $G(n)$ is explained in (3),

$$G(n) = diag\left(g_0(n), g_1(n), \dots., g_L - 1\ (n)\right) \tag{3}$$

and a gain factor $g_i(n)$ is assigned to the ith tap in proportion to $|w_i(n)|$

$$g_i(n) = \frac{w(n)}{\frac{1}{L}\sum_{L-1}^{i=0} wi(n)} \tag{4}$$

For the simplified PLMS algorithm, $\gamma_i(n)$ for each tap is evaluated as

$$\gamma_i(n) = F[|w_i(n)| + \rho] \tag{5}$$

and

$$F[|w_i(n)|] = |w_i(n)| \tag{6}$$

The Pt-LMS algorithm simplifies its predecessors by omitting weighted normalization and simplifying gain factor evaluation, with a small constant p ensuring minimum gain for inactive coefficients and reducing time complexity. These changes improve area and power efficiency, but high time complexity remains due to repeated gain matrix and weight updates. Delayed adaptation addresses this issue, leveraging the unchanged error gradient despite delays.

$$w(n+1) = w(n) + \mu G(n-M)u(n\ -\ M)e(n-M) \tag{7}$$

When we compare the results of Pt-LMS with other LMS algorithm we observe that the convergence performance of Pt-LMS is comparatively better than that of other LMS algorithms and its convergence performance can be improved further. It is also observed that Pt-LMS is real time flexible and robust. Hence, we decided to move forward with PLMS.

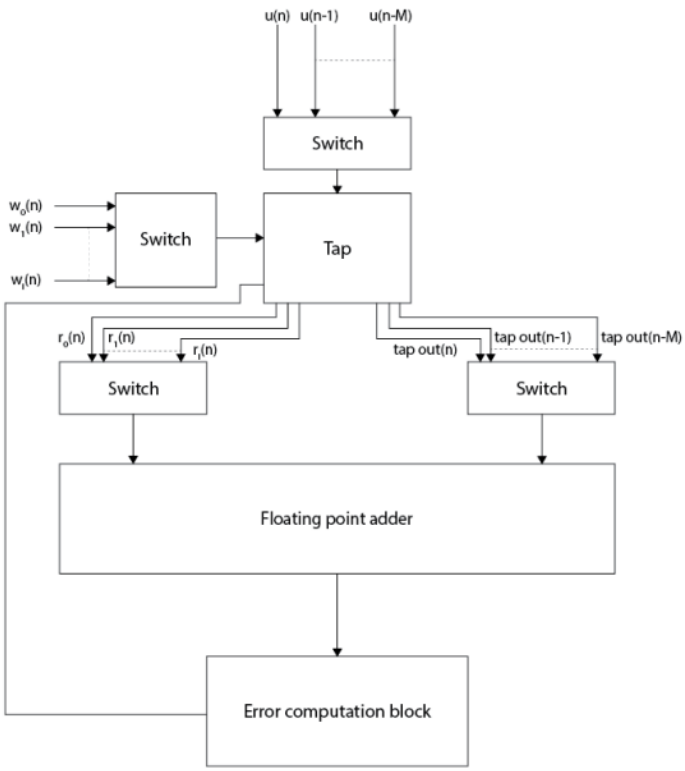
3. ARCHITECTURE

3.1. Proposed PLMS architecture

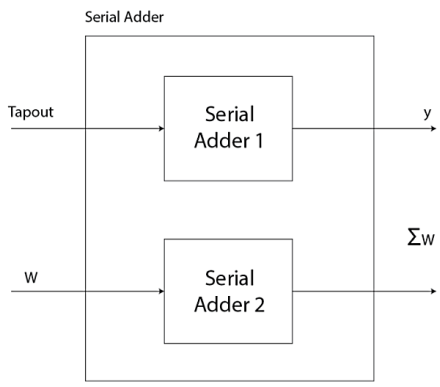
Figure 2 shows the proposed PLMS architecture and floating-point adder block respectively. As illustrated in Figure 2(a); to implement pipelining, the number of taps increases with the order of the filter, which significantly impacts the area. Additionally, switches are placed after every two taps to manage the tap-out and gamma function at the corresponding clock phases. While these switches help reduce timing complexity, their large number contributes to increased area. Instead of connecting the regressor input and initial weights directly to the taps, they are routed through a switch. Depending on the clock phase, each filter coefficient and input pass through a floating-point multiplier, which accelerates the multiplication process and generates the tap-out (n) and gain function. These outputs are directed to switch 2. After all the outputs are generated from a single tap, switch 1 is activated during one clock phase and switch 2 in the next. When switch 1 is active, the adder sums the tap-outs, providing the adaptive filter output, and when switch 2 is active in the following phase, the sum of the weighted functions is obtained.

The inputs to the serial adder block, as shown in Figure 2(b), come from a switch that receives partial filter outputs and gain factors from the corresponding taps over four successive switching cycles. The switch sends these tap-outs to the adder only after it has received the partial outputs from all N input samples. Since the inputs are 32-bit floating-point values, the tap-out, which is the product of the input x and weight W, also results in a 32-bit floating-point value. Therefore, a 32-bit floating-point adder is required to combine the partial filter outputs and generate the complete filter output. This architecture employs a 32-bit floating-

point adder (FPA) due to its ability to handle a wide range of numbers with high precision. Since the IEEE 754 32-bit floating-point format separates the exponent and mantissa, adding two floating-point numbers involves adding their mantissas, with a specific number of shifts applied to the mantissa of the number with the smaller exponent.



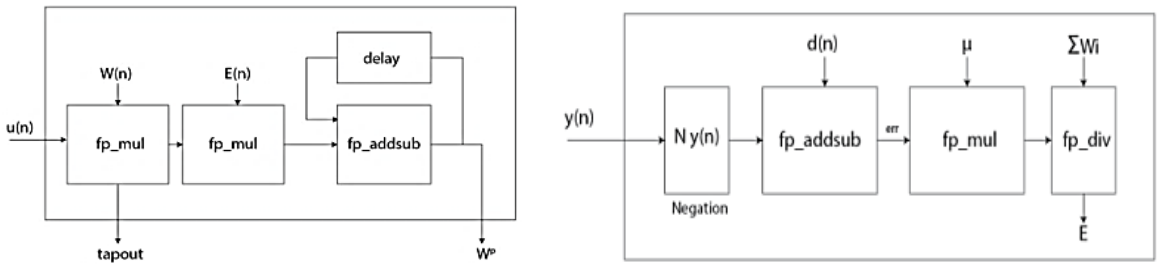
(a)



(b)

Figure 2. Representation of the proposed architecture components: (a) proposed PLMS architecture showcasing the pipeline and control mechanism and (b) floating-point adder block used for accurate computation of weights and updates

Figures 3(a) and 3(b) represent the tap block and error computation block respectively. The tap block architecture computes the gain factor and partial filter output using a 32-bit floating-point multiplier. The tap also receives an input, $E(n-M)$, from the error computation block. The system output, $y(n-i)$, is the sum of the tap outputs from the current and previous iterations. The error signal is subtracted from the actual output and fed back to the tap block, updating the weights for the next iteration. A serial adder sums the L previous tap outputs and weights for the gain factor and system output.



(a) (b)

Figure 3. Illustration of the key components in the adaptive filter architecture: (a) tap block for managing the input data and weight updates and (b) error computation block for determining the error signal to refine the filter's performance

3.2. Floating point modules architecture

We propose efficient floating-point (FP) arithmetic units, including FP addition, subtraction, multiplication, and division, for fast computation using single-precision IEEE 754 format. This 32-bit format includes a 1-bit sign (1 for negative, 0 for positive), an 8-bit exponent, and a 23-bit mantissa for high-range data representation.

$$X = (-1^{sign} x 2 \exp(1.man)) \tag{8}$$

where $sign$ is sign of the number X, exp is exponential value of a number, and man is mantissa value of the number.

3.2.1. Floating point adder/subtractor

Figure 4 shows the floating-point adder where the larger exponent is taken as common, and the mantissa of the smaller exponent is left-shifted by the exponent difference before addition. The mantissas are added, and any carry is added to the exponent while left-shifting the result. The sign bit is determined by XOR-ing the input signs. The process involves an exponent comparison block to align exponents, a mantissa block for addition/subtraction based on sign bits, and a normalization block for adjusting the final 32-bit result. Normalization shifts the mantissa based on carry/borrow, producing the final exponent and mantissa values.

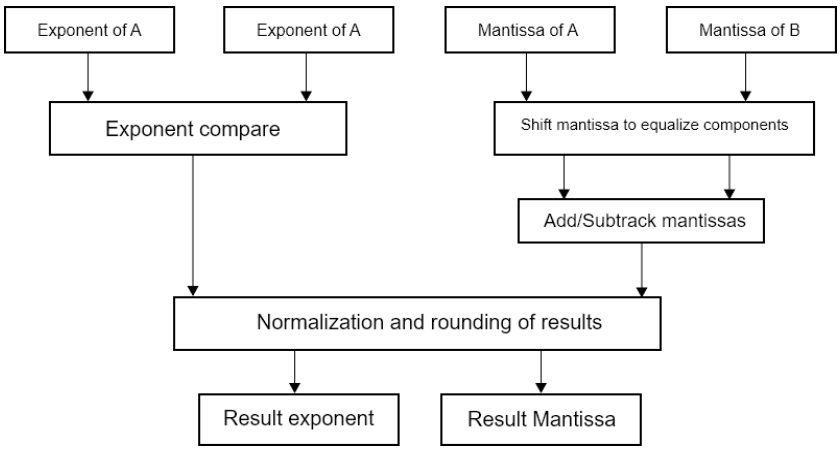


Figure 4. Floating point adder

3.2.2. Multiplication and division of two floating point value

Figure 5 shows the floating-point multiplier and floating-point divider respectively. The sign bit is obtained by XOR-ing the input sign bits. The mantissas are processed through a 23-bit adder and a Vedic multiplier for accuracy, with their results summed by another 23-bit adder. The combined carry from both adders is used in a shifter block and added to the exponent sum, yielding the final result's exponent and

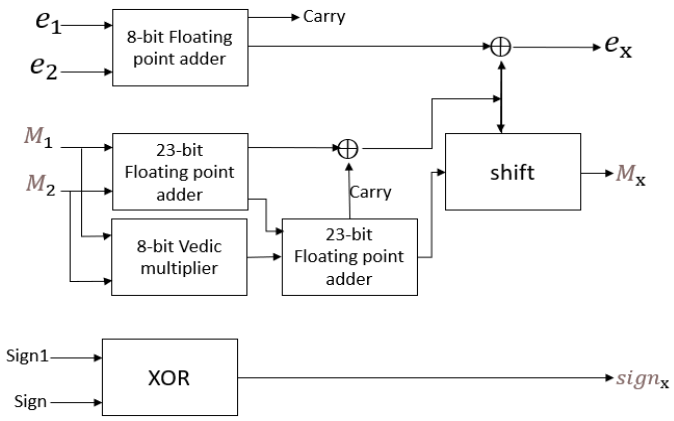
mantissa. Complex multiplication of two 32-bit floating-point (FP) values are broken down into simple module design as shown in Figure 5(a).

$$X1 = (-1)^{sign1} * (2^{e1}) * (1.m1) \tag{9}$$

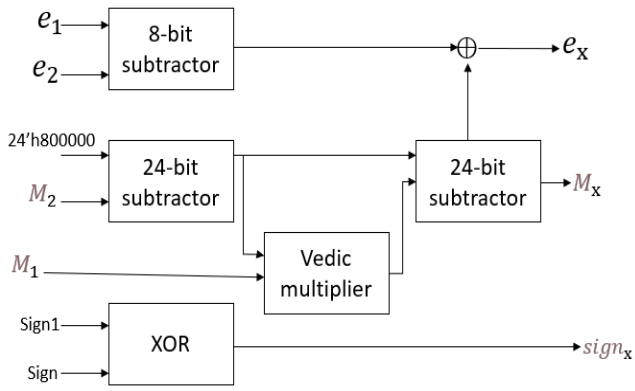
$$X1 = (-1)^{sign2} * (2^{e2}) * (1.m2) \tag{10}$$

where $X1$, $X2$ are values expressed in form of single precision floating point format; $sign1, sign2$ are the sign of number X; $e1$, $e2$ are the exponential value; and $m1$, $m2$ are the mantissa value.

Complex division of two 32-bit floating-point values is simplified as shown in Figure 5(b). The sign bit is obtained by XOR-ing the input signs. The second mantissa is subtracted from $24'h80000024$ and the result is multiplied with the first mantissa using a Vedic multiplier. The outputs are added to form the result's mantissa, while the carry is added to the exponent block for the final result's exponent.



(a)



(b)

Figure 5. Key computational blocks of the floating-point unit: (a) Floating-point multiplier for efficient multiplication operations and (b) Floating-point divider for precise division computations

4. RESULTS AND DISCUSSION

4.1. MATLAB results

This system was built to analyze any type of input signal which is generated by a signal generator, the same signal is been passed to unknown system and adaptive system and results in error convergence effectively. Once we achieved satisfactory results, we started the synthesis. The Simulink diagram can be seen in Figure 6(a). Figure 6(b) presents the Simulink model results for the adaptive filter, showing the desired signal, the filter's output, and the error signal. The third graph demonstrates error convergence over time. Figure 6(c) shows the register transfer language (RTL) schematic of PLMS algorithm using Libero SOC version 11.9 with FPGA A3P1000L from ProASIC3L series.

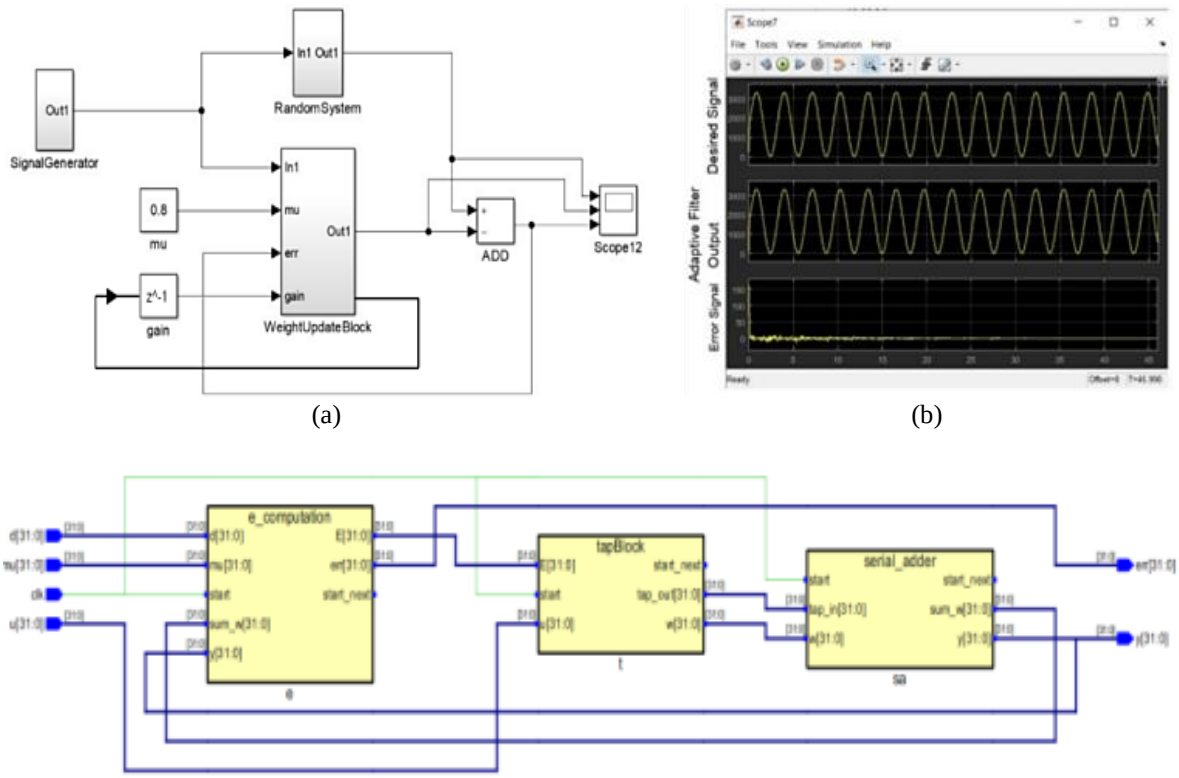


Figure 6. Comprehensive analysis and implementation of the proposed PLMS architecture: (a) Simulink model of the proposed PLMS architecture, (b) Simulink result for sine wave demonstrating the system response, and (c) RTL schematic representing the hardware implementation of the PLMS algorithm

4.2. Synthesis results

Tables 2 and 3 represents the characteristics of proposed PLMS and comparison with existing architectures respectively. Figures 7(a) and 7(b) show the graphical comparison power-delay comparison and timing comparison with referred algorithms with existing DLMS and DWMPLMS architectures respectively. Table 3 shows that the proposed design reduces power consumption by up to 95%, with savings of 95% and 88% compared to the DWMPLMS and DMPLMS architectures, respectively. This efficiency stems from replacing the logarithmic multiplier with a floating-point Vedic multiplier, which enhances power efficiency. The pipelined tap block design further improves timing, making the proposed architecture 30 times faster than logarithmic methods and the DLMS design. Fixed-point computations in DLMS are less efficient, with the proposed floating-point blocks achieving 84% power savings.

Table 2. Characteristics of proposed PLMS

Architecture	Power (mW)	Delay (ns)
DWMPLMS (Mula *et al.* [2])	19.43	3.31
DLMS (Meher and Park [1])	10.06	3.28
DLMS (Fan *et al.* [21])	12.56	3.27
DMPLMS [2]	14.13	3.31
Proposed (PLMS)	1.067	104.45

Table 3. Comparison with existing architectures

Metric	Value
Number of slices LUT's used	4094
Number of IO cells used	161
Device power consumption	1.067 mW
Operating frequency/timing	9.5 MHz
Operating timing	104 ns

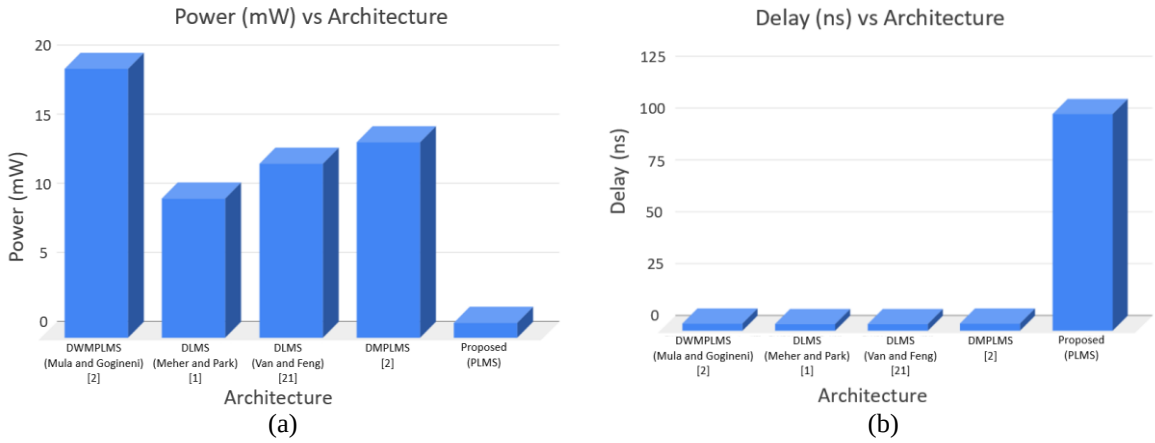


Figure 7. The graphical: (a) power comparison and (b) timing comparison, with referred algorithms

5. CONCLUSION

This paper proposes an adaptive filter design that leverages the PLMS algorithm, which is applied to a 32-bit filter length. The PLMS algorithm is selected due to its ability to achieve a lower mean-square-deviation (MSD) compared to the traditional LMS algorithm, resulting in better performance. Additionally, PLMS offers faster convergence than the DLMS algorithm, making it a more efficient choice in terms of area, power, and timing.

The proposed design replaces the logarithmic approach in existing DWMPLMS and DMPLMS architectures with floating-point computation, a Vedic multiplier, and a proportionate gain block. A pipelined architecture in the tap block enhances efficiency, while the design includes approximate multipliers, floating-point adders, and divider blocks. FPGA synthesis shows a 92% power reduction compared to existing architectures. Future work focuses on reducing area, improving timing, and fine-tuning output performance.

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