

Circulating current suppression and natural voltage balancing using phase-shifted modulation for modular multilevel converter

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ABSTRACT

The challenge of achieving a balanced capacitor voltage is one of the factors affecting the efficient operation of modular multilevel converters (MMC). This paper investigates this challenge through a proposed method that utilizes a high carrier frequency phase-shifted pulse width modulation (PS-PWM) scheme. This method aims to achieve natural balancing without the need for any additional control mechanisms. Moreover, the number of output voltage levels is affected by the phase shift between the carriers of the upper and lower arms. When there is no phase shift, $N+1$ discrete levels are achieved, but when there is a phase shift, the number of discrete levels increases to 2^{N+1} . The proportional-resonant (PR) controller and moving average filter (MAF) are employed to decrease the capacitor voltage ripples by suppressing the fourth and second harmonics in the circulating currents. The MMC inverter structure is modeled and simulated in the PLECS and MATLAB/Simulink environments to evaluate the impact of this control scheme on the converter's performance.

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1. INTRODUCTION

In 2003, Professor Marquardt was the first researcher to introduce the modular multilevel converter (MMC) [1]. Since then, it has attracted considerable attention and interest in the academic and industrial fields. After eight years of intensive research done on MMC, the Trans Bay cable project was the first industrial application based on this technology. Siemens introduced the project under the name high-voltage direct current (HVDC) Plus in 2010, marking a significant milestone in the industry application of MMCs. This project becomes the earliest HVDC transmission system implemented employing MMC technology. Since then, Alstom and ASEA Brown Boveri (ABB) have launched their MMC-HVDC [2]. In addition, MMC technology has other commercial applications such as medium-voltage motor drives [3], static synchronous compensators (STATCOMs) [4], multi-terminal MMC-based HVDC systems [5], and MMC-HVDC-base offshore wind farms [6], [7]. However, some MMC applications are in the theoretical research stage such as grid integration of solar photovoltaic systems [8], battery energy storage systems (BESS) [9], and hybrid electric vehicle drives [10].

Renewable energy integration, particularly photovoltaic systems, into the grid has garnered significant attention in the published literature. As a result, several publications have highlighted the implementation of MMCs in photovoltaic (PV) systems. Rong *et al.* [11] proposes a new way to connect the PV module directly to each sub-module capacitor, as opposed to the traditional method of connecting the PV array to the direct

control (DC) link of the MMC, with and without a DC/DC circuit. This configuration requires an extra redundant module to compensate for voltage loss resulting from fluctuations in irradiance. However, the authors in [12] improved the control method proposed in [11] by developing a way to control the MMC without additional redundancy modules. Another project under study that combines solar, wind generation, and battery storage will become operational in 2027. The energy produced from a clean energy facility in Morocco will be transmitted to the UK through subsea HVDC cables [13].

The mentioned applications in both commercial and research levels confirm the importance of this topology in low, medium, and high-voltage applications. The utilization of MMC technology in a large-scale application becomes possible due to its attractive characteristics, such as its capacity to scale in terms of voltage and power levels, which result in the reduction of harmonic distortion and minimized filter design. Other advantages of MMC are high modularity, low stress on switching devices, high efficiency, and high reliability improved by redundancy [14]. However, controlling MMC becomes more complex because of the significant number of submodules present. In addition, several technical challenges must be considered, such as output current control, minimization of switching frequency, capacitor voltage balancing [15], [16], suppression of circulating current [17]–[22], and reduction of capacitor voltage ripples [23].

The main objective of this paper is to demonstrate that it is possible to achieve a natural balancing of capacitor voltages without utilizing any balancing control. It is accomplished by employing a high carrier frequency of phase-shifted pulse width modulation (PS-PWM) and implementing a circulating current controller based on a proportional-resonant (PR) controller and a moving average filter (MAF). The organization of this paper is as follows: section 2 presents the topology and mathematical model of the modular multilevel converter. In the third section, the control method for capacitor voltage balancing and the circulating current suppression is described. Section 4 presents and compares the simulation results. Finally, section 5 provides a brief conclusion.

2. TOPOLOGY AND MATHEMATICAL MODEL OF MMC

2.1. MMC topology

The MMC scheme, depicted in Figure 1, works as an inverter connected to a passive load. This converter includes six arms, with two arms per phase. Each arm is composed of multiple submodules (SMs) connected in series, an arm inductor (L_{arm}), and a resistor (R_{arm}). In addition, by adjusting the switching states of the submodules, each arm can act as a controllable voltage source allowing the converter to synthesize a desired output voltage waveform.

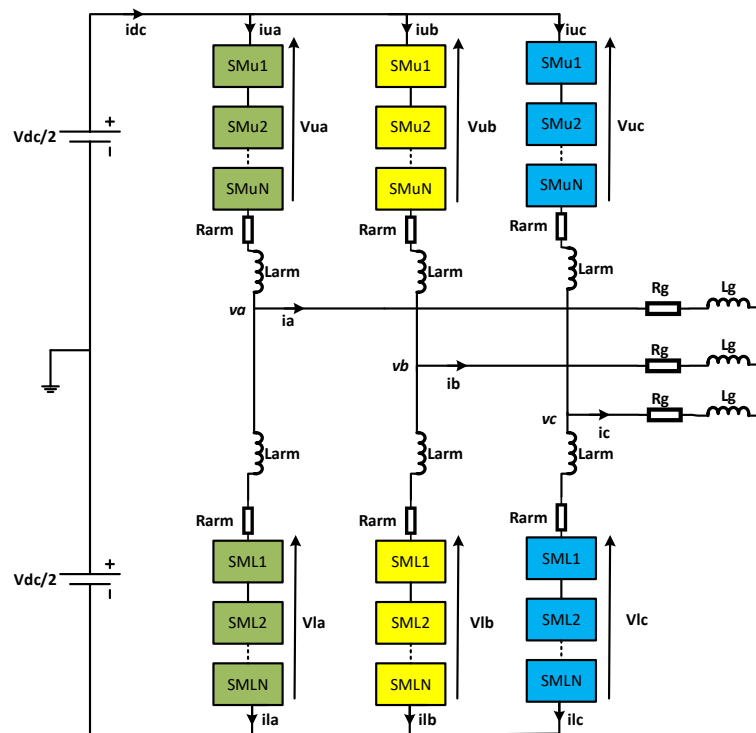


Figure 1. MMC system in the three-phase configuration

Several submodule topologies have been studied in the literature, classified as either unipolar or bipolar based on their ability to generate voltages of single or both polarities at their output terminals. The most commonly used SMs topology in MMCs is the half-bridge and full-bridge configurations [24], as shown in Figure 2. The half-bridge configuration is the simplest topology, composed of two insulated-gate bipolar transistors (IGBTs), two freewheeling diodes, and a floating capacitor, as shown in Figure 2(a). The output voltage of a submodule can either be V_C (during the inserted state) or zero (during the bypassed state), depending on the gate signal.

The full-bridge configuration is composed of four IGBTs, four freewheeling diodes, and a capacitor, as shown in Figure 2(b). Half-bridge topology is widely used because of its simple control and low number of switching devices. However, this topology does not have the blocking capability of DC-side faults as full-bridge topology.

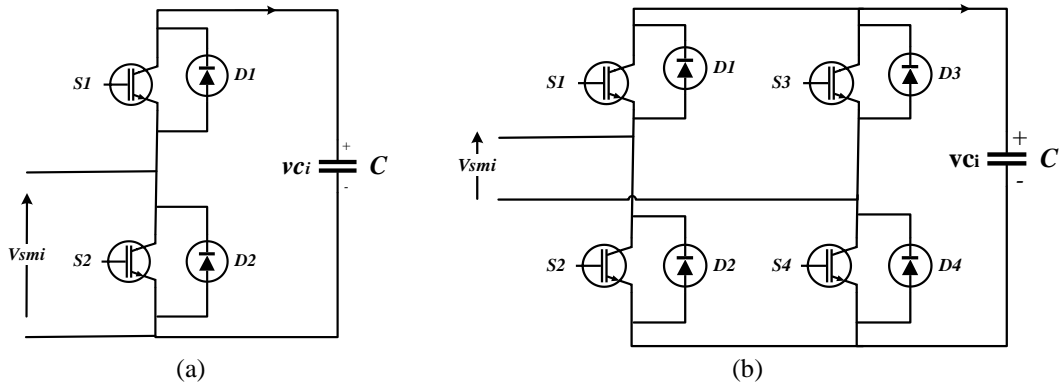


Figure 2. Submodule configuration (a) half-bridge and (b) full bridge

2.2. Mathematical model of MMC

From Figure 1 the phase current i_j can be expressed by the upper and lower arm currents as (1),

$$i_j = i_{uj} - i_{lj} \quad (1)$$

where i_j is the current of phase j ($j = a, b, c$). i_{uj} and i_{lj} are the currents of the upper and lower arm, respectively. The upper v_{uj} and lower v_{lj} arm voltage for phase j , respectively. They can be described as (2) and (3).

$$v_{uj} = \frac{V_{dc}}{2} - v_j - R_{arm} i_{uj} - L_{arm} \frac{di_{uj}}{dt} \quad (2)$$

$$v_{lj} = \frac{V_{dc}}{2} + v_j - R_{arm} i_{lj} - L_{arm} \frac{di_{lj}}{dt} \quad (3)$$

v_j is the output voltage of the phase j and V_{DC} is the DC-bus voltage.

The output voltage v_j is determined by subtracting (2) from (3) and using (1).

$$v_j = \frac{v_{lj} - v_{uj}}{2} - \frac{R_{arm}}{2} i_j - \frac{L_{arm}}{2} \frac{di_j}{dt} \quad (4)$$

The driving voltage e_j of output current i_j is expressed as (5).

$$e_j = \frac{v_{lj} - v_{uj}}{2} \quad (5)$$

The unbalance voltage $v_{diff,j}$ of phase j is determined by adding (2) and (3),

$$v_{diff,j} = \frac{V_{dc} - (v_{lj} + v_{uj})}{2} = R_{arm} i_{diff,j} + L_{arm} \frac{di_{diff,j}}{dt} \quad (6)$$

where i_{diffj} is the circulating current in phase j , which can be represented as the mean value of the upper and lower arm currents, is denoted by (7).

$$i_{diffj} = \frac{i_{uj} + i_{lj}}{2} \quad (7)$$

The circulating current i_{diffj} can be described by (8).

$$i_{diffj} = \frac{I_{DC}}{3} + i_{diffjAC} \quad (8)$$

The circulating current is composed of a DC component, which is equal to one-third of I_{DC} corresponding to the power exchange between the DC link and the converter. Additionally, the alternative current (AC) components, especially the second and fourth harmonics, are induced as a consequence of the capacitor voltage variations [20]. The average voltage of the upper and lower arms controls the circulating current. This voltage v_{sumj} can be expressed as (9).

$$v_{sumj} = \frac{v_{uj} + v_{lj}}{2} \quad (9)$$

3. CONTROL OF MMC

3.1. Modulation scheme

The gate signals for each submodule in the arm of each phase are generated by phase shifted PWM modulation. This modulation technique achieves a natural balance of submodule capacitor voltage without requiring a balancing algorithm. To achieve this, N triangular carriers, which are equivalent to the number of submodules in each arm, are used in this technique, as depicted in Figure 3. The carriers in the same arm have the same carrier frequency but are phase-shifted by $360^\circ/N$ between them [25]. The interleave angle between the upper and lower carriers determines the number of output levels. In the absence of an interleave angle, the converter produces $N+1$ output levels. Figure 3(a) shows the carrier arrangement of the upper and lower arm without an interleave angle. When there is an interleave angle of $180^\circ/N$ between the carriers in the upper and lower arms, as shown in Figure 3(b), the converter generates $2N+1$ voltage levels.

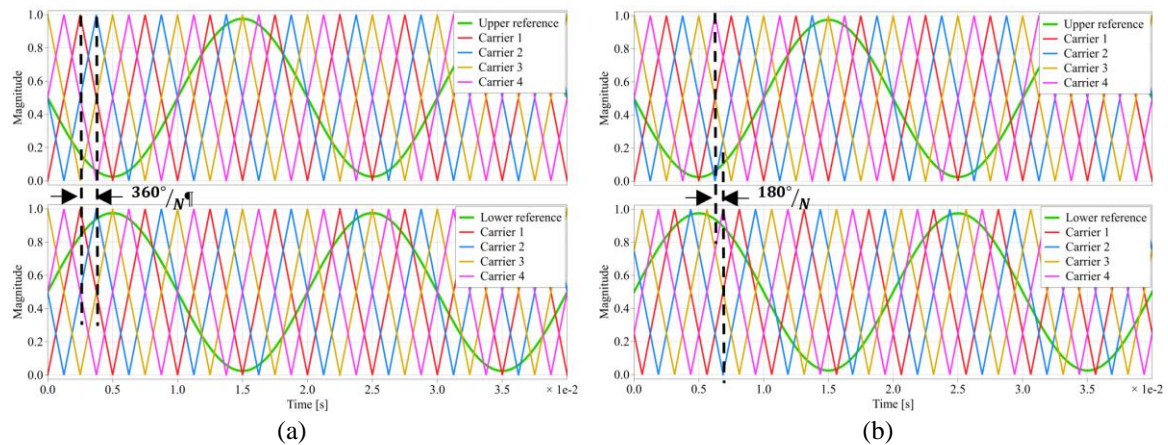


Figure 3. PS-PWM carriers' arrangement of the upper and lower arm (a) without interleave angle and (b) with interleave angle

3.2. Control method

The proposed method is based on a circulating current controller and an output voltage reference generator. In addition, this method does not need a balancing voltage control because of the properties of PS-PWM, which generates almost the same gate signal for each submodule [26]. As a consequence, an identical amount of energy is extracted from each submodule, resulting in a natural balancing of capacitor voltage. Merwe *et al.* [27] provide a comprehensive mathematical proof of the natural balancing mechanism under PS-PWM, highlighting its dependency on the values of all the circuit elements and the harmonic components

of all switching functions. Ilves *et al.* [28] have provided an explanation of how to select an appropriate switching frequency to maintain balanced capacitor voltages.

Figure 4 illustrates the control structure. Figure 5 shows the equivalent circuit of the three-phase MMC deduced from (6) and (9). The circuit illustrates that this current flows through the three phases of the converter without affecting the AC side. The circulating current contains a DC component equal to one-third of I_{DC} and undesired AC harmonics. The control objective is to suppress the AC components, especially the double fundamental harmonic, which is the dominant one. Figure 6 shows a diagram of the circulating current control based on a proportional-resonant (PR) controller. The circulating current reference i_{diffj}^* is obtained from a MAF. The block diagram of the MAF is shown in Figure 7, where T_w is adjusted to be $1/2f_{grid}$ to extract the DC component of i_{diffj} which is equal to $I_{DC}/3$.

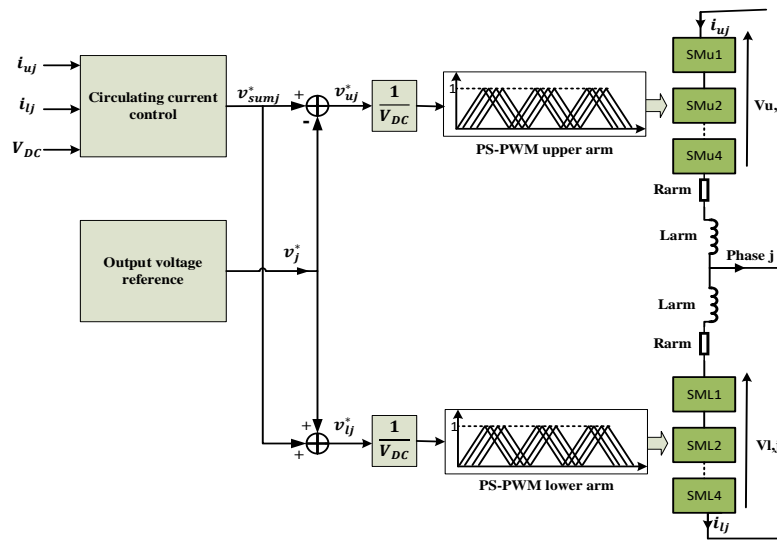


Figure 4. Control structure based on the proposed method

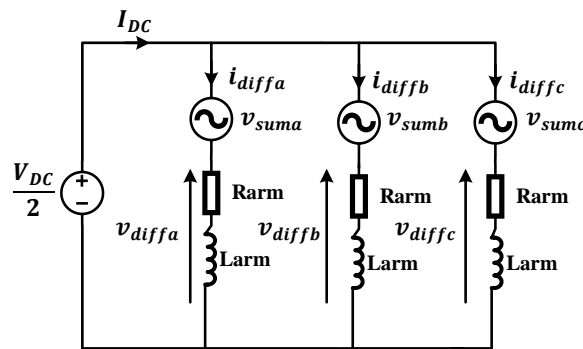


Figure 5. Equivalent circuit of MMC for circulating current

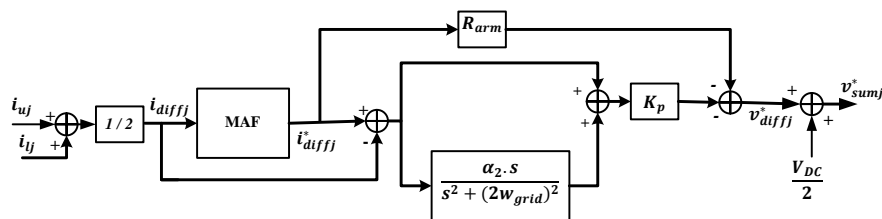


Figure 6. Diagram of the circulating current controller

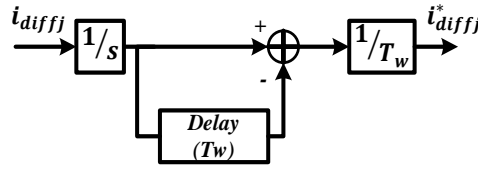


Figure 7. Block diagram of the MAF

The transfer function of a PR controller is expressed as (10).

$$G(s) = K_p \left(1 + \frac{s \cdot \alpha_2}{s^2 + (2 \cdot \omega_{grid})^2} \right) \quad (10)$$

Here, K_p is the proportional gain and α_2 is the resonant bandwidth. The tuning of parameters for PR is described in [29]. To suppress the second harmonic in i_{diffj} , the PR controller is tuned to twice the fundamental frequency ($2 \cdot f_{grid}$). The circulating current controller generates the internal voltage reference v_{sumj}^* , which is obtained by adding $V_{DC}/2$ to the unbalance voltage reference ($-v_{diffj}^*$). According to (5) and (9), the reference of the upper and lower arm voltage for each phase are defined as (11), (12).

$$v_{uj}^* = v_{sumj}^* - v_j^* \quad (11)$$

$$v_{lj}^* = v_{sumj}^* + v_j^* \quad (12)$$

The three-phase output voltage references v_j^* generated in the open loop are given as (13),

$$\begin{aligned} v_a^* &= \frac{V_{DC}}{2} m \sin(2\pi f_{grid} t) \\ v_b^* &= \frac{V_{DC}}{2} m \sin\left(2\pi f_{grid} t - \frac{2\pi}{3}\right) \\ v_c^* &= \frac{V_{DC}}{2} m \sin\left(2\pi f_{grid} t - \frac{4\pi}{3}\right) \end{aligned} \quad (13)$$

where m is the modulation index and V_{DC} is the DC-link voltage.

4. RESULTS AND DISCUSSION

A three-phase MMC connected to a passive load, as shown in Figure 1, with four SMs per arm ($N=4$), has been simulated in MATLAB/Simulink and PLECS. Table 1 summarizes the circuit parameters used in the simulations. Four scenarios are considered in the simulations; the impact of carrier frequency on the capacitor voltage balancing, output voltage levels under interleave angle, the circulating current effect on capacitor voltage ripples, and a comparison between the proposed method and the Hagiwara method.

Table 1. System parameters

Parameters	Value
Rated active power P	1 MW
Rated RMS current I	105 A
Grid inductance L_g	6 mH
Grid resistance R_g	30 Ω
Arm inductance L_{arm}	3 mH
Arm resistance R_{arm}	0.1 Ω
Number of SMs per arm N	4
DC bus voltage VDC	9 KV
Nominal SM voltage	VDC/N =2250 V
SM capacitance C	1.9 mF
Grid frequency f_{grid}	50 Hz
Carrier frequency f_c	2 KHz
Modulation index m	1
Resonant bandwidth α_2	400
Proportional gain K_p	3

4.1. Scenario 1: impact of carrier frequency on the capacitor voltage balancing

The proposed method is simulated under different carrier frequencies, with the circulating current controller activated at $t = 0$ s and no interleave angle applied in this case. Figure 8 presents the SM capacitor waveforms for the upper arm in phase A at various carrier frequencies. Figure 8(a) illustrates that the SM voltages start to diverge from the nominal value V_c^* when the carrier frequency is equal to 200 Hz; in this case, capacitors are not balanced. Figures 8(b) and 8(c) demonstrate that when the carrier frequency is above 500 Hz the natural balancing starts, and all capacitor voltages follow V_c^* . In addition, the consistency of the capacitor voltage increases with high carrier frequencies (above 2,000 Hz) as presented in Figure 8(d) when all capacitor voltages have the same shape and fluctuations. However, the MMC with high carrier frequency leads to an increase the switching losses. Table 2 presents the total harmonic distortion (THD) of both the output current and arm current, measured at varying carrier frequencies. It can be observed that higher carrier frequencies lead to a reduction in THD.

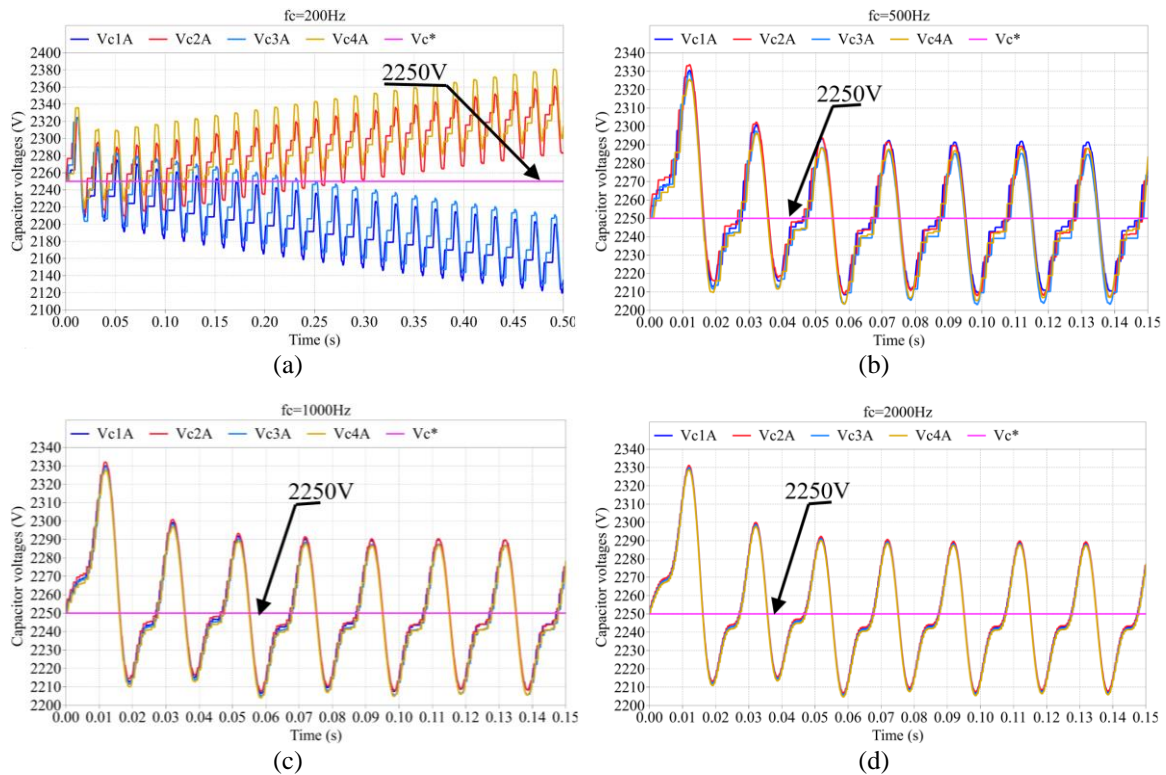


Figure 8. Capacitor voltages of upper arm for phase A under different carrier frequencies (a) $f_c = 200$ Hz, (b) $f_c = 500$ Hz, (c) $f_c = 1,000$ Hz, and (d) $f_c = 2,000$ Hz

Table 2. THD of output and arm current

f_c		3,000 Hz	2,000 Hz	1,000 Hz	500 Hz	200 Hz
THD %	i_A	1.19	1.75	3.48	6.4	12.13
	i_{uA}	1.3	1.9	3.76	7.01	14.57

4.2. Scenario 2: interleave angle and output voltage levels

The proposed method is simulated under a fixed carrier frequency and the circulating current controller is activated at $t = 0$ s. Figure 9 shows the impact of the interleave angle on the output voltage levels. From Figure 9(a), it can be observed that without the interleave angle, the number of voltage levels is five levels (2^{N+1}) in this case. It is possible to increase this number by applying an interleave angle ($180^\circ/N$) between the upper-lower arm carriers, which will improve the quality of output waveforms, as shown in Figure 9(b). In this case, nine levels (2^{N+1}) are obtained. By applying the interleave angle, the THD of the output waveforms can be reduced. However, it should be noted that this improvement is accompanied by an increase in the THD of arm current, as indicated in Table 3.

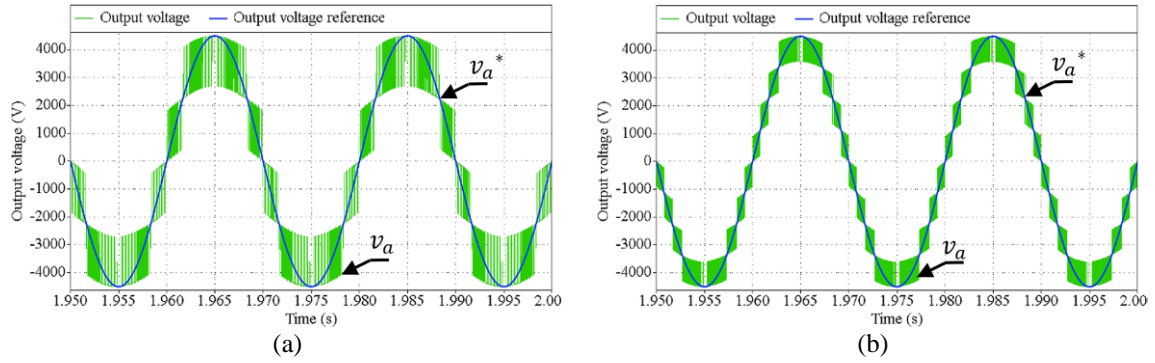


Figure 9. Output voltage v_a (a) without interleave angle and (b) with interleave angle

Table 3. Impact of interleave angle on THD

	Interleave angle	without	with
THD %	i_a	1.75	0.57
	i_{ua}	1.9	8.33
	v_a	20.93	11.04

4.3. Scenario 3: circulating current and capacitor voltage ripples

In this case, the proposed method is simulated with interleave angle and the carrier frequency is fixed at 2,000 Hz. The circulating current controller (CCC) is activated at 0.5 s, and the waveform of the circulating current in phase A and its harmonic spectra are shown in Figure 10. Figure 10(a) illustrates that before enabling the CCC, i_{diffa} oscillates around its reference value $i_{diff}^* = 37$ A. This oscillation is caused by the second and fourth harmonic in the circulating current, as shown in the harmonic spectra presented in Figure 10(b). Furthermore, the amplitude of the second harmonic is significantly higher than the fourth harmonic. After enabling the CCC, the harmonic spectra contain only a DC component, which indicates the suppression of the second and fourth harmonics. Even though tuning the CCC to twice the fundamental frequency, the fourth harmonic in i_{diffa} is removed. However, the circulating current still fluctuates around the DC component caused by the presence of a high harmonic in i_{diffa} .

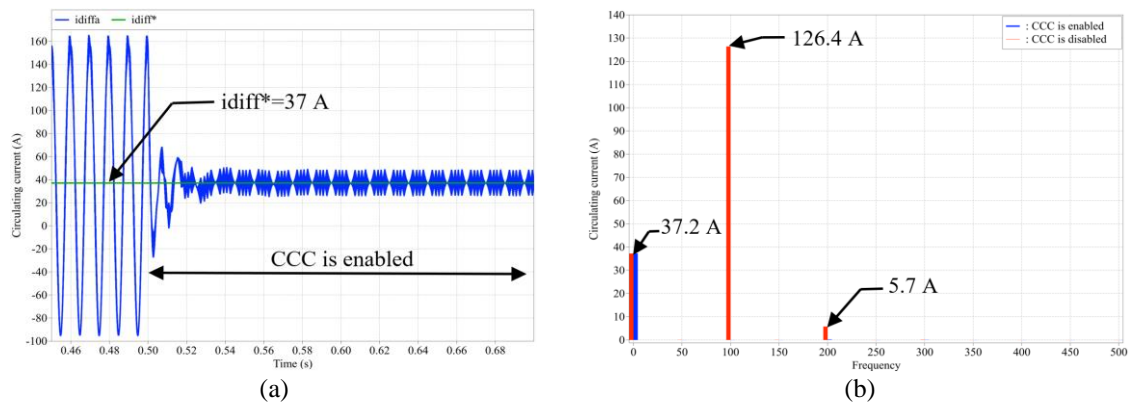


Figure 10. Circulating current in phase A (a) impact of CCC and (b) harmonic spectra of i_{diffa}

Figure 11 shows the capacitor voltages of the upper arm in phase A before and after enabling the CCC. The capacitor voltage ripples are reduced from 280 to 81 V when the CCC is enabled. In addition, all capacitors have the same average voltages, which are about 2,250 V, as shown in Figure 11(a). After the application of the CCC, the first and second harmonics in the capacitor voltage v_{c1ua} are decreased from 84 to 32 V and from 68 to 16 V, respectively, as shown in Figure 11(b). The circulating current controller does not affect the output waveforms, as depicted in Figure 12. Only their THD is improved, from 2.36% to 0.57% for the output current in Figure 12(a) and from 11.36% to 11.04% for the output voltage in Figure 12(b).

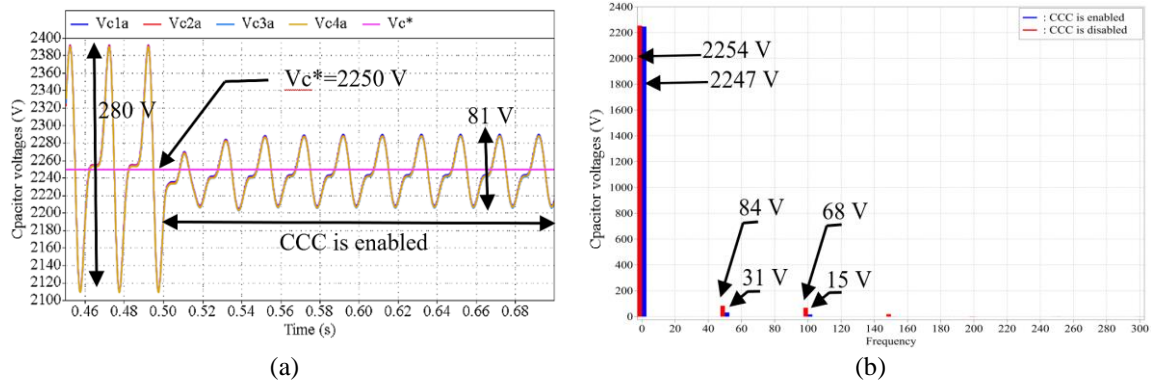


Figure 11. Capacitor voltages v_{c1ua} (a) impact of CCC and (b) harmonic spectra of v_{c1ua}

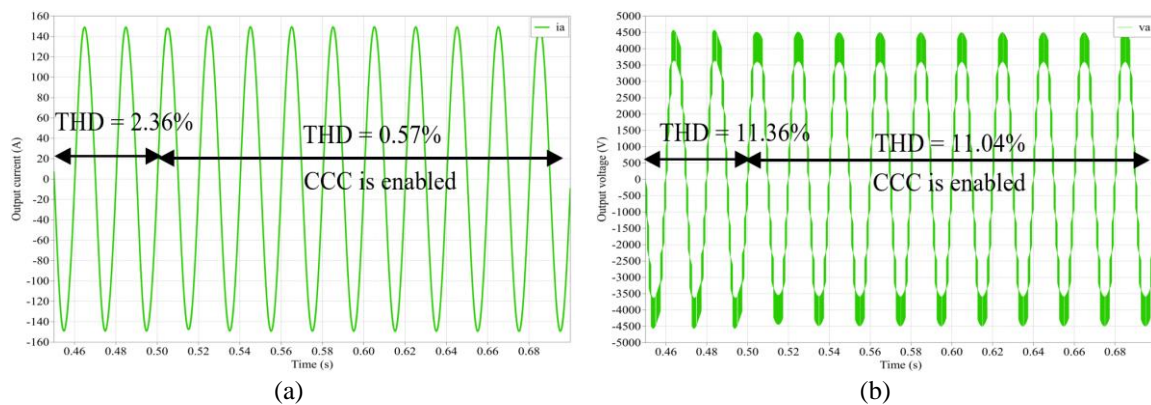


Figure 12. Output waveforms of phase A (a) output current i_a and (b) output voltage v_a

Figure 13 illustrates the impact of activating the CCC on the arm waveforms of phase A. When activating the CCC at $t = 0.5$ s, the arm's current shape is improved and becomes sinusoidal, as shown in Figure 13(a). Consequently, the harmonic content of i_{ua} , which is not represented in this case, contains only a DC component and a first harmonic. Specifically, the DC component is about 37 A, while the amplitude of the first harmonic is about 75 A once the CCC is enabled. In Figure 13(b), the upper arm voltage is shown. This waveform has five levels ($N+1$). Before the CCC is activated, its amplitude exceeds the DC link voltage of 9,000 V. This occurs due to the high ripples in the capacitor voltages. The activation of CCC reduces capacitor ripples, which prevents v_{ua} from exceeding the DC link voltage.

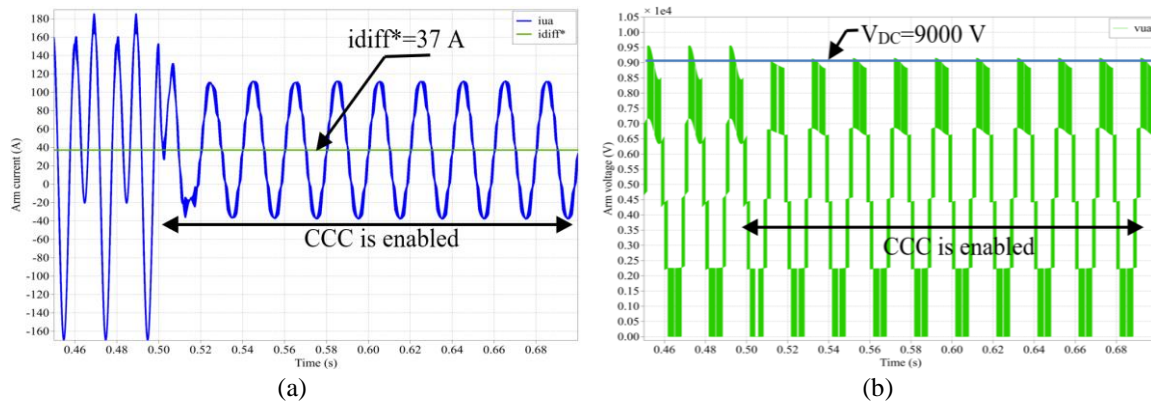


Figure 13. Arm waveforms of phase A (a) arm current i_{ua} and (b) arm voltage v_{ua}

4.4. Scenario 4: comparison between the Hagiwara method and the proposed method

The performance of the proposed method was evaluated through a simulation scenario and compared with the Hagiwara method [30], [31], using a carrier frequency of $f_c = 2,000$ Hz, with an interleaved angle applied, and circulating current enabled at $t = 0$ s. The control gains used in the Hagiwara simulation were obtained from [31]. This subsection provides a performance comparison between the proposed PR controller-based method and the Hagiwara method. Figure 14 displays the output current of phase A, demonstrating that the proposed method in Figure 14(a) has a lower current THD compared to the Hagiwara method shown in Figure 14(b). Furthermore, Figure 15 shows the output voltage v_a under both methods, with both methods generating nine levels. Interestingly, they exhibit similar THD values, as depicted in Figures 15(a) and 15(b).

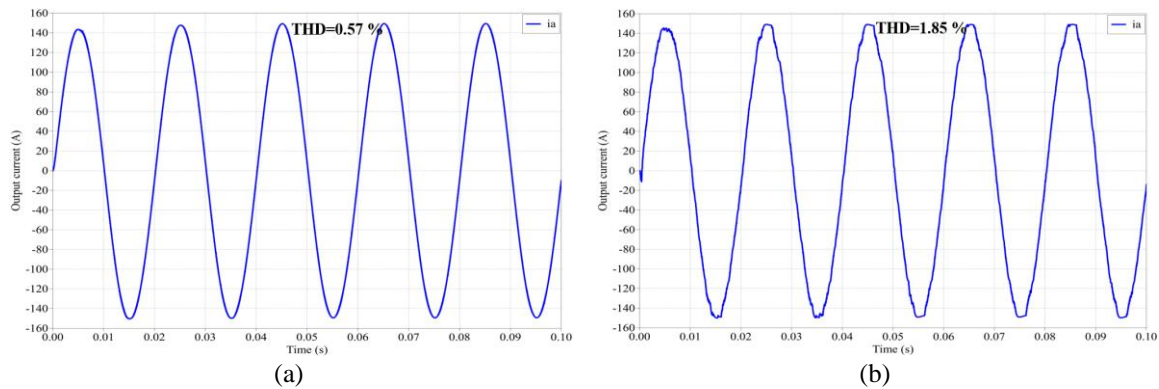


Figure 14. Output current i_a (a) proposed method and (b) Hagiwara method

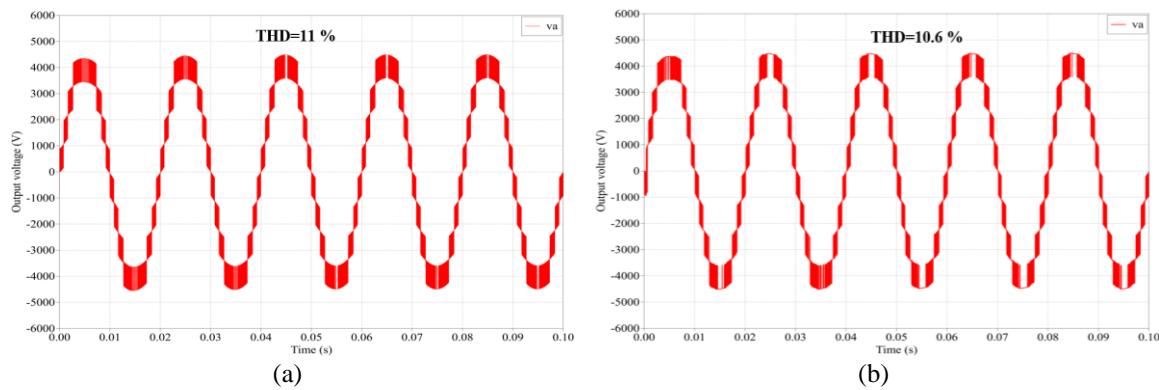


Figure 15. Output voltage v_a (a) proposed method and (b) Hagiwara method

Figure 16 displays the circulating current in phase A using both the proposed method and the Hagiwara method. The circulating current in Figure 16(a) exhibits low oscillation around its reference value $idiff^* = 37$ A, while in Figure 16(b), it shows high oscillation under the Hagiwara method. Figure 17 illustrates the harmonic spectra of the circulating current in phase A under both methods. The results in Figure 17(a) obtained using the proposed method, which employs a PR controller, demonstrate remarkable suppression capabilities for the second and fourth harmonics when compared to the Hagiwara method illustrated in Figure 17(b). It is evident that the presence of such harmonics in Figure 17(b) is the primary cause of the high oscillation in Figure 16(b).

Figure 18 shows the waveforms of the capacitor voltages for the upper arm of phase A. Using the proposed method, all capacitor voltages exhibit a perfect balance and have the same shape, as shown in Figure 18(a). This good consistency of the capacitor voltages is achieved naturally, without requiring any capacitor voltage balancing control. The peak-to-peak voltage ripple is approximately 81 V. In contrast, when the Hagiwara method is used, even with individual voltage balancing control, the capacitor voltages are more dispersed and have a lower consistency. The peak-to-peak voltage ripple is about 115 V, as shown in Figure 18(b).

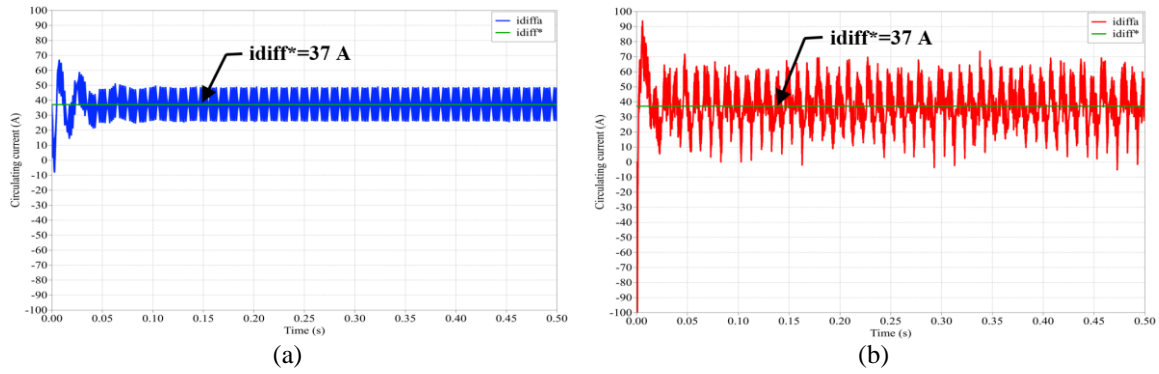


Figure 16. Circulating current i_{diffa} (a) proposed method and (b) Hagiwara method

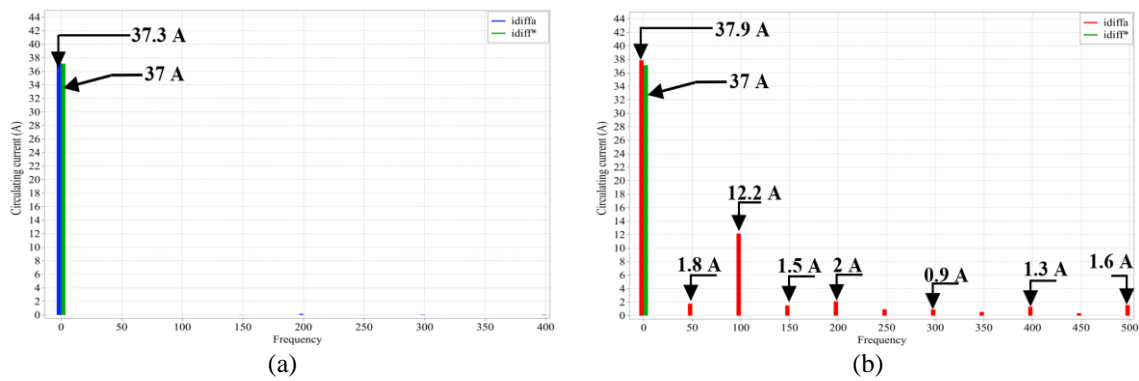


Figure 17. Harmonic spectra of circulating current i_{diffa} (a) proposed method and (b) Hagiwara method

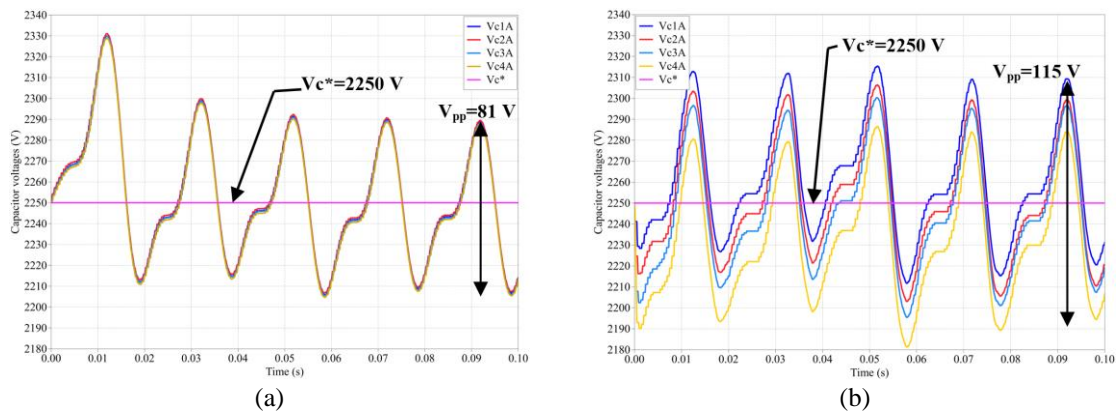


Figure 18. Capacitor voltages of the upper arm for phase A (a) proposed method and (b) Hagiwara method

5. CONCLUSION




This paper investigates the impact of PS-PWM modulation and circulating currents on the performance of MMC-based inverters. The proposed method achieves natural balancing of capacitor voltages only through a circulating current controller, using a high carrier frequency of PS-PWM modulation without additional control. Applying an interleave angle increases the output voltage levels to 2^{N+1} , thereby enhancing the quality of output waveforms. The circulating current controller is based on a PR controller and an MAF, effectively suppressing the second and fourth harmonic in the circulating current and minimizing capacitor voltage ripples. Comparing the proposed method to the widely used Hagiwara method for PS-PWM modulation reveals superior performance in terms of circulating current suppression and capacitor voltage balancing. Furthermore, the proposed method yields output waveforms with lower harmonics and THD.

REFERENCES




- [1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *2003 IEEE Bologna Power Tech Conference Proceedings*, 2003, vol. 3, pp. 272–277, doi: 10.1109/PTC.2003.1304403.
- [2] S. Du, A. Dekka, B. Wu, and N. Zargari, "Review of high-power converters," in *Modular Multilevel Converters: Analysis, Control, and Applications*, Hoboken, NJ, USA: John Wiley & Sons, Inc., 2018, pp. 3–36.
- [3] M. A. Perez, S. Ceballos, G. Konstantinou, J. Pou, and R. P. Aguilera, "Modular multilevel converters: recent achievements and challenges," *IEEE Open Journal of the Industrial Electronics Society*, vol. 2, pp. 224–239, 2021, doi: 10.1109/OJIES.2021.3060791.
- [4] F. Shahnazian *et al.*, "Control of MMC-based STATCOM as an effective interface between energy sources and the power grid," *Electronics*, vol. 8, no. 11, Nov. 2019, doi: 10.3390/electronics8111264.
- [5] J. Chen *et al.*, "An improved coordination method of multi-terminal MMC-HVDC system suitable for wind farm clusters integration," *International Journal of Electrical Power and Energy Systems*, vol. 117, May 2020, doi: 10.1016/j.ijepes.2019.105652.
- [6] M. Beza and M. Bongiorno, "Identification of resonance interactions in offshore-wind farms connected to the main grid by MMC-based HVDC system," *International Journal of Electrical Power and Energy Systems*, vol. 111, pp. 101–113, Oct. 2019, doi: 10.1016/j.ijepes.2019.04.004.
- [7] A. Dekka, B. Wu, R. L. Fuentes, M. Perez, and N. R. Zargari, "Evolution of topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 4, pp. 1631–1656, Dec. 2017, doi: 10.1109/JESTPE.2017.2742938.
- [8] A. I. Elsanabary, G. Konstantinou, S. Mekhilef, C. D. Townsend, M. Seyedmahmoudian, and A. Stojcevski, "Medium voltage large-scale grid-connected photovoltaic systems using cascaded H-bridge and modular multilevel converters: a review," *IEEE Access*, vol. 8, pp. 223686–223699, 2020, doi: 10.1109/ACCESS.2020.3044882.
- [9] Z. Ma *et al.*, "Multilayer SOH equalization scheme for MMC battery energy storage system," *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13514–13527, Dec. 2020, doi: 10.1109/TPEL.2020.2991879.
- [10] C. Gan, Q. Sun, J. Wu, W. Kong, C. Shi, and Y. Hu, "MMC-based SRM drives with decentralized battery energy storage system for hybrid electric vehicles," *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2608–2621, Mar. 2019, doi: 10.1109/TPEL.2018.2846622.
- [11] F. Rong, X. Gong, and S. Huang, "A novel grid-connected PV system based on MMC to get the maximum power under partial shading conditions," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4320–4333, Jun. 2017, doi: 10.1109/TPEL.2016.2594078.
- [12] S. Barcellona, M. Barresi, and L. Piegari, "MMC-based PV single-phase system with distributed MPPT," *Energies*, vol. 13, no. 15, Aug. 2020, doi: 10.3390/en13153964.
- [13] Xlinks, "Morocco-UK power project," *Xlinks*. <https://xlinks.co/morocco-uk-power-project/> (accessed: Nov. 28, 2022).
- [14] P. Tu, S. Yang, and P. Wang, "Reliability and cost based redundancy design for modular multilevel converter," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, 2018, doi: 10.1109/TIE.2018.2793263.
- [15] F. Zhao, G. Xiao, M. Liu, and D. Yang, "A fast sorting strategy based on a two-way merge sort for balancing the capacitor voltages in modular multilevel converters," *Journal of Power Electronics*, vol. 17, no. 2, pp. 346–357, 2017, doi: 10.6113/JPE.2017.17.2.346.
- [16] W. Luo, Y. Ma, and C. Zheng, "Selection-based capacitor voltage balancing control for modular multilevel converters," *Journal of Power Electronics*, vol. 21, no. 10, pp. 1427–1438, Oct. 2021, doi: 10.1007/s43236-021-00288-8.
- [17] R. Darus, J. Pou, G. Konstantinou, S. Ceballos, and V. G. Agelidis, "Controllers for eliminating the AC components in the circulating current of modular multilevel converters," *IET Power Electronics*, vol. 9, no. 1, pp. 1–8, Jan. 2016, doi: 10.1049/iet-pel.2014.0930.
- [18] Y. Li, E. A. Jones, and F. Wang, "Circulating current suppressing control's impact on arm inductance selection for modular multilevel converter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 182–188, Mar. 2017, doi: 10.1109/JESTPE.2016.2617865.
- [19] X. Shi, S. Filizadeh, and L. Wang, "Analysis of submodule capacitor voltage ripple and second-harmonic current in MMCs," in *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2019, pp. 1–8, doi: 10.1109/COMPEL.2019.8769665.
- [20] B. Bahrani, S. Debnath, and M. Saeedifard, "Circulating current suppression of the modular multilevel converter in a double-frequency rotating reference frame," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 783–792, Jan. 2016, doi: 10.1109/TPEL.2015.2405062.
- [21] S. Isik, M. Alharbi, and S. Bhattacharya, "An optimized circulating current control method based on PR and PI controller for MMC applications," *IEEE Transactions on Industry Applications*, vol. 57, no. 5, pp. 5074–5085, 2021, doi: 10.1109/TIA.2021.3092298.
- [22] L. Ben-Brahim, A. Gastli, M. Trabelsi, K. A. Ghazi, M. Houchati, and H. Abu-Rub, "Modular multilevel converter circulating current reduction using model predictive control," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 6, pp. 3857–3866, Jun. 2016, doi: 10.1109/TIE.2016.2519320.
- [23] F. Martinez-Rodrigo, D. Ramirez, A. Rey-Boue, S. de Pablo, and L. Herrero-de Lucas, "Modular multilevel converters: control and applications," *Energies*, vol. 10, no. 11, Oct. 2017, doi: 10.3390/en10111709.
- [24] Y. Tian, H. R. Wickramasinghe, Z. Li, J. Pou, and G. Konstantinou, "Review, classification and loss comparison of modular multilevel converter submodules for HVDC applications," *Energies*, vol. 15, no. 6, Mar. 2022, doi: 10.3390/en15061985.
- [25] Y. Wang, A. Aksoz, T. Geury, S. B. Ozturk, O. C. Kivanc, and O. Hegazy, "A review of modular multilevel converters for stationary applications," *Applied Sciences*, vol. 10, no. 21, Oct. 2020, doi: 10.3390/app10217719.
- [26] F. Deng and Z. Chen, "Elimination of DC-link current ripple for modular multilevel converters with capacitor voltage-balancing pulse-shifted carrier PWM," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 284–296, Jan. 2015, doi: 10.1109/TPEL.2014.2322913.
- [27] W. van der Merwe, P. Hokayem, and L. Stepanova, "Analysis of the 5-cell single phase MMC natural balancing mechanism," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2014, pp. 3416–3423, doi: 10.1109/ECCE.2014.6953864.
- [28] K. Ilves, L. Harnefors, S. Norrga, and H.-P. Nee, "Analysis and operation of modular multilevel converters with phase-shifted carrier PWM," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 268–283, Jan. 2015, doi: 10.1109/TPEL.2014.2321049.
- [29] W. Uddin, T. D. C. Busarello, K. Zeb, M. A. Khan, A. K. Yedluri, and H.-J. Kim, "Control strategy based on arm-level control for output and circulating current of MMC in stationary reference frame," *Energies*, vol. 14, no. 14, Jul. 2021, doi: 10.3390/en14144160.
- [30] M. Hagiwara, R. Maeda, and H. Akagi, "Control and analysis of the modular multilevel cascade converter based on double-star chopper-cells (MMCC-DSCC)," *IEEE Transactions on Power Electronics*, vol. 26, no. 6, pp. 1649–1658, Jun. 2011, doi: 10.1109/TPEL.2010.2089065.
- [31] M. Hagiwara and H. Akagi, "Control and experiment of pulse width-modulated modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009, doi: 10.1109/TPEL.2009.2014236.

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