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An efficient reconfigurable code rate cooperative low-density parity check codes for gigabits wide code encoder/decoder operations

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ABSTRACT

In recent days, extensive digital communication process has been performed. Due to this phenomenon, a proper maintenance of authentication, communication without any overhead such as signal attenuation code rate fluctuations during digital communication process can be minimized and optimized by adopting parallel encoder and decoder operations. To overcome the above-mentioned drawbacks by using proposed reconfigurable code rate cooperative (RCRC) and low-density parity check (LDPC) method. The proposed RCRC-LDPC is capable to operate over gigabits/sec data and it effectively performs linear encoding, dual diagonal form, widens the range of code rate and optimal degree distribution of LDPC mother code. The proposed method optimize the transmission rate and it is capable to operate on 0.98 code rate. It is the highest upper bounded code rate as compared to the existing methods. The proposed method optimizes the transmission rate and is capable to operate on a 0.98 code rate. It is the highest upper bounded code rate as compared to the existing methods. the proposed method's implementation has been carried out using MATLAB and as per the simulation result, the proposed method is capable of reaching a throughput efficiency greater than 8.2 (1.9) gigabits per second with a clock frequency of 160 MHz.

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1. INTRODUCTION

A challenge of designing rate-compatible low-density parity check (RC LDPC) codes, which need to improve size of rate of code, because to widen the overall channel size and to give a good and proper service depending on channel conditions. Among many paths, puncturing method gives an advantageous approach to gain a list of RC codes, where maximum daughter codes rate can be obtained from mother codes, following a method of puncturing, i.e., puncturing some parity bits [1]–[5]. code designs major challenge with specified way to maintain the performance of both codes are nearer to potential. Piercing leads to modification of degree distribution, is a main element for finding the decoding act, it is complex to get the best daughter codes at highest code levels.

A group of RC LDPC codes is recommended by document with different code levels. By asserting a perfect transmission pattern with a zero-filling encryption algorithm, the method to get RC codes does not change daughter codes degree of distribution. Thus, the method forces rates to a 0.98.

Designed from shifted identity matrices, the codes match the implementation of high-speed parallel encoders and decoders. The deployment results to a design of field programmable gate array (FPGA) devices, which show that a 32-parallel encoder for the said LDPC codes having rates from 0.5 to 0.98 is having a capacity to reach an outturn of 8.2 (1.9) gigabits per second (Gbps) with the help of a clock frequency of 180 MHz and absorbing only 0.3% (12%) of Xilinx Virtex-5's overall resources. Rate-compatible LDPC codes system is as shown in Figure 1. The information 'm' bits are applied to the RC-LDPC and the output of RC-LDPC generates a codeword 'C', which is then applied to modulation process. the modulated output is applied to the channel.

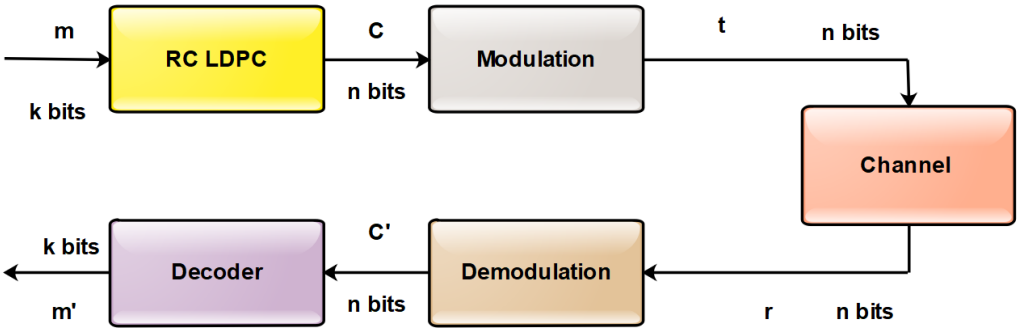

Figure 1. The fundamental block diagram of RC-LDPC codes

2. METHOD

2.1. Build rate compatible LDPC codes

RC LDPC codes have been considered using a subsequent parent matrix, which is having a set of i X (I+J) sub-matrices as shown in (1).

$$M = \begin{bmatrix} m_{1,1} & . & . & m_{1,j} & K & . & . \\ m_{1,1} & . & . & m_{2,j} & K & K & . \\ . & . & . & . & . & . & . \\ .m_{i-1,1} & . & . & m_{i-1,j} & K & K & K \\ m_i & . & . & m_{i,j} & . & K & K \end{bmatrix} \quad (1)$$

where 'K' is represented the it is an $a\ X\ a$ identity matrix and the null matrices are indicated by unmarked spaces. For $1 \leq i \leq I$ and $1 \leq j \leq J$ the submatrix $m_{i,j}$ within 'M' at position (i,j) is either a shifted identity matrix [6], [7]. The shifted identity matrix is gained by performing a circularly shifting the rows of 'K' to the right by $S_{i,j}$ positions i.e., $m_{i,j} = K(S_{i,j})$. $S_{i,j}$ shows shifting coefficient, and has been selected from the restricted set-in range 0 and 'a'. The main purpose is to prevent short and medium length cycles depending on the methods in [6], [7]. The submatrix size is represented by 'a'. To differentiate among conventional rows and columns, we access column of submatrices, which is present like a block column inside M. It has I block-rows and $(J + I)$ block columns inside the matrix (1) [8], [9].

2.2. Transmission and encoding algorithm

Assume splitting of a codeword 'X' into (J+K) parts, as shown in (2).

$$X = [p_1, p_2, p_3, \ldots\ldots\ldots p_j, q_1, q_2, q_3, \ldots\ldots q_i\ ] \quad (2)$$

where p_j is presented partitioning codewords with $1 \leq j \leq J$ shows systematic bits of 'a' vector and 'q' with $1 \leq i \leq J$, that is a vector of q parity bits. With coding basics, MX^T=0^T, results to a parity bit as (3) and (4):

$$Q_1^T = \sum_{j=1}^{J} m_{1,k} P_k^T \quad (3)$$

$$Q_i^T = \sum_{k=1}^{K} m_{i,j} P_k^T + Q_{i-1}^T \quad (4)$$

with $2 \leq i \leq I$,. it is agreed that the introduction of LDPC codes is linear time encoded. The code presented in (1) possess leas rate R_L is given in (5).

$$R_L = J/(J + I) \tag{5}$$

The daughter code having highest rate, R_H as shown in (6) is resulted by passing only one parity bit vector q_I.

$$R_H = J/(J + 1) \tag{6}$$

For *ARQ* which is called as automatic repeat request transmission, step-by-step transmission of systematic and parity bits are as follows:

- transmit parity bit vector q_i and systematic bit vector p.
- transfer parity bit vectors $[q_1, q_2, \ldots\ldots\ldots q_{i-1}]$ according to the following order, if asked.

$q_{\frac{j}{2}}$;
$q_{j/4}$, $q_{3j/4}$;
$q_2, q_4, q_6 \ldots\ldots\ldots\ldots (the\ rest\ even\ numbers)$
$q_1, q_3, q_5 \ldots\ldots\ldots\ldots (the\ rest\ ODD\ numbers)$

2.3. Case study

For instance, assume a 32×48 array of sub-matrices, which is considered as a mother matrix, across the entire text [10], [11]. It is simple to extend the suggested approach to LDPC codes having any numbers of block-rows and block-columns. Solid bars in a Figure 2 shows an offset ID matrix with unmarked spaces shows null matrices. A least code rate of $R_L = 0.5$ is associated with mother code.

$\boldsymbol{M} =$

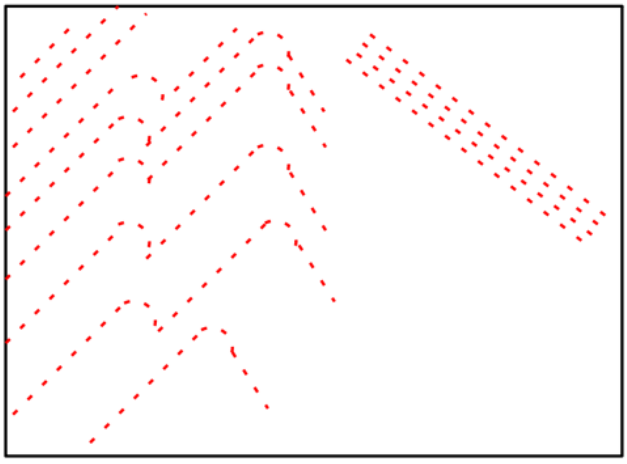

Figure 2. 32×48 sub matrix array constitutes a LDPC mother matrix. Shifted identity matrix forms solid bars and null matrices found unmarked spaces

We assume splitting a codeword *x* to smaller parts, say 64, is given in (7)

$$X = [p_1, p_2, p_3, \ldots\ldots\ldots p_{32}, q_1, q_2, q_3, \ldots\ldots q_{32}\ ] \tag{7}$$

where, p_j with $1 \leq j \leq 32$ indicates a vector of 'a' systematic bits and q_i with $1 \leq i \leq 32$ is a vector of 'a' parity bits. A systematic bit vector 'p' is initially transmitted by the transmitter along with the parity bit vector q_{32}.

It is discovered that; daughter code has the maximum rate $R_M = 0.98$. Send the other parity bit vectors in the following order if requested: $q_{12}, q_6, q_{18}, q_2, q_4, q_8, q_{10}, q_{14}, q_{16}, q_{20}, q_{22}, q_1, q_3, q_5, q_7, q_9, q_{11}, q_{13}, q_{15}, q_{17}, q_{19}, q_{21}, q_{23}$. We shall discuss the benefits of transmitting the parity bit vectors p_{32} first, in section 4.

2.4. Comparative analysis of rate-compatible code and rate-adaptive code

Rate-adaptive LDPC codes are created in [12]–[14] which are indicated with the help of mother matrix, and it also includes an array of circularly shifted identity sub-matrices. By deleting the highest rows from the mother matrix, the parity-check matrices of daughter codes with higher levels are obtained i.e., by row-deleting approach, the rates are adapted. By piercing few of the parity bits of the mother code, the daughter codes of rate-compatible LDPC codes are obtained. By deleting few columns from the parity portion of the mother matrix, the greater rates of parity-check matrices of daughter codes are generated. Table 1 show the performance analysis between reconfigurable code rate cooperative (RCRC) and rate-adaptive LDPC codes.

Table 1. Performance analysis between RCRC and rate-adaptive LDPC codes

Particulars	Rate adaptive LDPC code	RCRC
System parity check bits matrix for code length applications	This method is constant in various row removal adaptive modulation and coding algorithm	This method is constant in various column removal adaptive modulation and coding algorithm

3. IMPLEMENTATION PROCESS OF UNIVERSAL ENCODER:

The fact is that usage of single encoder/decoder pair, decoding and encoding of RC LDPC codes can be done and is one of its key benefits [15]. In this section, we walk through how the universal encoder is implemented in practice. Think about the following code having 'I' as 24 and 'j' as 24 in II.B). Due to the fact that $m_{i,j}$ is either a null matrix or a shifted identity matrix, the matrix vector multiplications in (3) and (4) is computed as (8):

$$X_{i,j}^{T} = m_{i,j} p_j^{T} \tag{8}$$

where $X_{i,j}^{T}$ with $1 \leq i \leq 32$ and $1 \leq j \leq 32$ indicates a vector of 'a' bits. $m_{i,j}$ indicates shifted identity matrix i.e., $m_{i,j} = k\ (S_{i,j})$. By shifting p_j to the left side by $S_{i,j}$ places, $X_{i,j}$ is obtained. $m_{i,j}$ is a null matrix and $X_{i,j}$ is a zero vector. Using a simple XOR processor, the computation in (3) and (4) can be implemented [16], [17].

$$q_i(k) = \sum_{j=1}^{24} x_{i,j}(k) + s_{i-1}(k) \tag{9}$$

where $q_0(k) = 0, 1 \leq i \leq 24$ and $1 \leq j \leq a$. The $k - bits$ in the bit vector $x_{i,j}$ is represented by every signal to the input $x_{i,j}(k)$. To shorten the time, it takes for signals to propagate from input to output, a tree design is used. A made up of 32 XOR processors are used to design a 32-parallel encoder and integrated into MATLAB and FPGA devices. The target XC5VFX200T device's created implementation was placed and routed using the Xilinx development system tool suite (ISE 10.1) with the speed option set to -2. Estimation of highest clock frequency was carried out using Xilinx static time analysis. The results give the following observation: 80 LUTs, slices of 416 with 467 flip-flops were used by 32 parallel encoders. Thus, the total resources consumed by encoder were only 3/10 percentage in an XC5VFX200T device [18], [19].

Static timing analysis is a critical process in digital design, particularly in the context of field-programmable gate arrays (FPGAs) like those manufactured by Xilinx. It involves analyzing the timing behavior of a digital circuit to ensure that it meets the required timing constraints, such as setup and hold times, and that it operates correctly within its intended clock frequency. Analysis of the Xilinx static timing shows that, in an XC5VFX200T device the highest encoding clock frequency of 32 parallel encoder attained is 460 MHz. An encoding speed of 7,200 Mbps was attained by the encoder with the use of 180 MHz frequency for the encoding clock.

4. DECODING ALGORITHM AND PERFORMANCE ANALYSIS

Here we are using Sum product algorithm to decode the implemented RC LDPC codes effectively. Sum and product of external communication in every column and each row is performed by this algorithm [19], [20]. Rather than using different series column processing in classical sum product method here we are using junction sum product sort out method. This decoding algorithm includes the computation of external communication in column processing into series processing. That is, we are using a processor called junction series column processor to operate each series from bottom series to top series in every loop.

4.1. Zero filling decoding algorithm

Before introducing the null-filling method for decoding the implemented RC codes. We shall talk over about the mother code. Assume the mother matrix as 'M' consisting of $i\ X\ a$ series and $(j+i)\ X\ a$ columns, in which $(j+i)$ and I are block columns and series. Hence this code is sort out with the junction processor from bottom series to top series inside the matrix M in every loop [21], [22]. When sort out is processing the series column processor captures the pair extrinsic messages y_{mn} from matrix and log likelihood ratio (LLR) (Z_n) from matrix after then it calculates the new ratio Z'_n and extrinsic communication y'_{mn} with $1 \leq m \leq i\ X\ a$ and $1 \leq n \leq (J+i)Xa$. The extracted n-bits LLR at received signal is given by (10).

$$Z_n = \log(s_n^0/s_n^1) \tag{10}$$

where s_n^0 and s_n^1 is described as nth bit probabilities of '0' or '1' respectively. The mother code with the least speed: systematic segment and parity segment are sent, where Log Likelihood ratio of all the segments can be captured out of the signal collected [23]–[25]. For daughter code: few parity segments are not sent, where Nth segment is large positive constant which is not sent and assigned to Z_n with value 0.

5. PERFORMANCE ANALYSIS

Implemented RCRC-LDPC code has to evolved for its performance. Hence the simulations are performed along with the binary phase-shift keying modulation in additive white gaussian noise channel for representing RC codes by Mother code matrices which is as shown in Figure 2 where $a = 72$. This method will finish if the correct code is originated else when it reaches 50 loops in the cycle. The proposed RCRC-LDPC has an advantage when it pushes upper rates (R) to 0.98 by transmitting a single parity bit vector (P24). The q_{32} code performs well so it is sent to loop. The frame error rate at 60th loop vs signal to noise ratio is given in Figure 2 which has $length = 1900$ and $Rate = 0.98$. The query is that why we are sending the segment vector q_{32}. The contrast occurred for frame error rate (FER) at 60th loop with the signal-to-noise ratio (SNR) per bit $\frac{E_b}{N_0}$ as shown in Figure 3 for those source code with the distance 1,900 and a speed of 0.98. This clearly says the source code with the segment vector q_{32} gives top and best result. We are rewriting the (3) and (4) by sending a vector S_i to describe why transferral plan attains the good performance which is given (11).

$$s_i^T = \sum_{k=1}^{i}\left(\sum_{j=1}^{J} m_{i,j}\, p_j^T\right) \tag{11}$$

with $1 \leq i \leq J$. It is shown in (11) here the vector s_i is encoding with the matrix m_i, here m_i, indicates the top a block series in structured portion of M. Dispatching s_i with $i < I$, since the level sharing in M a is dissimilar from ideal sharing in M, degradation of decoding result takes place. If we send vector s_i, the ideal level sharing keeps no change and the best performance is attained by transmission scheme.

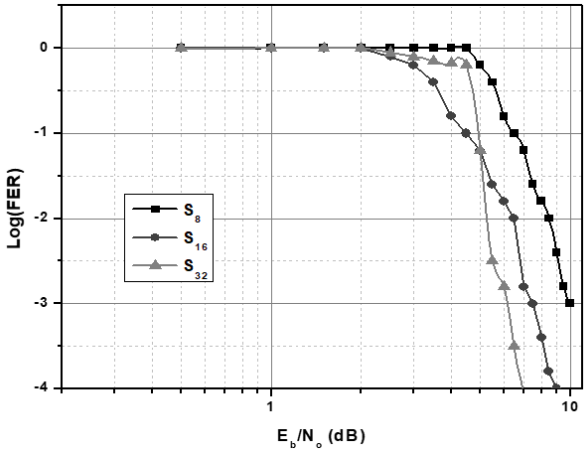

Figure 3. 60th code iteration with a range of 1900 and 0.98 code rate with respect to the transmission parity bit vector

In Figure 4 it is shown that the FER at the 60th loop versus E_b/N_0 for 8 speeds, i.e., R=0.99, 0.97, 0.93, 0.89, 0.86, 0.78, 0.68, and 0.52. In the codes, there is a stable number of well-ordered bits, 1896. In order to standard the implemented RC LDPC codes, the contrast existing with the LDPC codes for the code of range 2,562 and speed 0.52, 0.68, 0.78 and 0.86 are mentioned in the IEEE 802.16e standard, also known as WiMax codes. Figure 5 shows the performance analysis between RCRC LDPC and WiMax with respect to eight different code rates.

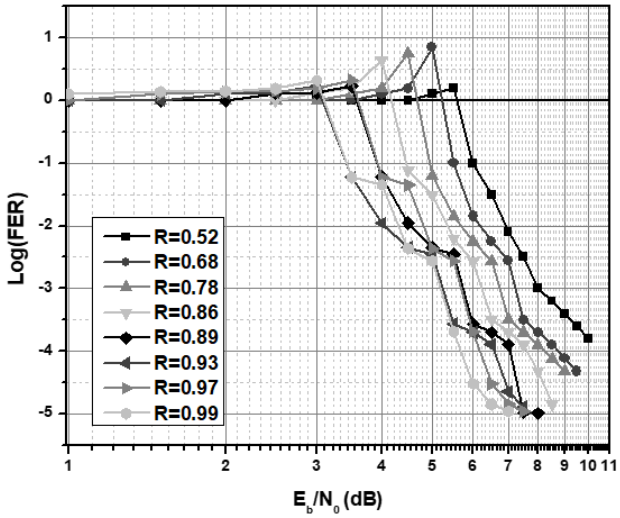

Figure 4. the performance analysis of FER at the 60th code iterations of the LDPC codes with respect to the eight different code rates using the proposed RCRC-LDPC

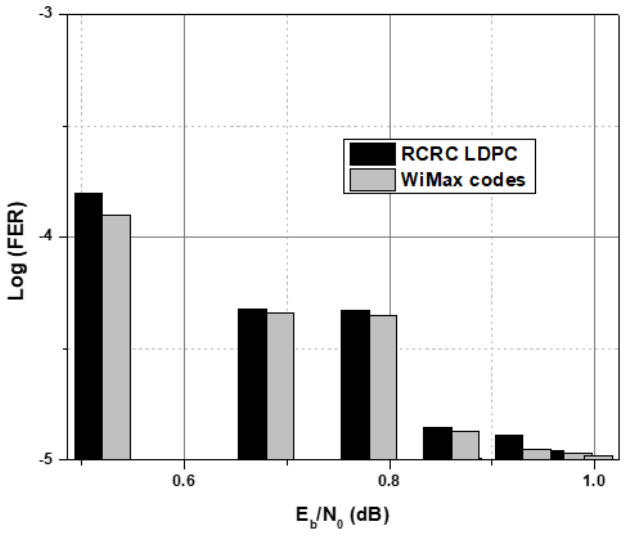

Figure 5. the performance analysis between RCRC LDPC and WiMax with respect to eight different code rates

6. IMPEMENTATION OF UNIVERSAL DECODER

Here we are implementing a 36 analogous decoder into action. For RC codes with a =72 It contains 36 junction series-column processors to calculate the hardware asserts utilization and decoding speed of a decoder. It is shown in the Figure 2 that mother matrices have a top 8 series level, that is maximum eight '1' sin the mother matrix at each row. In the Figure 3 it is shown that the junction series-column processors have a level of 8. We have "s-to-u" (u-to-s) box labelled indicates is a converter. Here The converter is converting input wave from(to) a wave number to(from) a positive number.

The Figure 6 that there is a processor which consists of both inputs and outputs, eight in number. The processor is designed using fifteen XOR gates and its carryout sign functioning as given in (12) and (13).

$$P = \prod_{i=1}^{8} sign\ (x_j) \tag{12}$$

$$P_i = P\ X\ sign\ (x_j) \tag{13}$$

with $1 \leq i \leq 8$. The magnitude operation is performed by the processor known as magnitude processor which has 8 inputs and 8 outputs in Figure 6.

$$y_j = \emptyset\left[\sum_{i=1, i\neq k}^{8} |x_i|\right] \tag{14}$$

where y_j is represented the magnitude operation, $\emptyset$ is describe the 7-bit look-up-table (LUT) function using 4 bits for fractional part. The measurement for the considered case code's submatrices is 72, the 36 analogous decoder is implemented with a MATLAB-XC5VFX200T FPGA tool with the rate of -2, it intakes below expedient: chop 8%, flipflop 12%, and look up table 12%. Timing analysis publishes above results, for 36 parallel decoder the maximum decoding clock frequency attained is 250 MHz with 180 MHz as decoding clock frequency and iteration number of 6 decoder is capable of attaining a decoding rate of 1.9 Gbps.

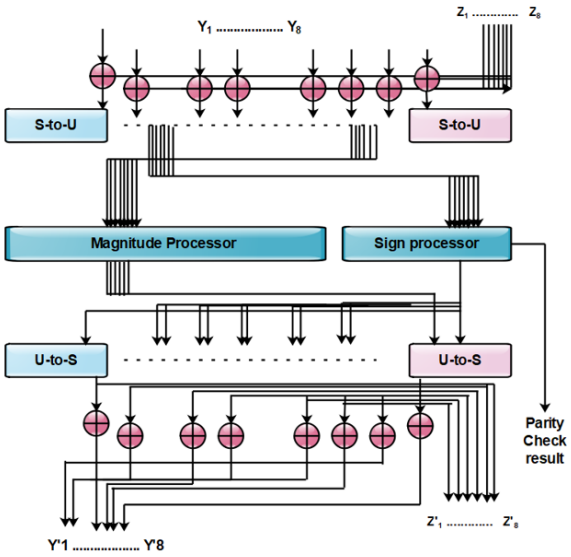

Figure 6. RCRC LDPC row-column processor with respect to the eight degrees

7. CONCLUSION

The proposed method RCRC LDPC code enhances the code rates and it is capable to optimize the transmission rate. The proposed method efficiently distributes the unchanged degree codes used for the more communication operation to increase the switching operation. Due to these activities, the mother code and all daughter codes very desired result. The proposed method optimizes the transmission rate and is capable to operate on a 0.98 code rate. It is the highest upper bounded code rate as compared to the existing methods. The proposed method enhances parallel operations of 32 encoders and 44 decoders with a throughput rate of 8.2 with 1.9 Gbps by using a clock frequency of 180 MHz and power consumption is reduced by 0.54% as compared to the existing methods and FER is reduced to 0.12% and signal to noise ratio increases to 1.2% as compared to the existing method (WiMAX). Due to this, the proposed method is capable to operate high bit rate data without any overheads, and millions of electric components are integrated efficiently with more accelerated performance.

FUTURE SCOPE

Nowadays, 5G LTE communication is an emerging field. Due to more devices being connected to the 5G LTE network, this research work will be enhanced to 128-bit operational and increases the switching speed.

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