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# A thermally aware performance analysis of quantum cellular automata logic gates

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**ABSTRACT**

The high-performance digital circuits can be constructed at high operating frequency, reduced power dissipation, portability, and large density. Using conventional complementary-metal-oxide-semiconductor (CMOS) design process, it is quite difficult to achieve ultra-high-speed circuits due to scaling problems. Recently quantum dot cellular automata (QCA) are prosed to develop logic circuits at atomic level. In this paper, we analyzed the performance of QCA circuits under different temperature effects and observed that polarization of the cells is highly sensitive to temperature. In case of the 3-input majority gate the cell polarization drops to 50% with an increase in the temperature of 18 K and for 5 input majority gate the cell polarization drops more quickly than the 3-input majority. Further, the performance of majority gates also compared in terms of area and power dissipation. It has been noticed that the proposed logic gates can also be used for developing simple and complex and memory circuits.

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## 1. INTRODUCTION

Emerging nano-technology such as carbon nanotubes [1], quantum dot cellular automata (QCA) [2], [3], nano magnetic logic, resonating tunnelling diodes, and spin-wave devices are designed to support the Moore's law trend in integrated circuits. A promising alternative is QCA technology. The advantages of QCA technology computing paradigm over complementary-metal-oxide-semiconductor (CMOS) technology, including degraded power, large density and fast operation in the terahertz frequencies. Due to the fact that QCA is distinct over existing technologies, it is evident that innovative and different design approaches are required to create the circuits.

The quantum dot cells are used to design the logic gates and also used for the signal transmission. The signal information is not represented by conventional voltage or current measurement; in fact, it is represented by the polarization of the quantum dot cell. Since the voltages and currents are not involved in the characterization of the output signal the QCA power designs are very minimal. The power analysis of QCA circuits has been reported in several papers [4], [5].

In the current literature, there are many papers available on design of the QCA circuits. In [6], [7], presented the XOR/XNOR gate circuits for QCA circuits modular design with 13 cells and also designed the full adder, parity circuit and comparator circuit. Later in, a modified XOR gate with a single layered structure using only 9 cells is explained. Therefore, the presented XOR gates occupies lesser area and lower latency.

The authors also designed full-adder, parity checker and binary to gray code converter using the modified XOR gate. It has been observed that 24% improvement in cost and 35.5% less power dissipation than the previously reported designs. In QCA circuits it values noting that the cell polarization is more sensitive to temperature variations and none of the previous studies addressed with issue. In this paper, we performed the temperature sensitive analysis of QCA circuits; especially analyzed the majority gates, which are the primary gates for the design in QCA technology. The cell polarization is highly sensitive to temperature. Therefore, we further performed the temperature sensitive analysis of the 3-inputs and 5-inputs majority gates.

## 2. QCA CIRCUITS

### 2.1. QCA basics

There are 4-quantum-dots stacked in a square arrangement to create a typical QCA cell. The polarization of stable state is determined by all parameters involved in electron charge, as shown in Table 1, two electrons can occupy these quantum dots based on the tunnelling process. At each of the four corners of a square QCA, 4-quantum-dots are situated [8], [9]. Six-dot and eight-dot QCA cell implementation is still a relatively new field of study [10], [11]. The cell polarization $P = +1$ represents "1" and $P = -1$ shows "0" [12], [13]. The polarization value can be determined by the electrostatic energy among cells *i* and *j*, this also be called as Kink energy can be calculated as (1) [14].

$$E_{i,j}^{m,n} = \frac{1}{4\pi\varepsilon_0\varepsilon_r}\sum_{m=1}^{4}\sum_{n=1}^{4}\frac{q_i^m - q_j^n}{\left|d_i^m - d_j^n\right|} \quad (1)$$

The Kink energy among the two cells can be calculated as (2).

$$E_{i,j}^{kink} = E_{i,j}^{opposite\ polarization} - E_{i,j}^{same\ polarization} \quad (2)$$

The parameter representation is presented in Table 1. For the opposite polarization the polarization values of $P_i$ and $P_j$ are considered to be not equal and for equal polarization are values are considered to be equal. The cell polarization of each can be calculated as (3),

$$E_{i,j} = \left(\frac{E_{i,j}^{kink}}{2\gamma}\sum_j P_j\right) \Big/ \sqrt{1 + \left(\frac{E_{i,j}^{kink}}{2\gamma}\sum_j P_j\right)^2} \quad (3)$$

where γ is the electron tunnelling energy inside the QCA cell.

Table 1. Parameter representation

| No. | Parameter symbol | Representation |
|---|---|---|
| 1 | $\varepsilon_0$ | free space permittivity |
| 2 | $\varepsilon_r$ | material permittivity |
| 3 | $q_i^m$ | charge of electron on $m^{th}$ dot in $i^{th}$ cell |
| 4 | $q_j^n$ | charge of electron on $n^{th}$ dot in $j^{th}$ cell |
| 5 | $\lvert d_i^m - d_i^n \rvert$ | gap among the $m^{th}$ dot in $i^{th}$ cell and $n^{th}$ dot in $j^{th}$ cell |

The QCA circuits require the clock signal for data synchronization and also it regulates the information flow and supplies the circuit power. There are four different clock zones are available in QCA each has the phase shift of 90°3 [15]–[17]. There are four different phases like switch, hold, release and relax in each clock. During switch phase, cells become polarized and they are ready to switch based on the kink energy. The inner dot barrier rises throughout in switch. The barriers have to keep high during the hold phase to ensure that the polarization current of the cell can be maintained [18], [19]. During the release, the inner dot barrier decreases and loose polarization [20], then it becomes non-polarized during the release phase and this situation continues during the relax phase.

### 2.2. Fundamental components of QCA circuits: wire and inverter

The design elements such as wire and inverter are presented in this section. The primary components of QCA circuits are wire, inverter, majority and minority gates. The QCA wire illustrated in Figure 1, made of aligning QCA cells in a cascading manner. The signal flows from one to another side based on Coulomb's interaction between the electrons [21]–[23].

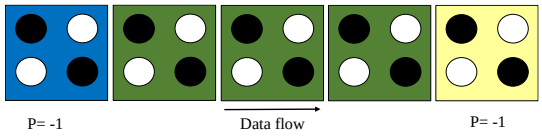



Figure 1. The interconnect wire structure of QCA Inverter

The inverter operation easily achieved by arranging the QCA cell in corner with the other cell. The inverter cell can be designed in two ways by using two and three-layer structures. The Figure 2 shows QCA inverters in two different types, whereas in Figure 2(a) the two layers are displaced by the length of the cell. It can be observed that the output cell becomes the logic 1 polarity in so far as the input driven by logic 0 [24], [25]. However, the inverter circuit is a not robust in nature and suffers with signal integrity issues due to the weak Coulomb interaction forces. This problem can be rectified by using a three-layered structure as represented in Figure 2(b).

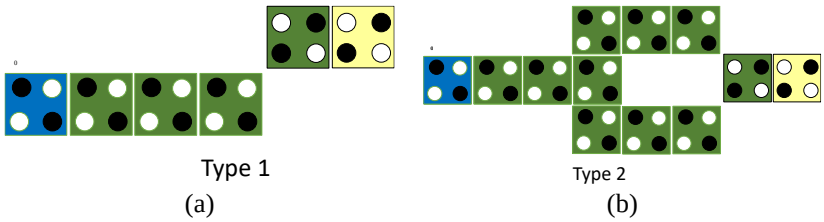



Figure 2 QCA inverter (a) type-1 and (b) type-2

### 2.3. QCA logic circuit implementation using majority and minority gates

In QCA the logic circuits are implemented by the majority gates and minority gates. The AND and OR gates are designed with majority, NAND and NOR are implemented using the minority gate. The majority gate brings out the output value based on the input majority bit pattern [26]. The majority gate Boolean expression of can be represented as (4).

$$Maj\ (A, B, C) = AB+BC+AC \tag{4}$$

For designing the 2-input basic gates, the 3-input majority is required [27]. The circuit of 3-input majority is represented in Figure 3. The majority gate can also act as a 2-input AND/OR by fixing the appropriate polarization to one of the QCA cell. The (5) and (6) demonstrate the conversion of the majority gate to AND/OR operations by forcing 1-input to logic "0" or "1" and the operation of 5-input majority is stated in the (7) [28], [29].

$$M\ (A, B, 0) = F = A.B \tag{5}$$

$$M\ (A, B, 1) = F = B.1 + 1.A + A.B = A.B + A + B = B + A\ (1 + B) = A + B \tag{6}$$

$$M\ (A, B, C, D, E) = (ABC + ABE + ABD + ACD + ADE + ACE + BCE + BDE + BCD + CDE) \tag{7}$$

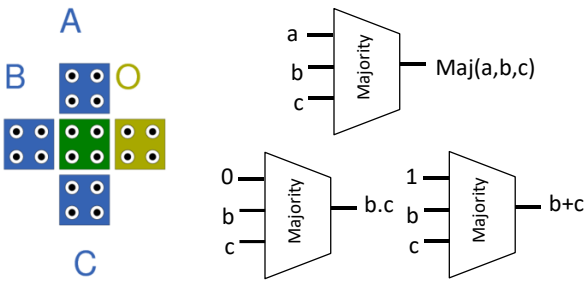



Figure 3. Design of three-input majority gate

Design of the three different 5-input majority gates is depicted in Figure 4. Type-1 majority is placed in Figure 4(a) where connection to output is provided in same layer. However, type -1 majority gate suffers with input cell-cell cross-talk since the cells are very close to each other. Type-2 majority gate in Figure 4(b), where inputs cells accept all five signal inputs in the same direction at the first clock. In type-3 in Figure 4(c) majority gate has ten cells, the connection to output is provided in multi-layer because the output cell is enclosed by input cells, this gate also suffers with cell-cell cross talk, since all cells are closely arranged.

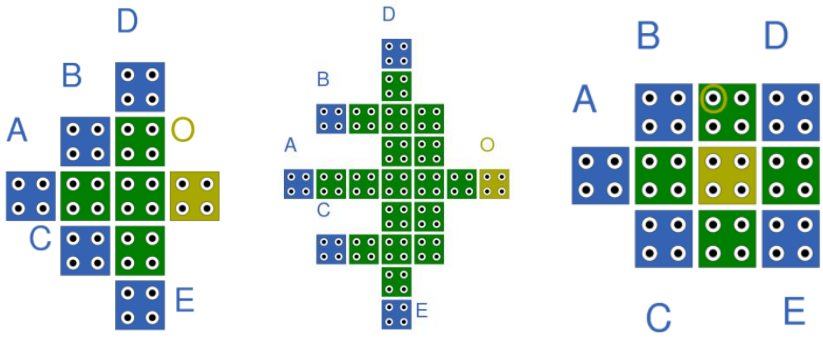



Figure 4. Different design techniques for five-input majority gate (a) type-1, (b) type-2 and (c) type-3

The minority gate generates the output value 0, if there are minority number of 0's in the input pattern. For example, the 3-input minority gate produces "0" if the input is (0,1,1). The design of 5-input minority gate and the conversion to NAND and NOR are represented in Figure 5. For the 5-input minority gate shown in Figure 5(a) the Boolean expression as (8).

$$\text{Min}\,(A,B,C,D,E) = \overline{(ABC + ACD + ACE + ADE + ABD + ABE + BCD + CDE + BCE + BDE)} \quad (8)$$

It can be observed that the minority gate produces output 1 when there is minority of "1" s in the input pattern, otherwise the circuit produces output 0. Similar to the majority gate, the minority functionality can be changed to NAND, NOR gates by changing the input cells polarization. The following equations demonstrate the conversion of the minority gate to NAND/NOR operations by forcing one of the inputs to logic "0" or "1". The QCA circuits for the implementation of three-input NAND, NOR are represented in Figures 5(b) and 5(c), respectively. Three-input NAND, NOR gates can be expressed as (9) and (10).

$$\text{Min}\,(A,B,C,0,0) = \overline{(ABC)} \quad (9)$$

$$\text{Min}\,(A,B,C,1,1) = \overline{(A+B+C)} \quad (10)$$

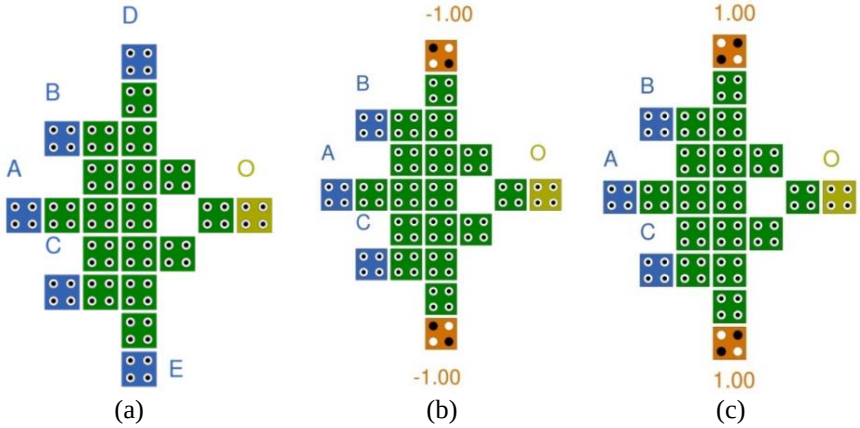
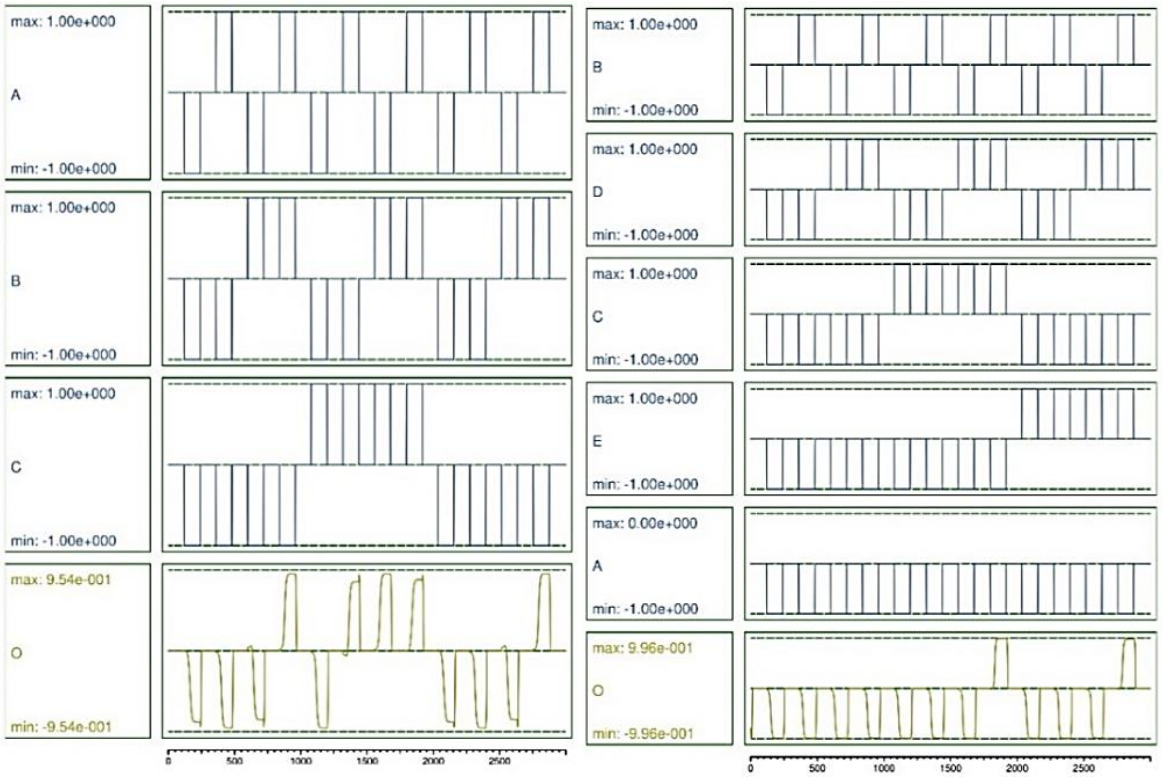



Figure 5. The structure of (a) five-input minority gate, (b) NAND gate, and (c) NOR gate

## 3. RESULTS AND DISCUSSION

Utilizing QCADesigner 2.0.3, simulations of majority, minority and proposed logic gate structures are performed [30]. The bistable approximation-simulation-engine and the coherence-vector-simulation-engine are used to simulate proposed architectures, and results were obtained from both engines. The default cell size is considered as 18×18 $nm^2$. In the simulations a total of 28,000 samples along with a 100 repetition per sample were utilized to support output results. We considered different conditions for the simulation test for exciting conditions; therefore, it approves consistency and success our designs.

The simulation results of minority and majority gates are shown in Figure 6. The 3-input majority is represented in Figure 6(a) and results of 5-input majority are shown in Figure 6(b). In both figures, it can be observed that the output produces the logic 1, when there is a majority of 1's in the input pattern; otherwise, the gate produces logic 0. By fixing the 1-majority input either 1 or 0, we can design a two-input AND or OR gates. If one of polarization input cell is fixed to -1 (logic-0), the majority act as AND. Similarly, if one of polarization of input cell is fixed to 1 (logic-1), the majority act as an OR.




(a) (b)

Figure 6. Results of (a) 3-input majority and (b) 5-input majority gates

Based on functional operation of minority gate, it can be observed that the output produces the logic 1, when there is a minority of 1's in the input pattern; otherwise, the gate produces logic 0. By fixing two inputs of minority gate either 1 or 0, we can design a three-input NAND or NOR gates. The simulations 3-input NAND and NOR are represented in Figure 7. It can be observed that functionality of logic gates is satisfied with the waveforms, that shows the accuracy of the design.

The comparison of cell area and power of different majority are analyzed and shown in Table 2. It has been noticed that the Type-2 majority gate occupies more area and dissipates more power than Type-1 and Type-3. The area of Type-2 majority gate is almost double than the Type-1 and Type-3 and power dissipation is also near equal to two times of Type-1 and 3. However, Type-2 majority gate most recommended gate due to easy access of output port and the input ports are almost isolate to each other. The cell area and power dissipation comparison of five-input majority and minority gates are presented in Table 3. It can be seen that the minority gate occupies cell lesser area and lesser power dissipation compared to the majority gate. The loss of power dissipation is observed to be 10%.

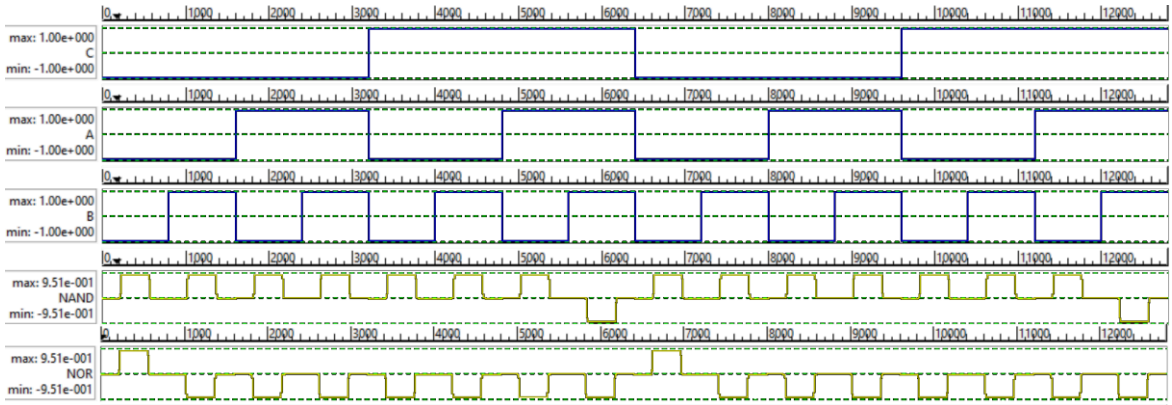



Figure 7. Timing waveform of three-input NAND and NOR gates

Table 2. Comparisons of cell area and power dissipation of different majority gates

| Parameter | 5- Majority Gate | | |
|---|---|---|---|
| | Type1 | Type2 | Type3 |
| Cell Area (nm$^2$) | 3,234 | 7,452 | 3,234 |
| Power Dissipation (meV) | 7.9 | 19.0 | 9.7 |

Table 3. Comparisons of cell area and power dissipation of majority and minority gates

| Parameter | 5-majority gate | 5-minority gate |
|---|---|---|
| Cell Area (nm$^2$) | 7,452 | 7,128 |
| Power Dissipation (meV) | 19.0 | 17.2 |

The comparative results of QCA with that of CMOS logic gates designed at 32 nm technology node is placed in Table 4. The comparison results show that the area occupied by the QCA are very small compared to CMOS logic gates. Moreover, the power of QCA is in order of eV; whereas the power of the CMOS is in order of µW.

Table 4. Comparisons of QCA and CMOS logic gates

| Area (µm$^2$) | NOT | AND | OR | NAND | NOR |
|---|---|---|---|---|---|
| QCA | 0.045 | 0.07416 | 0.0716 | 0.10021 | 0.10021 |
| CMOS | 2.87 | 8.92 | 8.94 | 8.12 | 8.23 |

It is worthy to discuss that QCA cells are highly sensitive to temperature changes. Therefore, we performed the temperature sensitive analysis and results are shown in Figure 8. The 3- majority and 5-majority gates and represented in Figures 8(a) and 8(b), respectively. The graph is drawn between the change in temperature and cell polarization. As can be seen from Figure 8(a), it is polarization maintains its value nearly constant level up to 15 K, and further increasing the temperature the cell loses the polarization and becomes unstable. The same analysis can also be analyzed from Figure 8(b). Therefore, we may conclude that the QCA gates computational fidelity is good for the temperature range $T < 15$ K, more or less acceptable in the above range of 15 K.

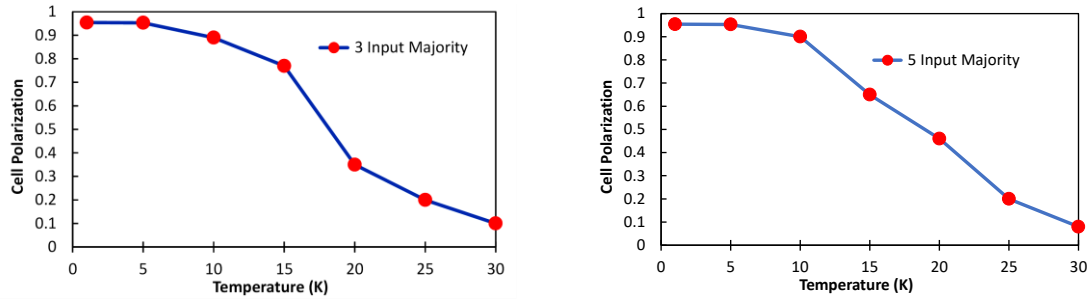



Figure 8. Temperature variations impact on polarization (a) three-input majority and (b) five-input majority gate

Less complex combinational circuits like half-adder and half-subtractor are also designed in the QCA technology and shown in Figure 9. The adder and subtractor QCA circuits are shown in Figures 9(a) and 9(b) and their temperature sensitive analysis results are shown in Figures 9(c) and 9(d). It can be observed that the cell becomes unstable at the temperature of 10 K.

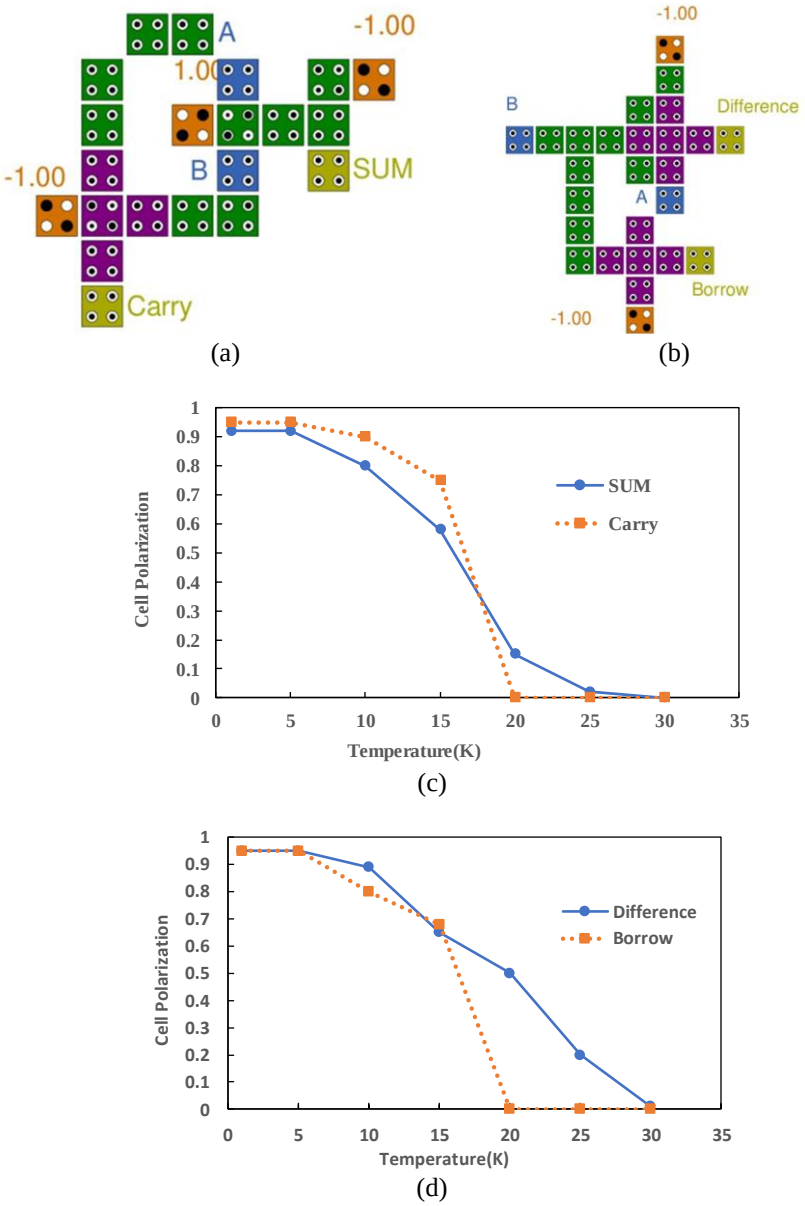



Figure 9. Design of combinational circuits in QCA (a) half adder, (b) half subtractor, (c) temperature variation analysis of half adder, and (d) temperature variation analysis of half subtractor

## 4. CONCLUSION

This work analyses a majority and minority gate using QCA. The majority gates are designed in various possible styles. The power dissipation and circuit area of Type-2 majority is observed to be higher than the other types. However, Type-2 majority is recommended for the design of digital logic gates in QCA due to high fan-out and less noise sensitivity. The majority is further used to design the AND and OR gates and the minority gate is used to design the NAND and NOR gates. It is observed that all logic gates are correctly functioning. Also, less complex combinational circuits like half adder and subtractor circuits are also designed. Finally, temperature sensitive analysis is performed for 3-and 5-majority gates and observed that circuits become unstable at temperatures more than 15 K. The logic gates can be extended in the future to design complex digital circuits.

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