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A survey of scan-capture power reduction techniques

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ABSTRACT

With the advent of sub-nanometer geometries, integrated circuits (ICs) are required to be checked for newer defects. While scan-based architectures help detect these defects using newer fault models, test data inflation happens, increasing test time and test cost. An automatic test pattern generator (ATPG) exercise's multiple fault sites simultaneously to reduce test data which causes elevated switching activity during the capture cycle. The switching activity results in an IR drop exceeding the devices under test (DUT) specification. An increase in IR-drop leads to failure of the patterns and may cause good DUTs to fail the test. The problem is severe during at-speed scan testing, which uses a functional rated clock with a high frequency for the capture operation. Researchers have proposed several techniques to reduce capture power. They used various methods, including the reduction of switching activity. This paper reviews the recently proposed techniques. The principle, algorithm, and architecture used in them are discussed, along with key advantages and limitations. In addition, it provides a classification of the techniques based on the method used and its application. The goal is to present a survey of the techniques and prepare a platform for future development in capture power reduction during scan testing.

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1. INTRODUCTION

Switching activity happens during scan capture when a value in a scan cell changes after the capture cycle is applied [1]. Excessive switching leads to increased power, leading to yield loss. Unlike shift power, capture power reduction is a more complex problem to solve since vectors are applied during the capture cycle considering circuit functionality and are usually strongly correlated. Though a few flip-flops are used to detect specific faults and are expected to toggle during the capture cycle, the value in a few additional flip-flops also changes during the cycle. Transitions of signals from the additional flops create undesired switching and may result in hot spots.

At-speed scan testing is the most widely adopted test strategy to detect speed-related defects. It offers advantages like minimal tester requirements and high quality. For example, a low-speed tester can provide a clock for shift operation. In contrast, a clock for capture operation could be generated using on-chip phase locked loop (PLL). A control circuit is added, which chooses the output of PLL instead of the shift clock coming from the tester during the capture operation.

Increased switching during testing creates excessive IR-drop than functional operation [2]. In particular, the IR drop resulting during the at-speed capture phase has a significant impact. Switching activity during the launch cycle could be up to 33% higher than a functional vector [2]. Increased switching activity results in excessive IR-drop that increases delays on circuit paths and causes timing violations. Eventually, the

capture cycle loads an incorrect value, as shown in Figure 1, causing a test-induced malfunction. These malfunction leads to false delay failures and discarding good chips as faulty, ultimately reducing the final yield. Rated frequency, which is usually high, is used for at-speed capture testing, resulting in a high risk of test-induced malfunction. Due to decreasing supply voltage, shrinking geometries (10 nm→7 nm→5 nm→3 nm →1.8 nm), growing gate count, and increasing clock frequencies, such test-induced yield loss is rapidly worsening [3], [4].

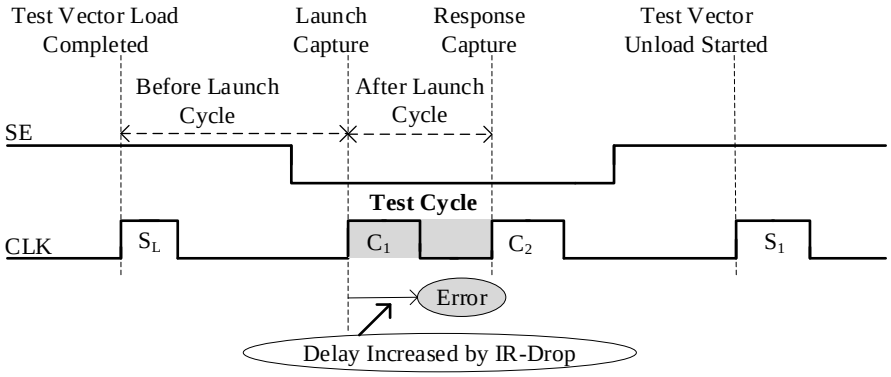

Figure 1. Capture malfunction in at-speed testing [5]

2. BACKGROUND

Only a few new faults get detected per pattern after the initial stages of pattern generation. While only the flip flops required to detect those new faults need to toggle, other flip flops could be prevented from capture operation. Furthermore, fault coverage can be maintained even after preventing these other flops from capturing. These capture preventions eliminate switching in those flip flops themselves as well as switching in combination logic driven by them. This property makes test data manipulation the most attractive technique for capture power reduction.

Two schemes are used for the generation of at-speed scan capture clocks: i) launch-off capture (LOC) or broadside, and ii) launch-off shift (LOS) or skewed load. Launch-off capture scheme-based architectures are popular as they generate patterns that activate fewer false paths. In addition, they are more straightforward for physical implementation due to non-timing critical requirements on scan enable (SE) signal [6].

Delay fault detection is done by applying a pair of bit vectors <V1 V2>. Initialization of the fault site is done by vector V1, and transition on the fault site is launched using vector V2, which also propagates the transition to primary outputs or pseudo-primary outputs. The main difference between launch-off capture and launch-off shift is the generation of vector V2. With launch-off capture, V2 depends on the circuit's functional response to V1, while the launch-off shift obtains V2 by shifting vector V1 by 1-bit [7]. Therefore, the launch-off capture method has two capture cycles, while the launch-off shift contains one. In LOC, the first capture cycle could be a slower frequency, but the second capture cycle needs to be rated at operating speed. Likewise, the duration from the last-shift cycle edge to the capture cycle edge for LOS must be at the rated operating speed. The scan-enable signal is operated during these two methods, as shown in Figure 2.

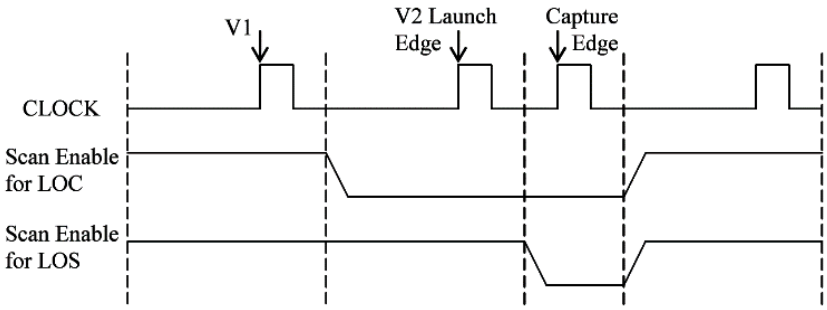

Figure 2. Clock and scan enable relationships during LOC and LOS testing [7]

2.1. Switching activity reduction during the capture cycle

During the capture cycle, flops are loaded with capture values. These values will be dependent upon the scan load values and functional logic. During the capture cycle of test patterns, the switching activity at a flip-flop can be mapped to one of the four scenarios shown in Table 1 [8]. The pattern generator fills bits required for fault detection and leaves remaining bits as don't care.

Table 1. Scenarios at a flop during capture operation and possible techniques to reduce switching [8]

Scenarios	Flop value before capture	Flop value after capture	Frequency of occurrence	Technique to reduce capture switching
A	X	Care bit	Low	X-fill
B	Care bit	Care bit	Low	No optimization required
C	Care bit	X	Medium	Clock gating aware automatic test pattern generator (ATPG)
D	X	X	Very high	X-fill or clock gating aware ATPG

Multiple techniques were presented to reduce scan capture power. While sections 4 and 5 present their details, Table 1 shows the usage of commonly used techniques for the following four scenarios:

- Scenario A: To minimize transition during capture, a don't care value could be replaced with the same value as the care bit. The X-filling technique could be effectively used for this vector manipulation.
- Scenario B: This does not have scope for improvement.
- Scenario C: A more straightforward way to reduce transition could be disabling the clock to the cells during the capture cycle. Disabling could be done by the clock gate enable logic using appropriate load values on corresponding scan cells during the last shift cycle.
- Scenario D: This transition could be minimized using the clock gating disable method if the same clock gating drives multiple flops. If this is proven ineffective, X-filling could be done based on a selective bit.

2.2. Previous surveys on low power test

Basker and Arulmurugan [9] presented a survey on low-power testing of very large-scale integration (VLSI) circuits, which summarizes power reduction techniques, including scan reordering, clock splitting, bit swapping-linear feedback shift register (BS-LFSR), and pattern generator for built-in self-test (BIST). It also describes basic X-filling techniques like 0-fill, 1-fill, and MT-fill. These techniques fundamentally work towards reducing shift power. The paper summarizes capture power reduction techniques very briefly.

Another survey for test power minimization is presented in [10]. Along with shift power reduction techniques for regular-scan, it summarizes power reduction when scan compression methodologies are being used. However, this survey also only covers capture power reduction techniques partially. These two surveys were presented in the years 2012 and 2013, respectively, and researchers have presented multiple techniques focusing on capture power reduction since then. This paper summarizes those techniques.

2.3. Abbreviations, acronyms, and terminology

Few abbreviations and acronyms are used throughout this paper. Table 2 gives their full form. Additionally, this section defines a few key power terms.

Table 2. Abbreviations and acronyms

Abbreviation	Full Form	Abbreviation	Full Form
ATPG	Automatic test pattern generation	SOC	System on chip
DFT	Design for Test	CAD	Computer-aided design
SA	Switching activity	SDQL	Statistical delay quality level
CUT	Circuit under test	SAT	Boolean satisfiability
WTM	Weighted transition metric	LSA	Launch switching activity
WSA	Weighted switching activity		

Terminology:

- Peak power: It is defined as the maximum power dissipated during a clock cycle [11]. Assuming T_c is the clock period broken further into intervals of size Δt, P_{ij} is the instantaneous power dissipated during the j^{th} minor interval of a pattern i, the peak power consumed during pattern i is (1),

$$Peak\ power(i) = \frac{\sum_j P_{ij}.\Delta t}{T_c} \quad (1)$$

Excessive peak power leads to package damage and reliability impact.

– Instantaneous peak power: For pattern *i*, instantaneous peak power is defined as $Maxj\{P_{ij}\}$. A large instantaneous peak power results in failure due to an excessive drop in power supply voltage.

2.4. Contribution and organization of this paper

Academia and industry have proposed many techniques to reduce the scan capture power. This paper describes the principle, algorithm, and architecture details used in them. It classifies the techniques, discusses the advantages and disadvantages of each type of those techniques, and enables selection for particular usage.

The organization of the remaining sections of this paper is as follows. Section 3 classifies techniques based on the principle used and its application. Details of the techniques to reduce power are discussed in sections 4 and 5. Finally, section 6 discusses the pros and cons of the techniques, while section 7 concludes the paper.

3. CLASSIFICATION

Over the years, researchers have developed many variants of techniques to reduce scan capture power. This survey covers the techniques presented in recent times. These techniques are divided into categories based on the fundamental principle and evolved variants. Tables 3 to 5 present these categories.

Table 3. Structural techniques

Sr.	Technique	References
1	Scan segmentation and using non-overlapping or staggered clocks	[12]–[16]
2	Test point insertion	[17]
3	Special scan flip flop †	[18]
4	Clock gating	[19]

Table 4. Pattern optimization techniques

Sr.	Technique	References
1	X-filling	[18], [20]–[27], [28]–[32]
2	X-identification	[27]
3	Test cubes merging	[33]
4	SAT/ILP solver	[20], [26]–[30]
5	Pattern reordering	[18]
6	Evaluating and choosing X-fill	[34]–[36]
7	Dictionary-based test data compression	[37]

Table 5. Specific usage techniques

Sr.	Technique	References
1	Launch-off shift (LOS) usage	[18], [31]
2	Launch-off capture (LOC) usage †	[12], [17], [18], [20], [22]–[27], [28]–[31], [33]
3	Techniques using layout information †	[12], [19], [20], [22], [25], [29], [38]

† - Sections 4 and 5 do not have separate sub-sections for these techniques. They are covered as part of other sub-sections.

4. STRUCTURAL TECHNIQUES

4.1. Scan segmentation and using non-overlapping or staggered clocks

Jiang *et al.* [12] presented a scan segmentation technique that reduces power during both the shift and capture phases. It creates scan chains based on layout information. The chains are further split into segments which are operated using different clocks chosen using a decoder. Only a group of segments are enabled during the shift, as well as launch and capture. All flops capture response when a few successive launch and capture clocks are applied. Since only a few flops are enabled during the capture cycle, switching activity reduces, thereby reducing power. However, one problem with multiple capture cycles is wrong responses due to data dependencies between different flops. The technique presents an algorithm that analyses flops' dependency by drawing an S-graph, as shown in Figure 3, and uses the information to create segments. Techniques presented in [39], [40] also create segments considering data dependency. They try to reduce paths crossings between segments groups which results in more fault coverage loss compared to the method proposed in [12] since the impact of a violating flop to fault coverage is more than a violating path.

Sun *et al.* [13] presented a segmentation-based architecture to reduce power during the capture cycle. It divides the scan chains into equal-length segments enabled selectively during the capture cycle. A chain having individual bits for each segment is used to enable them. Each pattern is analyzed to determine if a segment detects a new fault. This information is used to program the control chain at the beginning of each

pattern. While this technique directly controls power consumption during capture, it also reduces shift-out power. This is because the disabled segments shift out identical values as a shift in, preserving the effort made by the ATPG algorithm to reduce shift power for those segments.

Sun *et al.* [14] presented a similar technique with an enhancement for enabling segments. Instead of using a control chain, it inserts control bits to enable segments in the chain, as shown in Figure 4. Then it uses a commercial ATPG tool that automatically programs these bits. This technique offers advantages as no post-processing of patterns to add control bit programming is required, and patterns generated by ATPG can be used as it is.

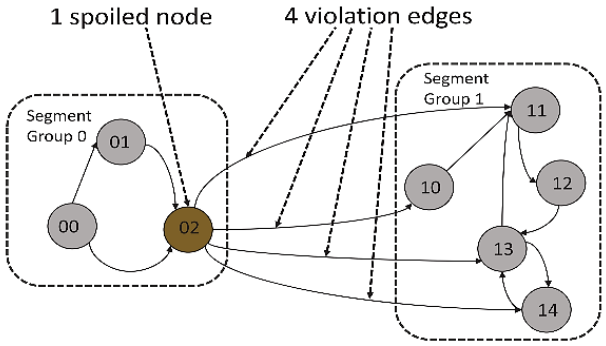

Figure 3. Modelling of data dependency violations [12]

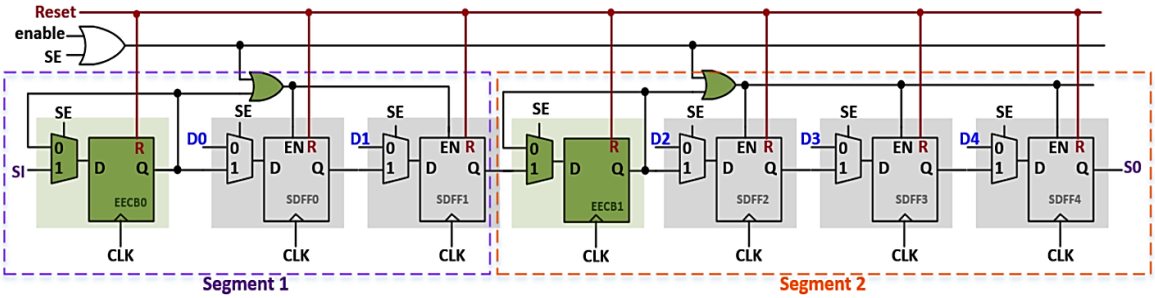

Figure 4. Scan architecture with embedded control for enabling segments [14]

Lim *et al.* [15] presented a scan bypass technique that bypasses segments consisting of don't care bits. It starts with the classification of cells based on stimulus and response values. Combinations (0/1, 1/0) are given the highest weight, (0/1, X), (X, 0/1) as a medium, and (X, X) as the lowest. Weight values of each cell are calculated for the entire pattern set, and scan cells are reordered based on the descending value of weight. Next, the chains are split for the required length. It also performs pattern reordering to match shifting length across successive patterns since length mismatch may occur due to bypassing segments. Switching activity during capture is reduced due to savings from bypassed segments toggling.

4.2. Test point insertion

A technique to reduce at-speed scan capture power by adding test points is presented in [17]. Low-capture-power test points (LCP-TPs) are used to reduce LSA in high-capture-power (HCP) regions while maintaining fault coverage and a low test-pattern count. The technique identifies HCP regions and calculates effective test point (TP) locations based on a test set and preliminary layout information.

Switching activity is measured either globally or regionally. A global estimate can easily be obtained early in the design flow based on a logic netlist. The disadvantage is that the estimate is unfocused. A test with a low global switching activity can still have a very high regionally concentrated switching activity, which causes problems. Hence, layout information is needed for a regional estimate.

The switching activity is often not evenly distributed across the circuit, depending on the design. As a result, some regions may have high switching activity. One more reason is that ATPG techniques often excite similar easy-to-control or easy-to-observe signals to provide high compaction. The method introduces

controllability and observability test points on signals going to and coming out of HCP regions. This, in turn, helps to avoid the high switching activity. Unfortunately, inserting LCP-TPs at all possible boundary signals is impossible since test points are expensive in terms of area.

The method partitions a circuit into regions using layout information DEF (*.def). The initial test set is simulated, and HCP regions, i.e., regions with a WSA value above a certain threshold, are identified for each vector. Boolean satisfiability (SAT) based procedure presented in [20] is used to identify effective test points. The optimization-SAT procedure identifies TPs that are necessary to detect faults in an HCP region and, at the same time, do not violate its threshold.

4.3. Clock gating

Shaikh *et al.* [19] presented a method that uses clock gating cells to control switching during at-speed scan capture. First, it analyses clock gating cells and flops relevant to them. Next, it creates groups of the clock gating cells and adds logic to control them using separate test enable. Finally, patterns are generated by enabling one group, thereby controlling simultaneous switching during capture.

5. PATTERN OPTIMIZATION TECHNIQUES

5.1. X-filling

Given that patterns generated using the automatic test pattern generation (ATPG) tool have many don't care bits, the X-filling technique is very effective for reducing peak power during the capture cycle. It follows a process to assign logic values to unspecified bits in test cubes to reduce switching activity in the resulting fully specified test vector. Logic values to be assigned are determined to minimize Hamming distance between the test vector and its response value or to reduce the weighted node transitions in the circuit.

Li *et al.* [21] presented a method to create a set of at-speed patterns that do not cross a threshold limit of capture power. First, it analyzes an initial set of patterns for capture power and removes patterns having power above the threshold. Then it performs X-filling on the remaining patterns to get additional coverage for faults detected by the discarded patterns. Finally, it generates new patterns for faults that remain undetected.

Delays increase on a logic path as well as a clock path due to IR-drop resulting from switching activities during the launch cycle of at-speed capture. Figure 5 shows an example of such a circuit. Asada *et al.* [22] presented a technique to reduce this switching activity, avoiding false capture failures. The paper proposes using static approximation methods to get a list of long paths with a risk of IR-drop-induced capture failures. First, it calculates the WSA of neighboring logic and the clock path of this path. Then, it uses layout and power distribution network information to find the impact area of the aggressor gates. The algorithm identifies free bits in a vector that can reach the impact area affecting the logic path and later performs X-filling to reduce switching activity in the impact area. Similarly, it performs X-filling to reduce switching activity in the impact area of the clock path. Considering the impact of the clock path in identifying risky logic paths provides more accurate results than the method proposed in [41], [42], which assumes an ideal clock in logic path analysis.

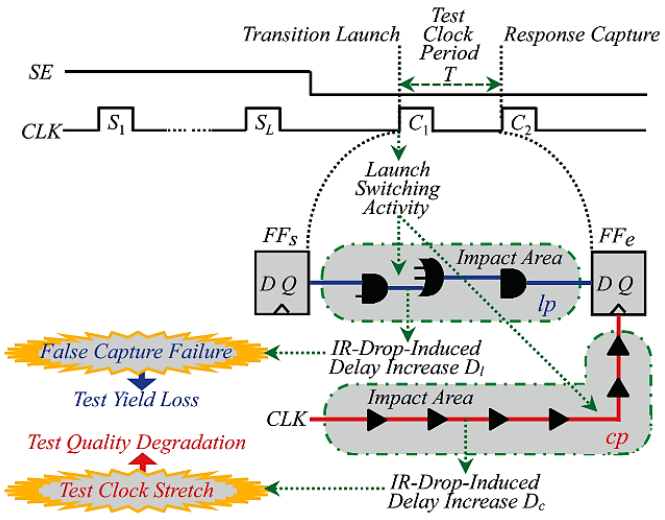

Figure 5. Impact of LSA in LOC-based at-speed testing [22]

Using an IR-drop distribution profile for switching power estimation provides better results [43]. Tsai *et al.* [23] presented a technique that considers the chip power network to estimate IR drop distribution for a test pattern. It performs logic simulation to note switching signals in each vector and adds their impact to derive the total IR drop due to the test vector. The test pattern generation engine fills X's randomly, then flips them one after another. Each pattern is then evaluated for IR drop and removed if the IR drop is above the requirement. The bit-flipping process is repeated till patterns are generated for all faults. Hou *et al.* [24] proposed another technique that improves the serial bit-flipping computation. It performs structural analysis and divides inputs into strongly related groups based on the fanout, as shown in Figure 6. The inputs with the highest relation, i.e., the most common fanout cone, are chosen, and their unspecified bits are assigned concurrently. Assigning multiple bits at a time significantly reduces the CPU time and produces better IR-drop cost reduction compared to [23].

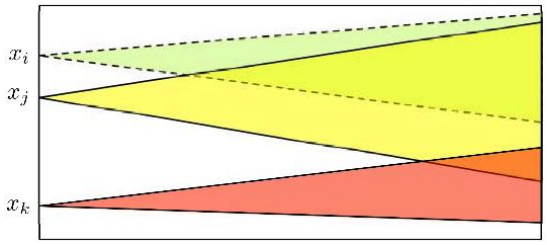

Figure 6. Related inputs groups–highly related (xi/xj), less related (xj/xk), and non-related (xi/xk) [24]

Ding *et al.* [25] presented a test pattern modification method to reduce capture cycle-induced IR-drop in hotspots. It calculates IR-drop contributions by every node to the nodes in the hotspot region and modifies only a few don't care bits rather than modifying all don't care bits. It starts with simulation using SDF annotation and note patterns that result in IR-drop larger than the threshold. For patterns resulting in IR-drop hotspots, it calculates the contribution to the impact by all logic gates to the gates in the hotspot region. Then it modifies X's, which reduces those impacts. The technique has been shown to create a pattern set with no hotspots, lesser test length, and better fault coverage than a pattern set created using the commercial power-aware ATPG tool.

Hosokawa *et al.* [26] presented an X-filling technique to reduce capture power. It aims to reduce the number of transitions on internal signals instead of flip flops, which improves power estimation accuracy. It uses initial test cubes and performs X-filling iterations on them. During X-filling iterations, it calculates the WSA of test vectors considering the fanout of cells, and vectors with a value higher than a threshold are carried forward for the next iteration.

5.2. X-identification

X-identification is a process of identifying possible X-bits in a set of fully specified test vectors by maintaining the same fault coverage. A test set with additional X-bits obtained using X-identification help to obtain a compact test set since a test cube containing many X-bits is more flexible than one containing few X-bits. Dynamic compaction and X-filling together could be used for compaction. Test vector count may double if compaction and X-filling are applied without X-identification [44]. The X-identification technique can find over 50% of the total X-bits [45].

Hosokawa *et al.* [27] presented another technique which complements the technique he presented in [26]. It performs X-identification before applying X-filling to test vectors. First, it uses fault propagation and justification method to identify X's in test vectors without affecting fault detection status. Then it uses these new X's during the X-filling process to reduce switching on internal signals. Figures 7 and 8 show the result of the application of these methods. The values with squares show transitions. This technique produces vector (0, 1, 0, 0, 1), which reduces the number of transitions on internal lines to 5, which is 44% less compared to transitions (*count* = 9) using the technique in [26].

5.3. Test cubes merging

Pomeranz [33] presented a technique to generate low-capture at-speed scan patterns that produce a compact low-power test set by merging test cubes. The technique uses a functional test to understand the maximum switching activity allowed. It first generates broadside tests for circuit states to be tested using scan-in values. While generating these tests, it uses the maximum switching activity of the functional test as bound.

For many patterns, i) faults detected by each of these tests are low since possible circuit values achievable using scan-input bit stream are limited, and ii) switching activity is less when compared to the bound derived from the functional test. The technique merges test cubes from the broadside test patterns to create a compact test set. It works towards improving fault coverage while limiting maximum switching activity to the bound set forth by the functional test. Deriving a test set using this technique also avoids testing patterns with unnecessarily low switching activity.

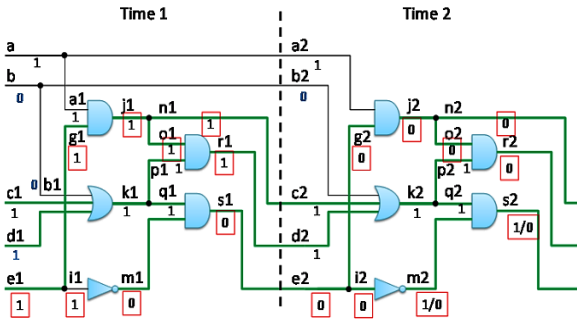

Figure 7. Pattern modification using [26]

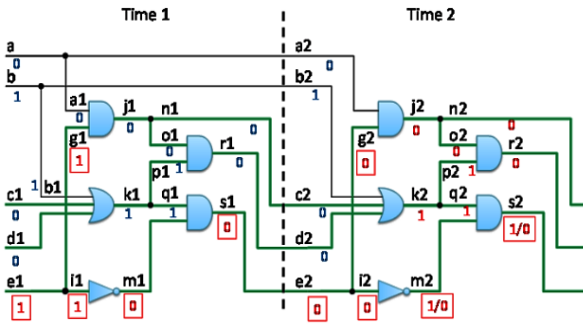

Figure 8. Pattern modification using [27]

5.4. SAT/ILP solver

The Boolean circuit satisfiability (SAT) method is used to find a solution to a problem defined by Boolean expressions. The expression consists of Boolean variables and logic gates. The method finds variables' values that satisfy the expressions [46]. WSA metric is widely used to measure switching activity during the test. Each signal in the circuit needs to be considered in this measurement. It needs to be calculated for every test vector to understand patterns above a threshold. The vectors are then modified to keep switching activity below the threshold. Boolean satisfiability (SAT) based methods can be used to perform search operations of correct test cube bit values. The method describes circuits as expressions representing AND, OR, and NOT gates by symbols $\wedge$, $\vee$, and $\neg$ respectively. Due to the effective reasoning engines, these methods perform better in solving hard problems.

Yoshimura *et al.* [28] presented a method to reduce power dissipation due to high switching activity at the launch cycle of at-speed scan capture. It performs test data manipulation to reduce the number of flip-flops with transitions at the launch cycle. Logic circuits, inputs, and outputs are represented in conjunctive normal form (CNF), as depicted in Table 6. An SAT solver is used to find test cube values such that transitions will not appear on all the selected flops. It also considers the impact of power dissipation on the whole circuit while deciding the order of flip-flops to block their outputs from transitioning. Selecting order this way gives better results compared to the selection methods used in [47], which assumes the effect of transition due to all flip-flops being the same.

Table 6. Rules to transfer circuit to CNFs [28]

Type	Input	Output	CNF
AND	X, Y	Z	$(X \vee \overline{Z}) \wedge (Y \vee \overline{Z}) \wedge (\overline{X} \vee \overline{Y} \vee Z)$
OR	X, Y	Z	$(\overline{X} \vee Z) \wedge (\overline{Y} \vee Z) \wedge (X \vee Y \vee \overline{Z})$
EXOR	X, Y	Z	$(\overline{X} \vee Y \vee Z) \wedge (X \vee \overline{Y} \vee Z)$ $\wedge (\overline{X} \vee Y \vee \overline{Z}) \wedge (\overline{X} \vee \overline{Y} \vee \overline{Z})$
NOT	X	Y	$(X \vee Y) \wedge (\overline{X} \vee \overline{Y})$
Fanout	X	Y, Z	$(\overline{X} \vee Y) \wedge (X \vee \overline{Y}) \wedge (\overline{X} \vee Z) \wedge (X \vee \overline{Z})$

Eggersgluss *et al.* [20] presents a technique that uses an SAT solver to eliminate high capture vectors in an at-speed scan test pattern set. First, it uses layout information from the DEF file to form physical regions of signals and gates. Then, it performs fault simulation using existing patterns to identify high-capture power regions and corresponding vectors. Finally, an SAT solver generates new vectors with low switching and replaces the high capture power vectors in the original pattern set with it. Since larger search space is used than X-filling, the technique offers better capture power reduction.

Hung *et al.* [29] presented a framework for 3D designs to update at-speed test patterns likely to cause yield loss resulting from induced voltage droop. It starts with calculating WSA for each pattern and simulates

patterns with the highest WSA to obtain the worst voltage droop. Based on the worst voltage droop, it calculates a scale factor for estimating increased path delays due to it. It obtains a list of paths whose slack becomes negative by applying the scale factor. Then it generates new patterns for faults on those paths and performs X-filling using an algorithm based on integer linear programming (ILP). The ILP model declares the functionality of each Boolean logic gate using a set of linear constraints. The new patterns are generated without filling in Xs. These Xs in each pattern are filled later to reduce voltage droop during the capture cycle.

Gulve and Singh [30] presented a technique that uses ILP solver CPLEX to fill the don't care bits to reduce capture power during at-speed scan testing. It models the functionality of CUT as linear programming equations with optimization functions as minimized switching. Digital circuits can have only 0/1 values. The functionality of the design is modeled with a set of zero-one linear problem (ZOLP) constraints. The variables are assigned values based on test pattern contents in the second step.

5.5. Pattern reordering

Test pattern reordering significantly impacts switching activity, and intelligent reordering has been shown to reduce switching activity in [48], [49]. Potluri *et al.* [18] used this phenomenon and presented a technique based on pattern reordering to reduce peak power occurring during launch to the capture cycle of the LOS at-speed testing. Pattern reordering reduces switching activity only if the states of combinational logic change during the capture cycle but remain unaltered during the shift and launch phases. The technique uses a special scan flip flop, shown in Figure 9, to preserve the combinational state of a circuit between launch clock pulses of successive patterns. In addition, an algorithm keeps track of don't care bits. It performs X-filling after reordering to reduce the switching activity further. The technique has been shown to reduce peak power in both circuits, having test cubes with fewer and more don't care bits.

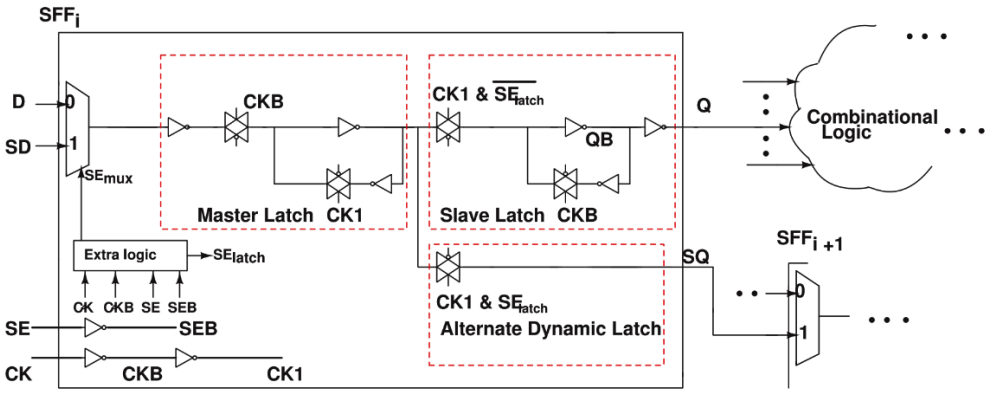

Figure 9. Scan flip flop with logic state preserve feature [18]

5.6. Evaluating and choosing X-fill

Wu *et al.* [50] presented a comparative study of various X-filling methods for test power reduction. Analysis with 0-fill, 1-fill, adjacent-fill, and random-fill algorithms shows that the filling techniques' performance depends on the circuit under test. One technique may be more or less efficient depending on the circuit under test. Sinduja *et al.* [34] presented a technique based on these observations. It performs 0-fill and 1-fill for each vector and computes switching activity for them. Next, it performs a switching activity comparison for each vector and selects the vector with less switching for addition to the final pattern set. The technique has shown a reduction in average shift and average capture power. Techniques presented in [35], [36] also use different filling methods and choose the pattern with lesser switching activity.

5.7. Dictionary-based test data compression

Sismanoglou and Nikolos [37] presented a technique to reduce capture power during launch-off capture-based at-speed scan testing that uses dictionary-based test data compression. It starts by extracting representative slices and storing them on-chip in a dictionary using the method described in [51]. Then it randomly fills Xs and produces test vectors. For vectors with high switching activity, it uses a bit correction method which reduces the Hamming distance of the vectors to its response. The technique has shown a reduction in both average and peak power with minimal degradation of compression efficiency. Karmakar and Chattopadhyay [52] also proposes a dictionary-based technique; however, it only targets power reduction during shifts.

5.8. LOS usage

LOC and LOS are two prevalently used schemes for at-speed testing. Fault coverage obtained using the LOS method is usually better, but it dissipates more capture power than LOC. Most other techniques presented in this paper also help to reduce power during the capture cycle of LOS testing. However, only some techniques have been presented that focus on power reduction during LOS testing. This section summarizes them.

A technique to perform X-filling to reduce the peak capture power in LOS is presented in [31]. It assumes that the DFT architecture preserves the state in which the combinational logic settles down after launching the current test pattern until the launching of the following test pattern. One method to achieve this is blocking flop outputs during scan-in and scan-out operations. Suppose the combinational state preservation property can be ensured. In that case, the combinational part of the circuit behaves as if the test patterns are applied one after the other. Once this property is satisfied, the sequential circuit behaves like a combinational circuit from the point of test patterns application. Thus, the test pattern ordering techniques proposed earlier in [48], [53] for reducing test power in combinational circuits become equally effective for sequential circuits.

The technique chooses a Dynamic Programming paradigm that considers the global picture. It computes the optimal value to fill the X-bits to achieve the best reduction in peak toggles. The objective of X-filling is to reduce Hamming distance between test cubes, as shown in Table 7. The technique is based on converting don't care (X-bit) stretches 0XX...X1 and 1XX...X0 into smaller X-bit stretches 0X1 and 1X0, respectively. In addition, the paper presents a test vector ordering algorithm called interleaved test vector ordering (I-ordering) which converts the don't care stretches into a moderate size which helps to fill those Xs optimally later to achieve peak toggle savings.

A similar technique that uses a special flip-flop is presented in [18] to reduce capture power during LOS testing. The special flip-flop preserves data between shift to launch cycle, enabling effective use of reordering patterns. In addition, it performs X-filling after reordering, which further reduces the power. Another X-filling technique is presented in [50] for LOS-based pattern generation. However, one limitation of it is its heuristics do not offer a performance guarantee.

Table 7. Test cubes before and after X-filling with [31]

(a) Initial test					(b) X-filling					
V1	V2	V3	V4	V5	V1	V2	V3	V4	V5	
0	X	X	1	X	0	1	1	1	1	
1	X	X	X	0	1	1	1	1	0	
0	X	X	1	X	0	0	1	1	1	
1	X	X	X	0	1	1	1	1	0	
1	X	1	X	0	1	1	1	0	0	
X	0	X	X	1	0	0	1	1	1	
1	0	X	X	1	1	0	0	1	1	
						2	2	2	2	(toggles)

6. DISCUSSION

Each technique presented in sections 4 and 5 offers unique advantages and disadvantages. While choosing a scan power reduction strategy for a SOC, constraints like impact to design performance, test pattern inflation, fault coverage loss, and design flow compliance should be considered. This section presents a summary of the advantages and disadvantages. It also lists critical challenges to be worked on in the future. These together will also help the SOC designers formulate a power reduction strategy.

– Scan segmentation and using non-overlapping or staggered clocks

Though structurally based, these techniques do not affect the performance of the design. Commercial CAD tools can be used directly to generate patterns with the technique presented in [14]. They reduce power without any loss in fault coverage. However, techniques presented in [12], [39], [40] result in coverage loss when used with those tools due to data dependency. A special algorithm needs to be developed to avoid loss.

– X-identification, X-filling, and test cubes merging

X-filling is a widely used technique for capture power reduction due to its unique advantage that it is post-ATPG and does not involve any impact to test circuit size and timing. However, one disadvantage of X-filling is that bit assignments done for fault detection cannot be changed anymore. Hence, its effectiveness is limited and may lead tradeoff between a reduction in fault coverage and test pattern inflation. It also faces challenges when a test compaction circuit is added to the design. The on-chip decompressor fills many of the patterns' otherwise, don't care bits. Though the ATPG tool generates low capture power patterns for designs employing such decompressors, the effectiveness is limited since filling the don't care bits also needs to satisfy the requirement of the decompression algorithm.

All the test vector manipulation-based techniques like X-identification-filling and test cubes merging have the advantage of not requiring changing circuits for capture power reduction. The X-identification makes additional don't care bits available for X-filling usage. So, the techniques using X-identification along with X-filling are more effective as the X-filling algorithm gets more freedom for bit assignments.

- Test point insertion

Design modification-based techniques involving test points addition offer a solution to avoid fault coverage loss or test pattern inflation. For example, control and observe test points could be inserted to control the switching of high fanout nets or nets around high-switching logic. However, caution must be taken while selecting such test points as they may degrade performance by adding delay.

- Layout information usage

Switching activity reduction without considering physical layout information may not eliminate switching activity concentrated in a small region. Also, the long-sensitized paths are more prone to excessive IR-drop, but global switching reduction may not help to eliminate failures due to them. Another drawback of reducing global switching activity is test data inflation due to highly constrained search space. Therefore, the techniques that use layout information effectively produce high-quality patterns, especially for at-speed scan testing.

- Pattern reordering

These techniques are attractive as they do not incur any area overhead or change in test time while maintaining fault coverage. However, they have two drawbacks. First, they must perform multiple iterations to find the shorter distance between patterns. This results in high run time, which could be prohibitive for a larger set of patterns. Secondly, these techniques are effective only when a special flop, which supports preserving the logic state between two consecutive capture cycles, is used.

7. CONCLUSION

This paper presented a survey of techniques to reduce capture power in scan testing. Their characteristic features, advantages, and disadvantages are discussed. Few of these techniques have been deployed by vendors in commercial tools and are easier to integrate into the flow. However, most lead to inflation in test patterns. A framework needs to be developed to effectively use a combination of techniques like test point insertion and X-filling to improve performance in terms of lesser fault coverage drop, better testing quality, and lesser test pattern inflation. In addition, shrinking geometries, lesser power consumption specifications, and growing SOC sizes will require testing devices with newer fault models that, too, with increased frequency specifications. These requirements demand further explorations in reducing capture power during scan testing to maintain high test quality with less pattern count inflation, directly impacting the test cost.

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