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Single-phase binary phase-shift keying, quadrature phase shift keying demodulators using an XOR gate as a phase detector

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ABSTRACT

A single-phase/single-loop multiple-phase-shift-keying (*m*-PSK) demodulator is described. The demodulator relies on a linear range of an exclusive-OR (XOR) gate employed as a phase detector. The phase controller takes the average output from the XOR gate and performs a sub-ranging/re-scaling operation to provide an input signal to a voltage-controlled oscillator (VCO). The demodulator is truly modular which theoretically can be extended for an *m*-PSK signal. The proposed single-phase binary-/quadrature-PSK (BPSK/QPSK) demodulators have been implemented with low-cost discrete components. The core of the phase controller simply relies on number of stages of a full-wave rectifier and a linear amplifier built from well-known op-amp-based negative feedback circuits. The demodulator prototypes operate from a single supply of 5 V. At a carrier frequency of 100 kHz, both the BPSK and QPSK demodulators achieved the maximum symbol rate of 20 ksymbol/s respectively. At these symbol rates, the BPSK and QPSK demodulators deliver symbol-error rates less than 2×10^{-10} and 7×10^{-10}.

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1. INTRODUCTION

Phase shift keying (PSK) signaling such as binary phase shift keying (BPSK) and quadrature phase shift keying (QPSK) has been playing a significant role in modern digital communications [1]–[4] covering many areas of applications ranging from internet-of-things, mobile/smart devices, biomedical, wireless radio and optical data links [5]–[13]. One of the most widely-used BPSK demodulation technique in integrated circuits and systems relies on Costas loop [14], [1] which allows carrier frequency tracking and phase synchronization. With the use of a quadrature voltage-controlled oscillator (VCO) inside a phase-locked loop, the Costas loop has a deep impact on digital communications for many decades, especially on the receiver end [15].

In [6], Costas loop has been equipped with an extra frequency-locking mechanism for high data-rate BPSK demodulation in a high-speed wireless link. To improve the Costas loop's stability, a delay-locked loop (DLL) can be utilized to build a BPSK demodulator as demonstrated in [10], [8] for human-body communications. Linear multiplication and quadrature-signal generation from the VCO in the Costas loop pose a design challenge, especially at a high-frequency operation. A BPSK or QPSK demodulator using a single-phase VCO without any linear multiplier would be truly attractive. The BPSK demodulator in [16] employs a DLL-based clock-data recovery technique (CDR) with a half-rate bang-bang phase detector (BBPD) that directly extracts a synchronized clock signal from the BPSK signal. The demodulator employs a separate phase-locked-loop-based (PLL) and an *I/Q* generator to produce 0/90° signals to be used inside the

CDR loop. The demodulator works perfectly for a fixed/pre-defined carrier frequency that is an integer-multiple of the data rate. Extending this technique for higher-order PSK demodulation is possible but with a more complicate design on the CDR loop and the phase detector.

A locked-loop-based BPSK demodulator with a single-phase VCO in [5] is proposed for a biomedical data link. However, the structure still possesses two overlapping loops making the design rather complicated in controlling the loop stability. Another single-phase BPSK demodulator can be found in [11] which employs a phase-frequency detector (PFD) inside a single-loop structure. The demodulation principle practically relies on transition detection where it requires a dedicated data recovery block to obtain demodulated data from the transition detector. For both of these BPSK demodulators, it would be rather difficult to extend these demodulators for QPSK, 8-PSK or *m*-PSK demodulation.

Non-locked-loop BPSK demodulators are also feasible as demonstrated in [17] and [18]. The BPSK demodulator in [17] utilizes an injection-locking oscillator together with signal addition and amplitude detection for extraction. Although it offers a fairly competitive performance in term of energy-per-bit (E_b), the technique is prone to adjacent channel interference with a rather high bit-error rate (BER) of about 10-3. The all-digital non-locked-loop system in [18] delivers one of the best E_b-based BPSK demodulator's performance. Its principle is based on generating a data flipping signal whose rising edges indicate the instants when the recovered data should be flipped. The architecture is non-modular and not straightforward to be extended for demodulating high-order PSK signals.

The Costas loop can also be effectively extended for QPSK demodulation with additional circuitries to perform a specific phase-control function suitable for QPSK demodulation as in [19]–[22]. The modifications of these QPSK demodulator structures can be found in [6], [8] for high data-rate applications. These demodulators still employ a quadrature VCO where the accuracy of 0/90° phase difference is still eminent in the design. To the authors' knowledge, there is still no 8-PSK demodulator developed from the Costas loop, so its modularity is limited to a certain extent. The QPSK demodulator of the receiver in [12] utilizes a carrier recovery loop (CRL), multiphase generator and I/Q demodulator where a single-phase VCO is only required for down conversion. However, a low data rate of this demodulator from 2.4 GHz carrier results in a rather high E_b value. The non-locked-loop 8-PSK demodulator in [23] implemented with an InP 250 nm DHBT process delivers a very high data rate of 15 Gbps. It employs a comparator and a frequency divider for carrier recovery. However, deployment of power-hungry active circuits such as an amplifier, a bandpass filter and a power detector makes it less attractive.

In this work, an alternative PLL based *m*-PSK demodulator employing a single-phase VCO inside a single loop structure without any linear multiplier is introduced for BPSK and QPSK demodulation. The structure is very simple, modular and theoretically, it can be straightforwardly extended for demodulating any *m*-PSK signal. A phase controller suitable for this particular m-PSK demodulator is also introduced. These demodulators have been experimentally verified using low-cost, discrete components to prove the concept. The basic principle for PLL-based m-PSK demodulation is reviewed in section 2 which paves a way for proposing a single-phase/single-loop PLL-based m-PSK demodulator in section 3. Design and analysis of the circuit building blocks for the BPSK, QPSK demodulators are described in section 4. Circuit implementation and measurement is reported in section 5, and conclusion in section 6.

2. A BASIC PRINCIPLE OF PLL-BASED *m*-PSK DEMODULATION

One straight-forward technique to demodulate the BPSK, QPSK, 8-PSK or *m*-PSK modulated signals (with a carrier frequency of ω_c and phase $\phi_S(t)$) is to carry out phase comparison between the modulated *m*-PSK signal and a synchronized signal usually generated from a voltage-controlled oscillator (VCO) inside a phase-locked loop PLL as shown in Figure 1(a). The VCO's frequency ω_V is exactly equal to ω_c and its phase $\phi_{VCO}(t)$ is unchanged regardless of data symbol change. An output from the phase detector (PD), $\Delta\phi(t)=\phi_S(t) - \phi_{VCO}(t)$ can then be utilized to distinguish among these data symbols by various means such as the pulse width and the duty cycle where eventually the digital data bits can be recovered.

A PLL technique is one of the most popular strategies for achieving frequency locking, i.e., $\omega_V=\omega_c$. Furthermore, to extend the PLL technique for *m*-PSK demodulation, the VCO's input, VCO_{in} voltage has to stay quietly undisturbed where the VCO does not feel any change at its input after initial frequency lock so that the VCO output's frequency and phase remain unaltered even if the phase of the modulated PSK signal is varied according to the data symbol. This can be succeeded by inserting a phase controller (PhCtrl) between the loop filter and the VCO as shown in Figure 1(a) to keep VCO_{in} solidly fixed even if the output of the loop filter $u(t)$ level varies according to the modulated signal's phase. The obtained VCO_{in} voltage also needs to be at the correct value corresponding to the locked frequency complying with the VCO's characteristic. Each level of the analog signal $u(t)$ uniquely represents specific data symbol which has to be further decoded so the digital data bits can be fully recovered. The process transforming $u(t)$ to VCO_{in} plotted

against the phase difference, $\Delta\phi(t)$ is depicted in Figure 1(b) for BPSK and QPSK demodulation. Ideally, it can be seen that the phase controller's main function is to translate the different regions of the $u(t)$ curve by the function $g(\cdot)$ into an identical VCO_{in} curve over the different data phases. Note that if the carrier frequency changes, the loop will adjust itself and *re*-lock to this new frequency. This will basically move the voltage V_K along the VCO_{in} curves in Figure 1(b). In another word, this *m*-PSK demodulator loop is able to track with a carrier frequency and it basically possesses capturing and locking mechanisms similar to a typical PLL.

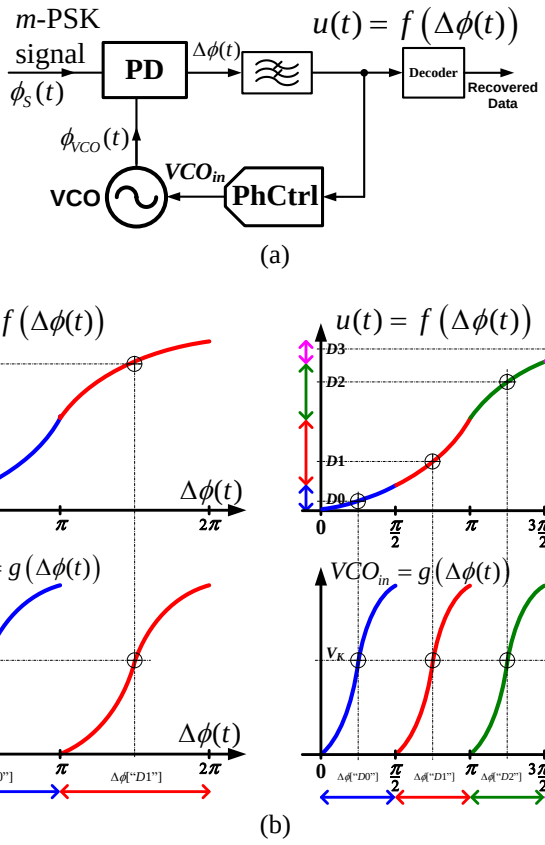


Figure 1. A conceptual PLL-based structure for m-PSK demodulation with a phase controller (PhCtrl) (a) basic structure (b) Phase controller's graph for BPSK (left) and QPSK (right)

3. PROPOSED PLL-BASED *m*-PSK DEMODULATORS WITH A SINGLE-PHASE VCO USING AN XOR GATE AS A PHASE DETECTOR

Practical realization of a locked-loop-based *m*-PSK demodulator will be addressed here where a single-phase VCO can be employed by exploiting the XOR gate's characteristic shown in Figure 2. Figure 2(a) shows a typical timing diagram of the XOR's input and output signals with its average output voltage, $\{vy\}$. The average output voltage, $\{vy\}$ against the phase difference, $\Delta\phi$ is characterized in Figure 2(b) indicating a repeating relation between $\{vy\}$=0 and *VDD* over $\Delta\phi=2n\pi$ to $2(n+1)\pi$ radians where n=0, ±1, ±2, The increasingly monotonic region of the XOR gate's $\{vy\}$–$\Delta\phi$ characteristic helps relax designing a phase controller as explained below.

The phase controller operates differently on $\{v_y\}$ depending on a particular order of PSK signal as depicted in Figure 3. On the first graph of Figure 3(a) and Figure 3(b), the data symbols of the BPSK and QPSK signals are represented by the unique $\{v_y\}$ level. The phase controller has to operate on these $\{v_y\}$ positions such that all the different data symbol levels on the $\{v_y\}$–$\Delta\phi$ graph have to be mapped to the same level similar to what has been presented in Figure 1(b). That is, $\{v_y\}$ is turned into $\{v_z\}$ and passed on to VCO_{in} which in turn produces a specific output frequency identical to the incoming carrier frequency. This essentially restricts VCO_{in} not to experience any significant change for different data symbols; hence the VCO's phase remains undisturbed after the initial frequency lock. Consider the BPSK scenario in

Figure 3(a), $\{v_y\}$ is mapped to $\{v_z\}$ by subtracting with $V_{DD}/2$ then taking absolute or rectification before re-scaling (amplifying) by a factor of two as described by (1).

$$\{v_z\} = 2\left|\{v_y\} - \left(\frac{V_{DD}}{2}\right)\right| \quad (1)$$

This 1-bit sub-ranging/rectifying/re-scaling process can be recursively repeated for QPSK (Figure 3(b)), 8-PSK or *m*-PSK demodulation where 2, 3 or $log_2(m)$ sub-ranging/re-scaling stages are needed. The phase control (1) for $\{v_z\}$ can be modified for *m*-PSK demodulation using $n(= log_2(m))$ stages of sub-ranging/re-scaling as (2).

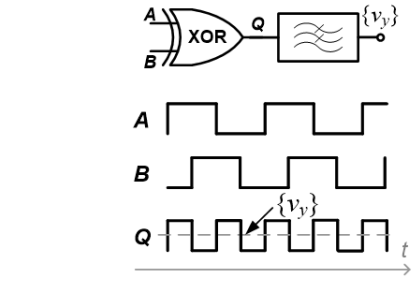
$$\{v_{y(j+1)}\} = 2\left|\{v_{y(j)}\} - \left(\frac{V_{DD}}{2}\right)\right|, \quad j = 1,2 \ldots, n \quad (2)$$

where the last stage renders. Extension to an *m*-PSK demodulator with n $(=log_2(m))$ stages of 1-bit sub-ranging/re-scaling.

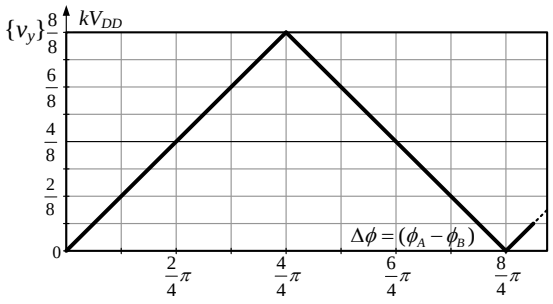
$$VCO_{in} = \{v_z\} = \{v_{y(n)}\} = 2\left|\{v_{y(n-1)}\} - \left(\frac{V_{DD}}{2}\right)\right| \quad (3)$$

It is important to note that other alternate signal processing methods for the phase control process are also possible as long as they can provide correct transformation from $\{v_y\}$ to $\{v_z\}$. Moreover, because the phase controller still preserves the PLL's loop dynamic, if the carrier frequency changes, the phase controller would automatically set the voltage $\{v_z\}$ (and VCO_{in}) to the new value to attain frequency tracking as shown by the inclining arrows in Figure 3(a) and 3(b). In this way, the frequency tuning can be achieved for this *m*-PSK demodulator similar to the conventional PLL technique. Time-domain signaling of the phase control is also illustrated in Figure 3(c) for QPSK demodulation (in practice, there will be a high-frequency signal component embedded in $\{v_y\}$ where it cannot be completely removed by the lowpass filter).

The phase control operations with a 1-bit sub-ranging/re-scaling process can be conceptually implemented with ideal building blocks as shown in Figure 4(a) for BPSK and QPSK demodulation. The demodulator in Figure 4(b) is the extended version for *m*-PSK demodulation where multi-bit sub-ranging/re-scaling phase controller comprises $log_2(m)$ stages of the 1-bit sub-ranging step. It is also important to note that the digital data bits b_0, b_1,…, $b_{log_2(m)-1}$can be directly retrieved from the comparator's output inside the individual sub-ranging stage.



(a)



(b)

Figure 2. An XOR gate's properties (a) a timing diagram (b) an average output voltage vs the input phase difference

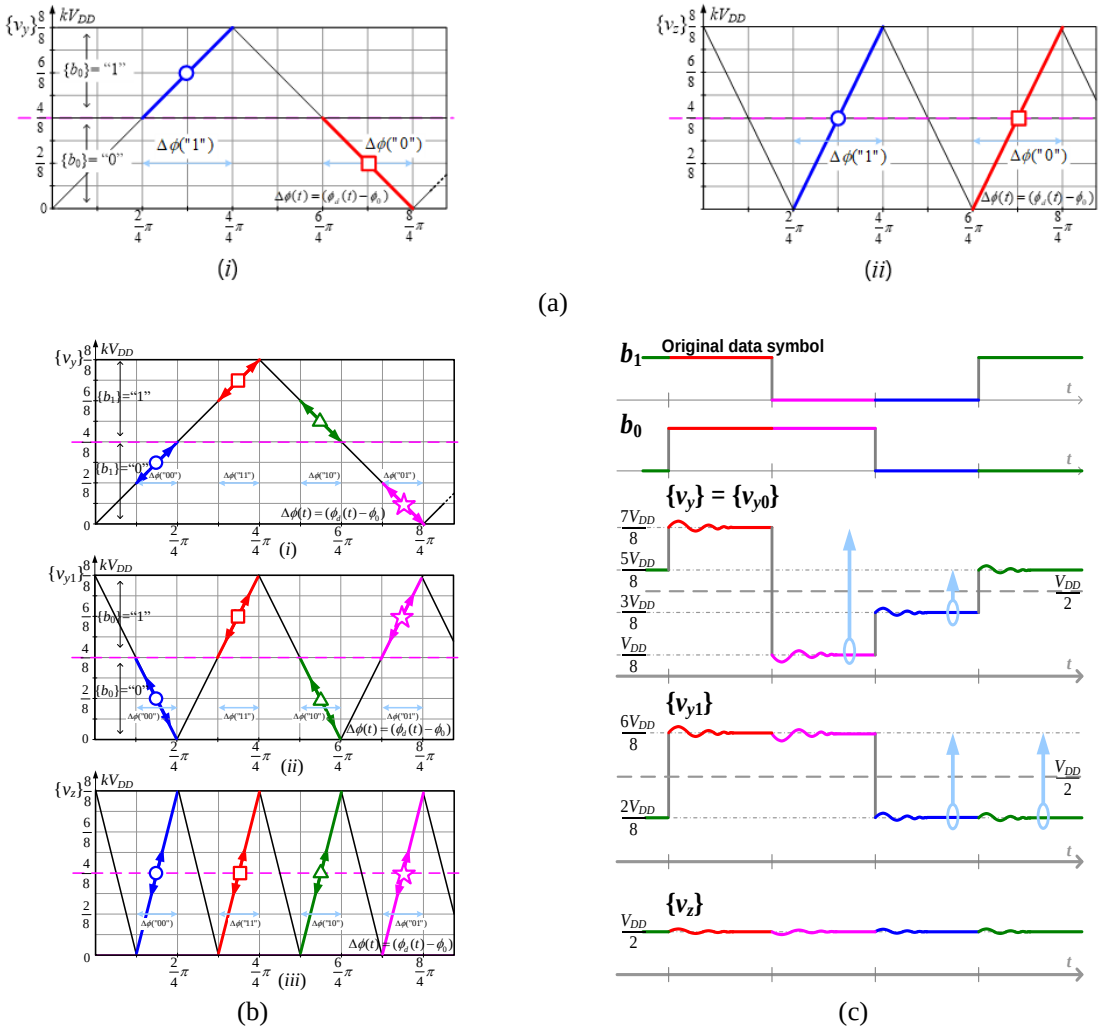


Figure 3. A sub-ranging/rectifying/re-scaling signal diagram for phase control, the voltage $\{v_z\}$ is applied to VCO_{in} as in Figure 1(a), for (a) BPSK, (b) QPSK, and (c) time-domain signaling for QPSK phase control of (b)

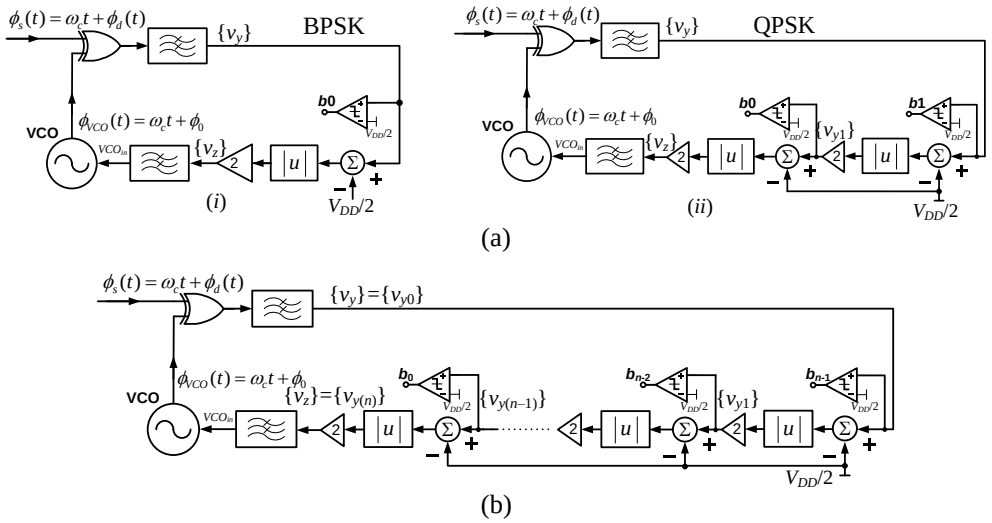


Figure 4. A conceptual PLL-based BPSK, QPSK, *m*-PSK demodulators employing a single-phase VCO (a) BPSK (*i*) and QPSK (*ii*) demodulators employing a "sub-ranging/rescaling" process for phase control (b) Extension to an m-PSK demodulator with n (= log_2(m)) stages of 1-bit sub-ranging/re-scaling

4. BUILDING BLOCKS AND DESIGN CONSIDERATIONS

The important circuit building blocks of the proposed BPSK and QPSK demodulators suitable for discrete implementation are constructed from low-cost and easy-to-find components. This is to test and verify versatility of the proposed demodulation technique. These building blocks are described as follows.

4.1. Single-bit phase-control circuit

A single-bit sub-ranging/rectifying/re-scaling process required for the demodulator's phase-control operation in Figure 3 and Figure 4 can be achieved by the circuit shown in Figure 5. If an ideal op-amp is assumed, the circuit in Figure 5 with k=2 can realize the relation in (1). The first two op-amps comprise a full-wave rectifier around a voltage of $V_{DD}/2$. The third op-amp performs a voltage scaling with a factor k, for the case of the proposed demodulator in Figure 4, k=2.

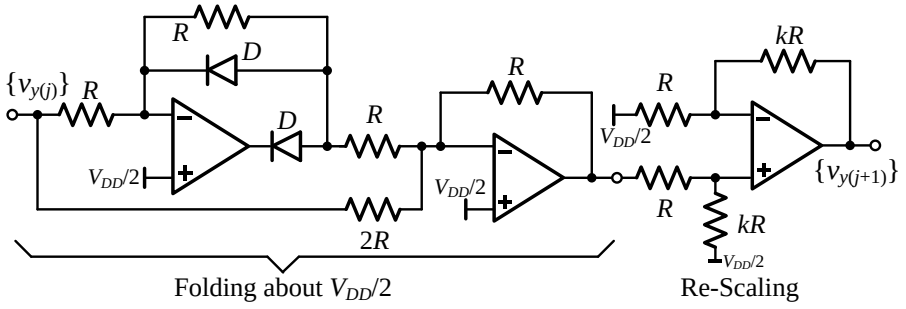


Figure 5. A 1-bit rectifying/re-scaling circuit is based on an op-amp-based precision full-wave rectifier and a difference amplifier where k=2 for Figure 4

4.2. Phase Detector and voltage-controlled oscillator

An Exclusive-OR (XOR) gate (employed as a phase detector) and a voltage-controlled oscillator (VCO) are both taken from a CD4046 integrated circuit [24] for verification purpose. Under a 5-V single supply, the VCO is designed to oscillate at a 100 kHz center frequency. The VCO possesses the minimum/maximum frequencies of 50 kHz/150 kHz. The VCO constant, K_{VCO} has been measured to be 180 krad/s.

4.3. Demodulator loop design consideration

A practical BPSK demodulator circuit example (realizing the system in Figure 4(a(i))) is displayed in Figure 6 with details of the 1-bit sub-ranging/re-scaling circuit and two lag-lead filters. A comparator used to recover a data bit comes from an LM339 IC [25] while the three op-amps are taken from LM324 [26]. The two lag-lead filters essentially perform lowpass filtering as well as provide a compensation zero to help stabilize the loop. Here, the BPSK demodulator in Figure 6 is considered as a design example and the open-loop transfer function $T_{OL}(s)$ is given by (4).

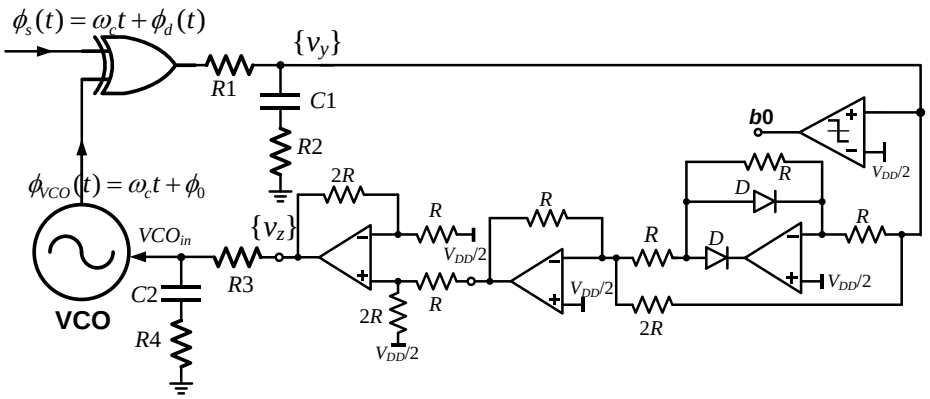
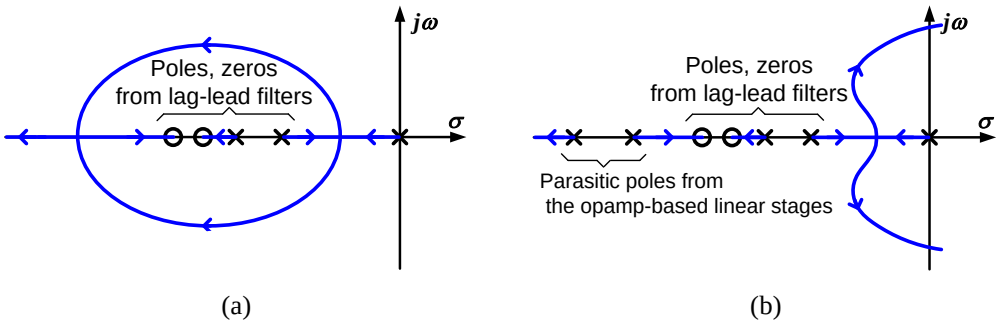


Figure 6. A BPSK demodulator with a 1-bit sub-ranging/re-scaling circuit and two lag-lead filters

$$T_{OL}(s) = K_{PD} \underbrace{\left(\frac{1+sR_2C_1}{1+s(R_1+R_2)C_1}\right)}_{1^{st}\text{ lag-lead filter}} G_{sbrscl}(s) \underbrace{\left(\frac{R_D(1+sR_4C_2)}{1+s(R_3+R_4)C_2}\right)}_{2^{nd}\text{ lag-lead filter}} \frac{K_{VCO}}{s} \quad (4)$$

where the phase detector constant $K_{PD}=V_{DD}/\pi$ for an XOR-gate and $G_{sbrscl}(s)$ represents the transfer function of the op-amp-based precision rectifying/re-scaling circuit of Figure 5. The conceptual root locus design of this BPSK demodulator is illustrated in Figure 7(a). It shows two pole-zero pairs from the two lag-lead filters added to the original pole at the origin associated with the VCO, i.e., $G_{sbrscl}(s)$ contains neither pole nor zero. It is fairly obvious that the presence of two zeros bring the closed-loop poles away from $j\omega$ axis making the loop fairly stable. However, if the non-dominant parasitic poles coming from the op-amp-based circuits are considered as shown in Figure 7(b) where the loop stability deteriorates. In such case, the demodulator loop has to be carefully designed to ensure that the loop is stable and locking can be attained correctly.



(a) (b)

Figure 7. The conceptual BPSK demodulator design with a root locus (a) only with dominant poles and zeros and (b) also with parasitic poles from op-amp-based linear stages

5. EXPERIMENTAL VERIFICATION

The BPSK and QPSK modulation as well as a 2^{16}–1 pseudo-random symbol generator has been implemented with a FPGA platform (Xilink Zybo zynq 7000). A carrier frequency of 100 kHz has been used for both BPSK and QPSK modulation. The demodulator prototypes operate under a 5 V single supply whose PCB is depicted in Figure 8(a). The measurement results are as follows.

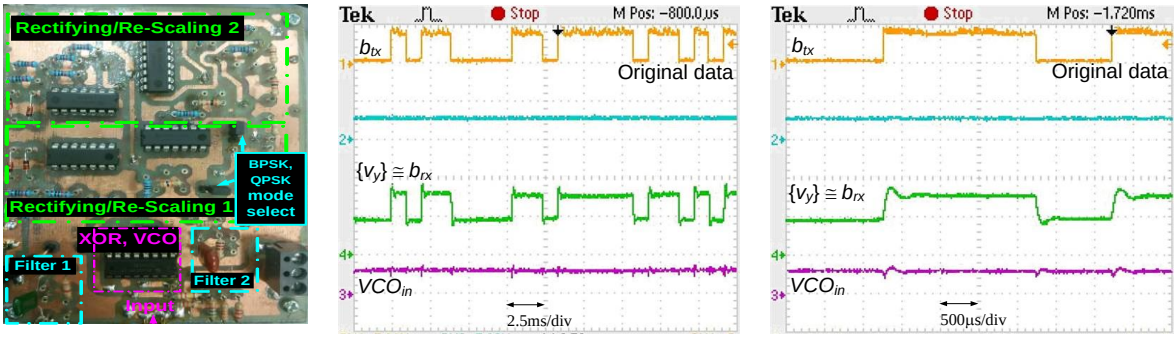
5.1. BPSK demodulator

BPSK demodulation and bit recovery is illustrated in Figures 8(b), 8(c). The digital bit has been correctly recovered when the locked condition has been successfully attained. Noting that the proposed demodulators do not resolve a phase ambiguity issue, the in-phase condition in Figure 8(b) between the recovered bit b_{rx} and the original data bit b_{tx} occurs coincidentally making it easier for demonstration purpose. It can be seen that $\{v_y\}$ shows two distinguished levels according to the original data bits. This $\{v_y\}$ is then passed on to the band-limited voltage comparator which consequently renders the recovered data bit b_{rx}. Figure 8(c) displays the closed-up of Figure 8(b) demonstrating how the phase controller (the rectifying and re-scaling circuit) operates on the filter's output after the XOR gate, $\{v_y\}$ which produces a fairly constant VCO_{in}. A slight disturbance of VCO_{in} can also be observed at the bit transition moments. The BPSK demodulator's capture range is between 70 kHz and 110 kHz. It achieves the maximum bit rate *(=symbol rate*) of 20 kbps.

5.2. QPSK demodulator

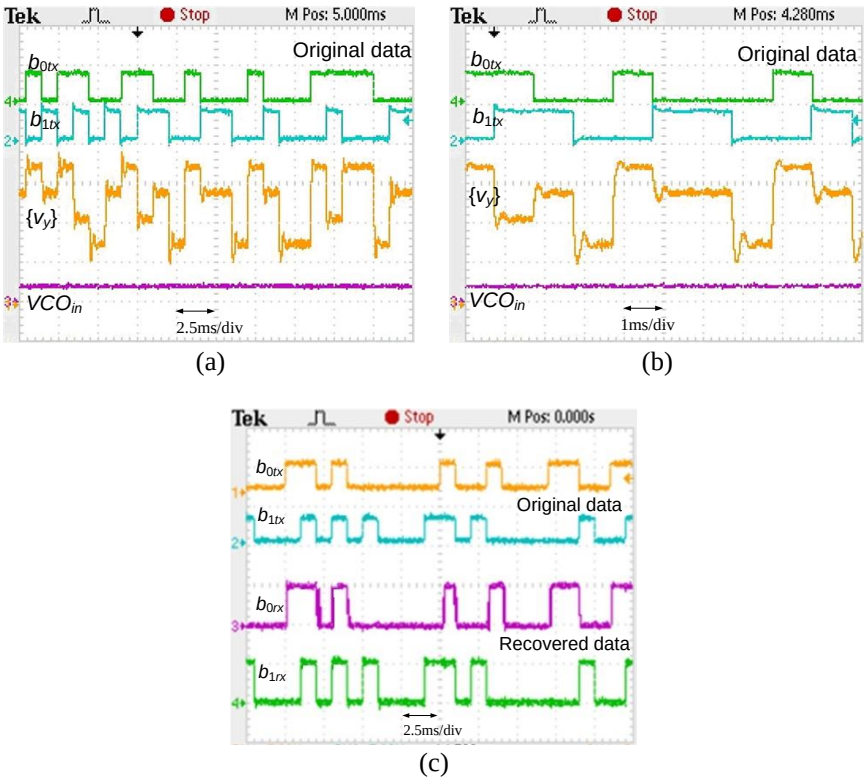
Under a lock condition inside the QPSK demodulator, Figure 9(a) shows the signal $\{v_y\}$ at the XOR gate filter's output possessing four different voltage levels which uniquely correspond to the original 2-bit data symbols $b_{tx1}b_{tx0}$ as previously predicted in Figure 3(c). The VCO_{in} level with small disturbance is also displayed in the figure. The closed-up of the similar measurement is also shown in Figure 9(b) where $\{v_y\}$ clearly illustrates the loop transient dynamic with obvious overshooting and ringing with a natural frequency. Two digital data bits $b_{rx1}b_{rx0}$ can be successfully recovered as compared to the original bits $b_{tx1}b_{tx0}$ in Figure 9(c). The QPSK demodulator can capture the incoming modulated signal with a carrier frequency from 75 to 103 kHz. The loop can perform demodulation at the maximum symbol rate of 10 ksymbol/s (=20 kbps).

An *SER* measurement has been carried out by comparing the recovered symbol to its transmitted counterpart using appropriate data re-timing and sampling by the second FPGA platform. The online symbol-error counting algorithm has also taken into account the phase ambiguity issue. The BPSK's *SER* is practically equal to the bit-error rate (*BER*), i.e. $BER=SER/\log_2(m)$ with $m=2$ for BPSK. This simple formula can be applied to the QPSK and m-PSK for $m \geq 4$ if Gray code is employed and signal-to-noise ratio (SNR) is sufficiently high [1]. The *SER* has been measured against the modulated signal's *SNRs*, i.e., the power ratio between the BPSK or QPSK modulated signal P_S and the noise P_n at the input of the demodulator. Plots of the measured *SER* vs E_b/N_o have been obtained as shown in Figure 10 using the relation $SNR_S=\log_2(m)E_b/(N_0/2)$ as suggested in [1, 3]. These measured *SER*s from the BPSK and QPSK demodulators are also compared with the calculations from ideal situations when using the conventional distance-decision analysis on the BPSK, QPSK constellation diagrams [1, 2, 3]. Note that to test the demodulator versatility under server symbol transition, gray code has not been exercised for these measurements.



(a) (b) (c)

Figure 8. BPSK demodulator's measured results: (a) PCB, (b) bit recovery at 1 kbps, (c) the closed-up of (b)



(a) (b) (c)

Figure 9. QPSK demodulator's measured results at 1 ksymbol/s (a) $\{v_y\}$ as compared to the transmitted bits, (b) the close-up of (a), and (c) recovered bits b_{rx1}, b_{rx0} compared to the original data b_{tx1}, b_{tx0}

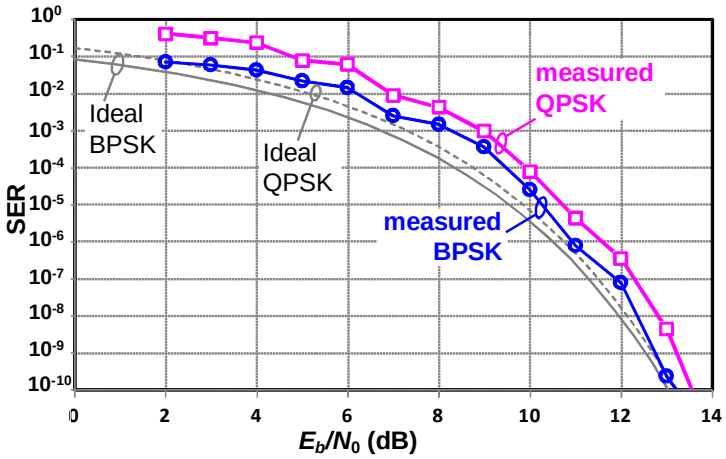


Figure 10. Measured SER versus Eb/N0 from the BPSK and QPSK demodulators

6. CONCLUSION

Coherent BPSK and QPSK demodulators using a single-phase VCO inside a single-loop PLL-based structure has been reported. The demodulators are truly modular and they employ a simple phase controller that operates on the average voltage from an XOR-gate phase detector's output. The demodulator prototype has been implemented with low-cost, easy-to-find discrete components. The measurements have successfully verified the proposed *m*-PSK demodulation concept.

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