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Energy saving through load balancing of 3-wire loads

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ABSTRACT

In this paper, static var compensators (SVCs) and many load compensation techniques are reviewed. A continuously and linearly controlled compensating susceptance is devised from a switched capacitor bank and a switched reactor bank. The switched capacitor bank is built of four binary weighted thyristor switched capacitors, while the switched reactor bank is built of three binary weighted thyristor switched reactors. Although few switched capacitors and reactor are used, their binary weighted values beside their control scheme make them respond as a continuously and linearly controlled reactive device in capacitive and inductive modes of operation. A load balancing system is constructed of three identical devised compensating susceptances connected in delta-form. It is designed for balancing an 11 kV 50 Hz distribution station. The proposed system is designed and tested on PSpice which is a computer program equivalent in performance to real hardware design. The simulation results of the proposed system have showed significant treatment of severe imbalance conditions.

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1. INTRODUCTION

Traditional static var compensators (SVCs) and synchronous static compensators (STATCOMs) are the basic means used for power quality purposes [1]–[25]. Traditional static var compensators are represented by thyristor-controlled reactor (TCR), thyristor switched reactor (TSR), and thyristor switched capacitor (TSC). Static compensators are represented by power converter based static var compensators and STATCOMs. Load compensation and power factor correction systems have great impact in transmission losses reduction and energy saving in power generation stations [1]–[25] . The minimization of current harmonics released from the operation of TSC-TCR based SVC into the distribution systems at low voltage distribution level was discussed by [1]. In the proposed study, intelligent control was used to determine the TCR triggering signals required for minimal harmonic injection. A three-phase STATCOM based compensation system was introduced by [2] for compensating unbalanced voltage and current. By choosing appropriate control schemes, the proposed compensation system can achieve voltage regulation in addition to certain limit of current balancing and power factor correction.

In [3], a new type of STATCOM designed for high-power applications was proposed for fully compensating the imbalanced and disfigured nonlinear loads operating in large-current medium-voltage grids. Hagiwara *et al.* [4] introduced an application using a modular multilevel cascade converter on basis of the single-delta bridge-cells to synchronized STATCOM, especially for the control of negative-sequence var. A DSTATCOM in [5] was capable of real-time compensation for unbalanced loads in 4-wire distribution systems. The method of symmetrical components was exploited for devising the controlling scheme for this

DSTATCOM. In [6] a new configuration of harmonic suppression circuitries was proposed to a TCR, which promoted it to respond linearly to reactive current demand without harmonic association.

A simulation package depending on LABVIEW was developed by [7] for reduction of energy loss purposes. The work in [8] discussed safe operation of grid-connected power converters with related to peak current limitation as well as maximum permissible fluctuations of the direct current (DC) voltage. Balancing of load currents can be accomplished via correction process of power factor and compensation of load active current components [9]. Many researches exploited converter-based static compensators for harmonic reduction, voltage regulation, and current compensation [9]–[13], [22]. Compensators built of separate susceptances in star and delta configurations showed more compensation flexibility than traditional lumped systems represented by DSTATCOMs [9], [15]–[20]. A 3-phase load current balancing scheme in a transmission system having distributed static compensators connected in series and using the method of variable quadrature voltage injection was proposed by [14]. This topology either exhibits capacitive or inductive impedance into the alternating current (AC) grid lines for current balancing purposes. The works in [21], introduced reactances for 3-phase load compensation. The reactances connected in star form were used for compensating reactive currents, whereas those connected in delta for were exploited for balancing the active components of line currents. Active filters were introduced in [23] for the purposes of treating harmonic current components associating nonlinear loads, whereas in [24], a shunt active filter was provided to a single-phase converter to achieve significant reduction in harmonic current components. A DSTATCOM was introduced in [25] for power quality purposes. It was suggested to enhance the improvement of power factor, voltage regulation, current balancing, and harmonic minimization.

In this paper, a continuously and linearly controlled SVC is devised from a new configuration of TSCs and TSRs. The new configuration is built of a binary weighted switched capacitor bank (BWSCB) and a binary weighted switched reactor bank (BWSRB). Even though the devised SVC is built of limited number of stepping response TSCs and TSRs, it shows a performance of a continuously and linearly controlled compensating susceptance. A static compensator is built of three identical compensating susceptances connected in delta-form. It is designed for load currents balancing for an 11 kV 50 Hz distribution station. The station involves five feeders. The average line current drawn from this station varies in the range of 1,200 to 1,300 A (rms values) depending on the daily loading conditions. A 30% unbalance in line currents is permissible there.

2. THE ADOPTED LOAD BALANCING STRATEGY

Figure 1 shows the layout of the balancing mechanism of an ungrounded load fed by a balanced three phase voltage. B_{SAB}, B_{SBC}, and B_{SCA} are the compensating susceptances of the static compensator power circuit. I_{SA}, I_{SB}, and I_{SC} are the static compensator line currents. The AC power system phase voltages V_A, V_B, and V_C can be given by (1), (2), and (3).

$$V_A = V \tag{1}$$

$$V_B = V e^{j\frac{-2\pi}{3}} \tag{2}$$

$$V_B = V e^{j\frac{-4\pi}{3}} \tag{3}$$

where, V is the rms magnitude of each phase voltage. The line currents of the unbalanced three-phase load can be given by (4), (5), dan (6).

$$I_{LA} = |I_{LA}|\angle\phi_{LA} = |I_{LA}|\cos\phi_{LA} + |I_{LA}|\sin\phi_{LA}\, e^{j\frac{\pi}{2}} \tag{4}$$

$$I_{LB} = |I_{LB}|\angle\phi_{LB} = |I_{LB}|\cos\phi_{LB}\, e^{j\frac{-2\pi}{3}} + |I_{LB}|\sin\phi_{LB}\, e^{j\frac{-\pi}{6}} \tag{5}$$

$$I_{LC} = |I_{LC}|\angle\phi_{LC} = |I_{LC}|\cos\phi_{LC}\, e^{j\frac{-4\pi}{3}} + |I_{LC}|\sin\phi_{LC}\, e^{j\frac{-5\pi}{6}} \tag{6}$$

where, φ_{LA}, φ_{LB}, and φ_{LC} are the power factor angles of phases A, B, and C respectively. $|I_{LA}|$, $|I_{LB}|$, and $|I_{LC}|$, are the absolute rms values of I_{LA}, I_{LB}, and I_{LC} respectively. The active current components of line currents are in phase with their corresponding phase voltages, while reactive current components lead them by π/2. Similarly, the static compensator rms currents I_{SA}, I_{SB}, and I_{SC} can be expressed in terms of their active and reactive current components as (7), (8), and (9).

$$I_{SA} = \sqrt{3}V\cos\left(\frac{\pi}{3}\right)(B_{SCA} - B_{SAB}) + \sqrt{3}V\sin\left(\frac{\pi}{3}\right)(B_{SAB} + B_{SCA})e^{j\frac{\pi}{2}} \quad (7)$$

$$I_{SB} = \sqrt{3}V\cos\left(\frac{\pi}{3}\right)(B_{SAB} - B_{SBC})e^{j\frac{-2\pi}{3}} + \sqrt{3}V\sin\left(\frac{\pi}{3}\right)(B_{SBC} + B_{SAB})e^{j\frac{-\pi}{6}} \quad (8)$$

$$I_{SC} = \sqrt{3}V\cos\left(\frac{\pi}{3}\right)(B_{SBC} - B_{SCA})e^{j\frac{-4\pi}{3}} + \sqrt{3}V\sin\left(\frac{\pi}{3}\right)(B_{SCA} + B_{SBC})e^{j\frac{-5\pi}{6}} \quad (9)$$

I_A, I_B, and I_C are the rms line currents of the AC source. According to the main objective of this research, these currents should be balanced and active. Consequently, they can be given by (10), (11), (12).

$$I_A = I \quad (10)$$

$$I_B = Ie^{j\frac{-2\pi}{3}} \quad (11)$$

$$I_C = Ie^{j\frac{-4\pi}{3}} \quad (12)$$

where, I is the rms magnitude of each line current. The active power P_L supplied to the unbalanced load can be given by (13) and (14).

$$P_L = V(|I_{LA}|\cos\phi_{LA} + |I_{LB}|\cos\phi_{LB} + |I_{LC}|\cos\phi_{LC}) \quad (13)$$

The active power P supplied by the AC source can be given by (14).

$$P = 3VI \quad (14)$$

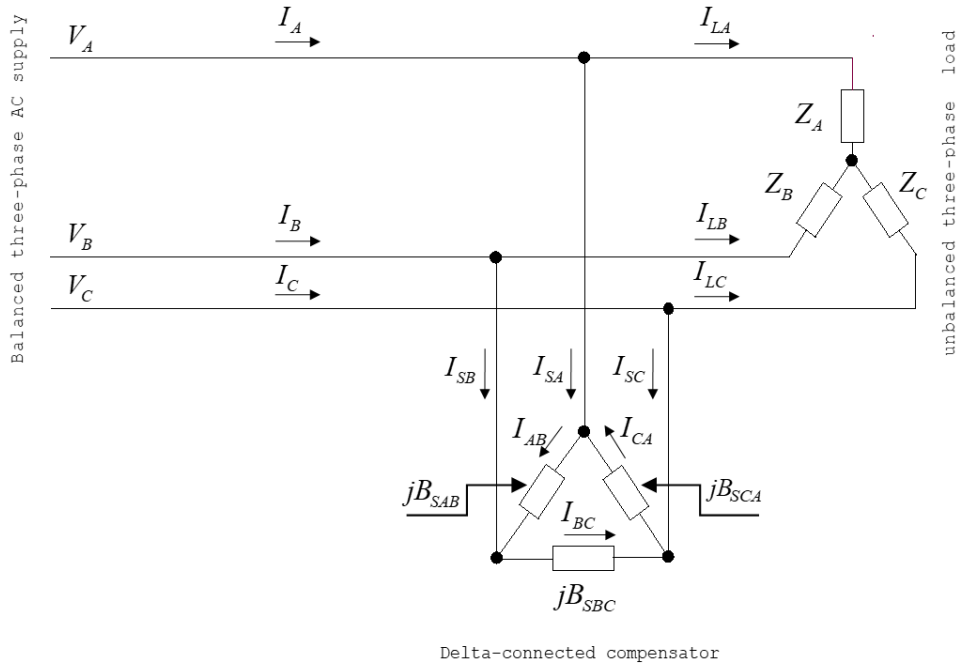

Figure 1. The mechanism of balancing an ungrounded load

The active power supplied by the AC source should be equal to the power consumed by the unbalanced load or in other words:

$$P = 3VI = P_L \quad (15)$$

equating the (15) for I, gives (16).

$$I = \frac{1}{3}(|I_{LA}| \cos \phi_{LA} + |I_{LB}| \cos \phi_{LB} + |I_{LC}| \cos \phi_{LC}) \quad (16)$$

Applying Kirchhoff's current law at nodes A, B, and C on reactive current components of load and compensator currents for obtaining B_{SAB}, B_{SBC}, and B_{SCA} gives

$$B_{SAB} = -\frac{1}{3V}(|I_{LA}| \sin \phi_{LA} + |I_{LB}| \sin \phi_{LB} - |I_{LC}| \sin \phi_{LC}) \quad (17)$$

$$B_{SBC} = -\frac{1}{3V}(|I_{LB}| \sin \phi_{LB} + |I_{LC}| \sin \phi_{LC} - |I_{LA}| \sin \phi_{LA}) \quad (18)$$

$$B_{SCA} = -\frac{1}{3V}(|I_{LC}| \sin \phi_{LC} + |I_{LA}| \sin \phi_{LA} - |I_{LB}| \sin \phi_{LB}) \quad (19)$$

2.1. Layout of the 11 kV 50 Hz BWSCB-BWSRB based SVC

The power circuit of this SVC is shown in Figure 2. It is constructed of the BWSCB represented by the switched capacitors C_1 to C_4 and the BWSRB represented by the switched reactors L_1 to L_3. The inductors L_{C1} to L_{C4} are used as current limiters for the solid-state switching devices of the switched capacitors. The switched capacitor and reactor banks are designed such that,

$$\omega C = 1/\omega L \quad (20)$$

where, ω is the angular frequency of the AC power system voltage V_{ac}. C and L are the basic capacitance and inductance of the BWSCB and BWSRB, respectively.

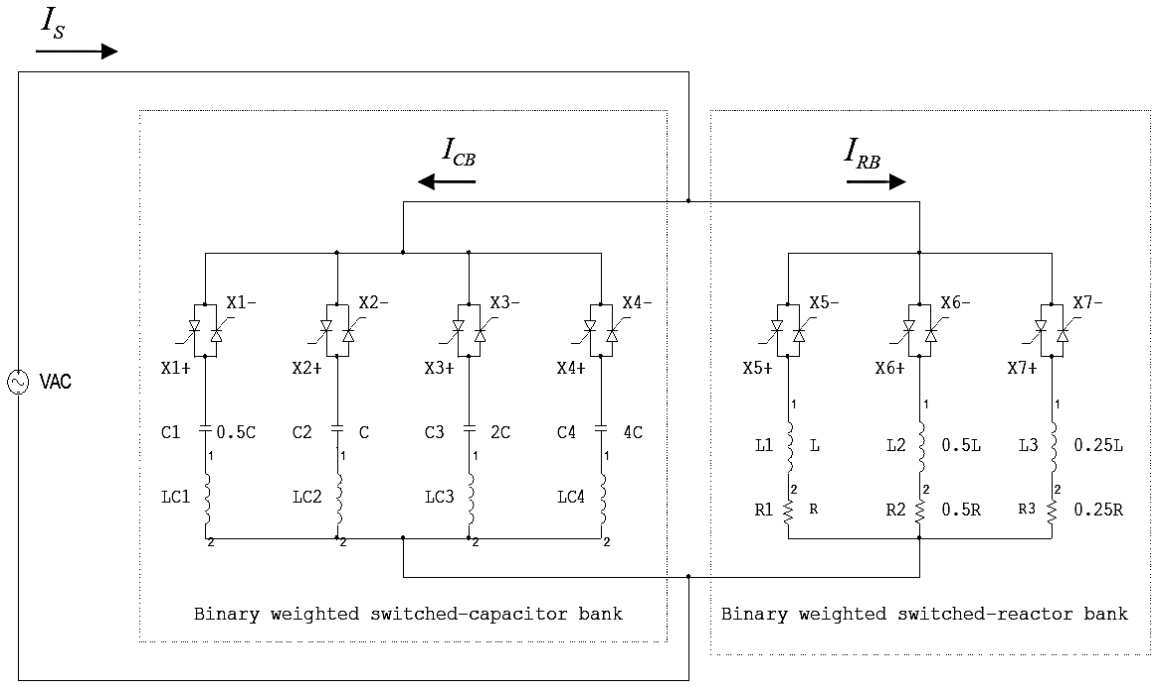

Figure 2. Layout of BWSCB and BWSRB based SVC

This SVC is designed such that its reactive current response to reactive current demand follows the response indicated in Figure 3. The minus sign refers to inductive reactive current. The maximum deviation of BWSCB-BWSRB based SVC current from the required linear reactive current response is within ±0.5I_{BB}. Where, I_{BB} is current magnitude between two adjacent current levels of BWSCB capacitive reactive current response. This current can be expressed as (21).

$$I_{BB} = V_{ac} \frac{\omega C}{2} \quad (21)$$

Since the absolute deviation of the SVC total current from the required linear response is negligible compared to its absolute reactive current rating, the proposed SVC can be considered to some extent as continuously and linearly controlled compensating susceptance. The maximum capacitive and inductive current ratings of this SVC are $15I_{BB}$ and $-14I_{BB}$ respectively.

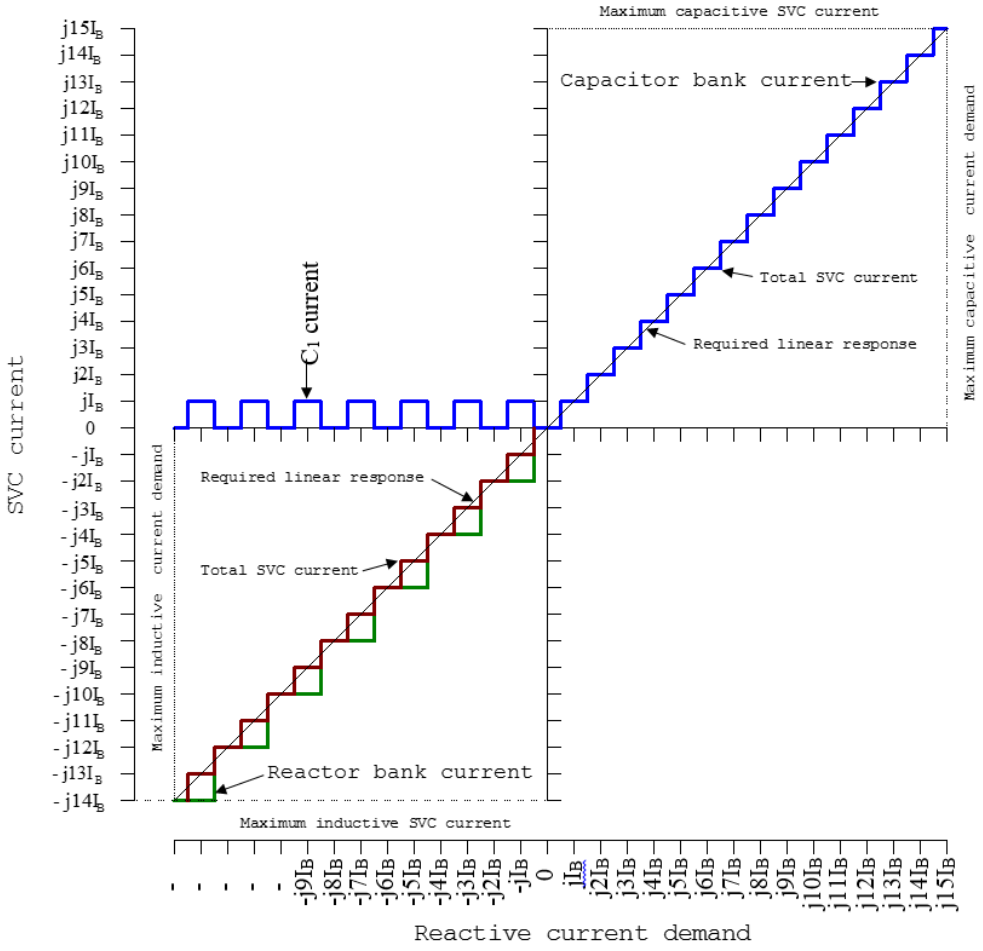

Figure 3. The current of BWSCB-BWSRB based SVC against reactive current demand

The switching status of the binary switched capacitor and reactor banks are shown in Table 1. The table states the variations of the reactive current demand (I_D) from maximum inductive to maximum capacitive. The DATA of this table were exploited to draw Figure 3.

2.2. Circuit design of 11 kV 50 Hz BWSCB-BWSRB based SVC

There are no separate thyristors that can handle a line-to-line voltage of the 11 kV. Therefore, the switching devices X_{1+} to X_{7-} of Figure 2 are built by using arrays of thyristors. Figure 4 shows these arrays. The circuit diagram of the 11 kV 50 Hz BWSCB-BWSRB based SVC is shown in Figure 5. The circuit is designed and built on PSpice. In this circuit, the line-to-line AC voltage is detected by using a potential transformer which is generated as electronic part and saved as a separate library on PSpice. The output of the potential transformer is the voltage signal k_3v_{ac}, which has amplitude of 5 V. Where, v_{ac} represents the instantaneous line to line voltage exerted on the compensator. The controller of this SVC is represented by the electronic part "BINARY SVC CONTROLLING CCT" which is responsible for generating the controlling signals required for the SVC triggering circuit. The triggering circuit of the BWSCB-BWSRB based SVC is represented by the electronic part "TRIGGERING CCT" which is responsible for generating the triggering signals of the thyristor switching arrays X_{1+} to X_{7-}. The thyristor and its driving circuit are merged together in its corresponding switching array. The anti-parallel switching arrays with their driving circuits are represented by the electronic parts "SCR ARR-1IB", "SCR ARR-2IB", "SCR ARR-4IB", and "SCR ARR-8IB".

Table 1. The switching status of switched capacitors and reactors

Reactive current demand (I_D)	Capacitors switching status				Reactors switching status		
	C_1	C_2	C_3	C_4	L_1	L_2	L_3
$-j14I_{BB} \le I_D < -j13.5I_{BB}$	OFF	OFF	OFF	OFF	ON	ON	ON
$-j13.5I_{BB} \le I_D < -j12.5I_{BB}$	ON	OFF	OFF	OFF	ON	ON	ON
$-j12.5I_{BB} \le I_D < -j11.5I_{BB}$	OFF	OFF	OFF	OFF	OFF	ON	ON
$-j11.5I_{BB} \le I_D < -j10.5I_{BB}$	ON	OFF	OFF	OFF	OFF	ON	ON
$-j10.5I_{BB} \le I_D < -j9.5I_{BB}$	OFF	OFF	OFF	OFF	ON	OFF	ON
$-j9.5I_{BB} \le I_D < -j8.5I_{BB}$	ON	OFF	OFF	OFF	ON	OFF	ON
$-j8.5I_{BB} \le I_D < -j7.5I_{BB}$	OFF	OFF	OFF	OFF	OFF	OFF	ON
$-j7.5I_{BB} \le I_D < -j6.5I_{BB}$	ON	OFF	OFF	OFF	OFF	OFF	ON
$-j6.5I_{BB} \le I_D < -j5.5I_{BB}$	OFF	OFF	OFF	OFF	ON	ON	OFF
$-j5.5I_{BB} \le I_D < -j4.5I_{BB}$	ON	OFF	OFF	OFF	ON	ON	OFF
$-j4.5I_{BB} \le I_D < -j3.5I_{BB}$	OFF	OFF	OFF	OFF	OFF	ON	OFF
$-j3.5I_{BB} \le I_D < -j2.5I_{BB}$	ON	OFF	OFF	OFF	OFF	ON	OFF
$-j2.5I_{BB} \le I_D < -j1.5I_{BB}$	OFF	OFF	OFF	OFF	ON	OFF	OFF
$-j1.5I_{BB} \le I_D < -j0.5I_{BB}$	ON	OFF	OFF	OFF	ON	OFF	OFF
$-j0.5I_{BB} \le I_D < 0$	OFF	OFF	OFF	OFF	OFF	OFF	OFF
$0 \le I_D < j0.5I_{BB}$	OFF	OFF	OFF	OFF	OFF	OFF	OFF
$j0.5I_{BB} \le I_D < j1.5I_{BB}$	ON	OFF	OFF	OFF	OFF	OFF	OFF
$j1.5I_{BB} \le I_D < j2.5I_{BB}$	OFF	ON	OFF	OFF	OFF	OFF	OFF
$j2.5I_{BB} \le I_D < j3.5I_{BB}$	ON	ON	OFF	OFF	OFF	OFF	OFF
$j3.5I_{BB} \le I_D < j4.5I_{BB}$	OFF	OFF	ON	OFF	OFF	OFF	OFF
$j4.5I_{BB} \le I_D < j5.5I_{BB}$	ON	OFF	ON	OFF	OFF	OFF	OFF
$j5.5I_{BB} \le I_D < j6.5I_{BB}$	OFF	ON	ON	OFF	OFF	OFF	OFF
$j6.5I_{BB} \le I_D < j7.5I_{BB}$	ON	ON	ON	OFF	OFF	OFF	OFF
$j7.5I_{BB} \le I_D < j8.5I_{BB}$	OFF	OFF	OFF	ON	OFF	OFF	OFF
$j8.5I_{BB} \le I_D < j9.5I_{BB}$	ON	OFF	OFF	ON	OFF	OFF	OFF
$j9.5I_{BB} \le I_D < j10.5I_{BB}$	OFF	ON	OFF	ON	OFF	OFF	OFF
$j10.5I_{BB} \le I_D < j11.5I_{BB}$	ON	ON	OFF	ON	OFF	OFF	OFF
$j11.5I_{BB} \le I_D < j12.5I_{BB}$	OFF	OFF	ON	ON	OFF	OFF	OFF
$j12.5I_{BB} \le I_D < j13.5I_{BB}$	ON	OFF	ON	ON	OFF	OFF	OFF
$j13.5I_{BB} \le I_D < j14.5I_{BB}$	OFF	ON	ON	ON	OFF	OFF	OFF
$j14.5I_{BB} \le I_D < j15I_{BB}$	ON	ON	ON	ON	OFF	OFF	OFF

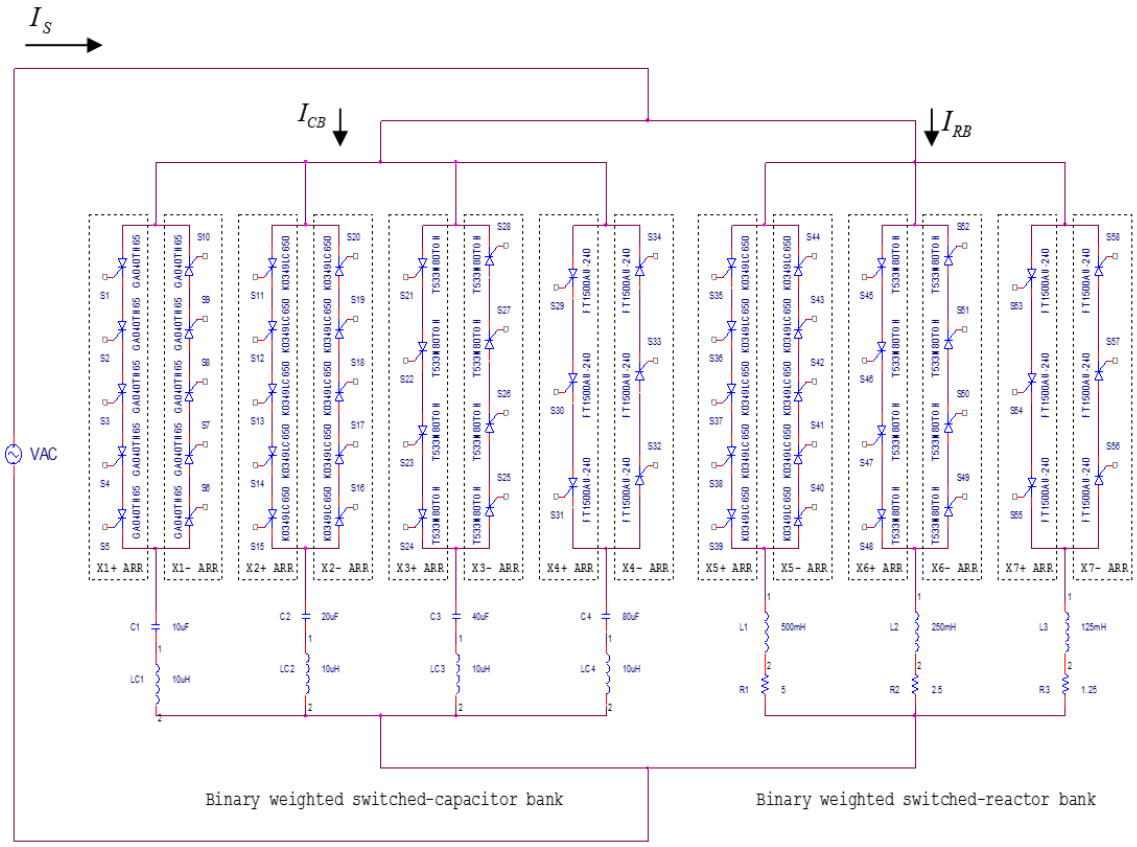

Figure 4. Thyristors arrays of 11 kV 50 Hz BWSCB-BWSRB based SVC

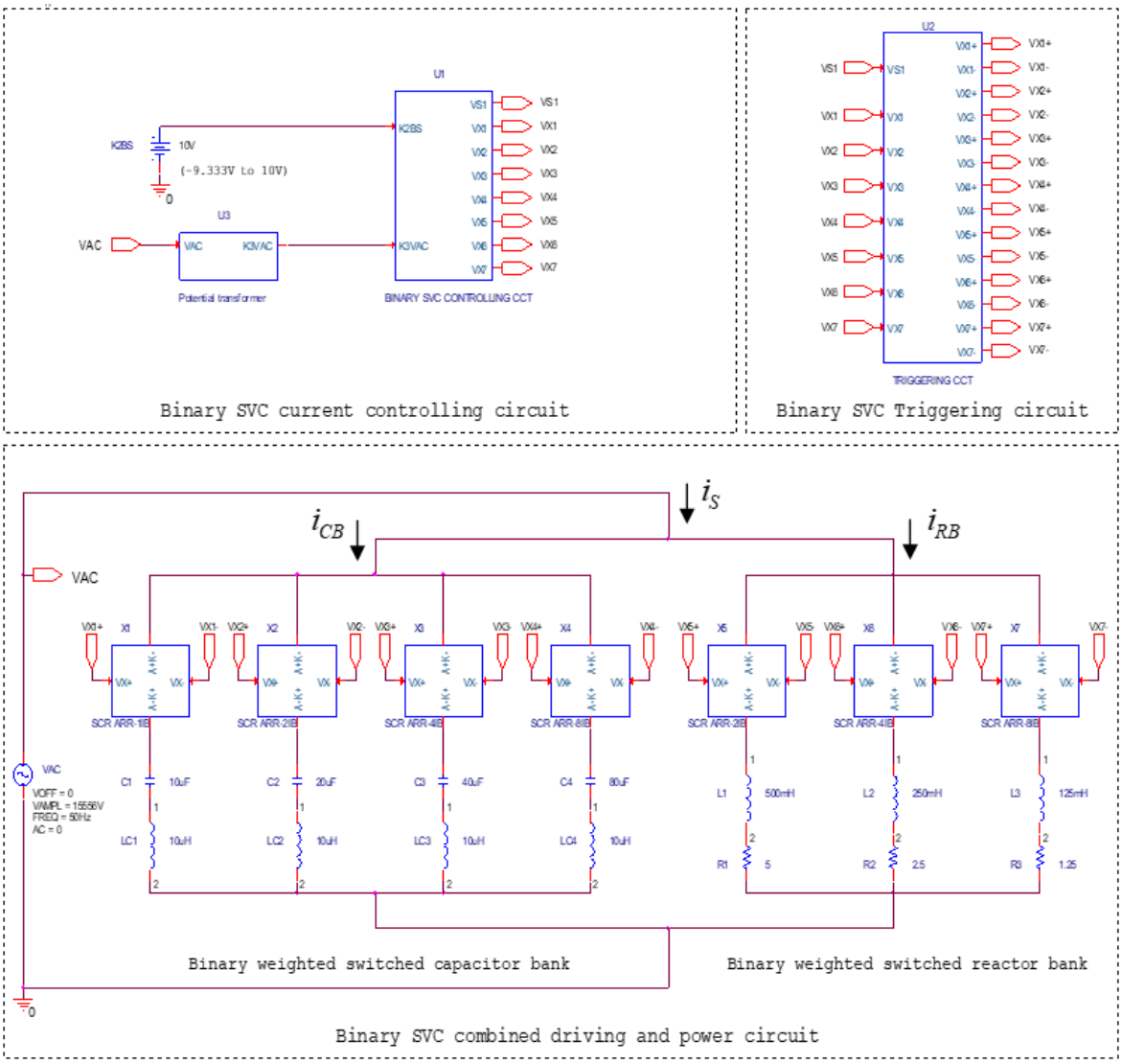

Figure 5. Circuit diagram of 11 kV 50 Hz BWSCB and BWSRB based SVC

2.2.1. Current controller of BWSCB-BWSRB based SVC

The electronic circuit of this current controller is designed such that the reactive current response of the SVC follows the response indicated in Figure 3. The electronic circuit of this controller is shown in Figure 6. In this figure, the DC voltage source k_2B_S represents an analogue signal proportional to the reactive current demand. This signal varies in the range of -9.333 to +10 V. Its negative sign denotes inductive reactive current demand, while its positive sign is related to capacitive reactive current demand. In this controlling circuit, two 8-bit analogue-to-digital converters (8-bit ADCs) are employed to control the capacitor and the reactor banks. The 8-bit ADC digital outputs are all logic one, when its analogue input V_{ADC} is 10 V and are all logic zero when its input is zero. Logics zero and one correspond to voltage levels of zero and +5 V respectively. The two ADCs input voltages V_{ADC1} and V_{ADC2} are related to k_2B_S by (22) and (23).

$$V_{ADC1} = 0.9375k_2B_S + 0.3125 \quad (22)$$

$$V_{ADC2} = -0.9375k_2B_S + 0.3125 \quad (23)$$

Only the four most significant digits of each ADC are employed in the SVC current controller. This makes each 8-bit ADC equivalent to 4-bit ADC. The first 4-bit ADC output digits are D_{1C}, D_{2C}, D_{3C}, and D_{4C}, while the second 4-bit output digits are D_{1L}, D_{2L}, D_{3L}, and D_{4L}. Note that D_{4C} and D_{4L} are representing the most significant digits of the first and the second equivalent 4-bit ADCs respectively. The controlling signals V_{X1} to V_{X7} are the triggering signals of X_1 to X_7 respectively. These signals are defined by (24)–(30).

$$V_{X1} = D_{1C} + D_{1L} \quad (24)$$

$$V_{X2} = D_{2C} \quad (25)$$

$$V_{X3} = D_{3C} \quad (26)$$

$$V_{X4} = D_{4C} \quad (27)$$

$$V_{X5} = D_{1L} \oplus D_{2L} \quad (28)$$

$$V_{X6} = (D_{1L} \oplus D_{3L})D_{2L} + \overline{D_{2L}}D_{3L} \quad (29)$$

$$V_{X7} = D_{1L}D_{2L}D_{3L}\overline{D_{4L}} + D_{4L} \quad (30)$$

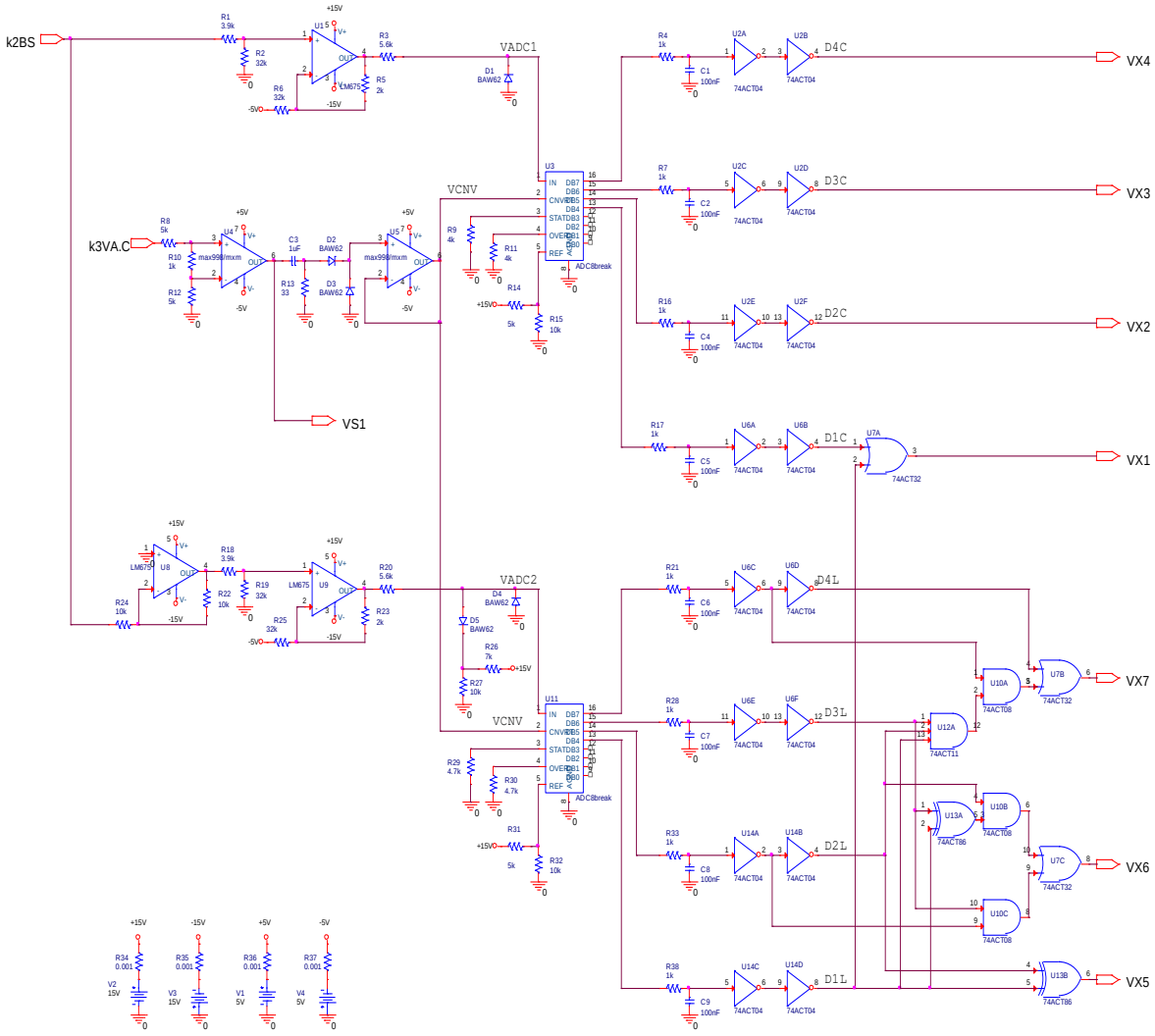

Figure 6. The current controller of BWSCB and BWSRB based SVC

2.2.2. Triggering circuit of BWSCB-BWSRB based SVC

Figure 7 shows the BWSCB and BWSRB based SVC triggering circuit. The controlling signals of this circuit are the output signals of the current controller which are represented by V_{S1} and V_{X1}-V_{X7}. V_{S1} is a rectangular waveform denoting the zero crossing points and polarity of $k_3 v_{A.C}$. It is delayed by a time of 5 ms which corresponds to lagging phase shift angle of π/2. The resulting signal is designated by V_{S2}. The latter

signal is processed digitally with V_{X1}-V_{X7} as shown in Figure 7 for generating the triggering signals of the positive and negative half-cycles of thyristors arrays depicted in Figure 4.

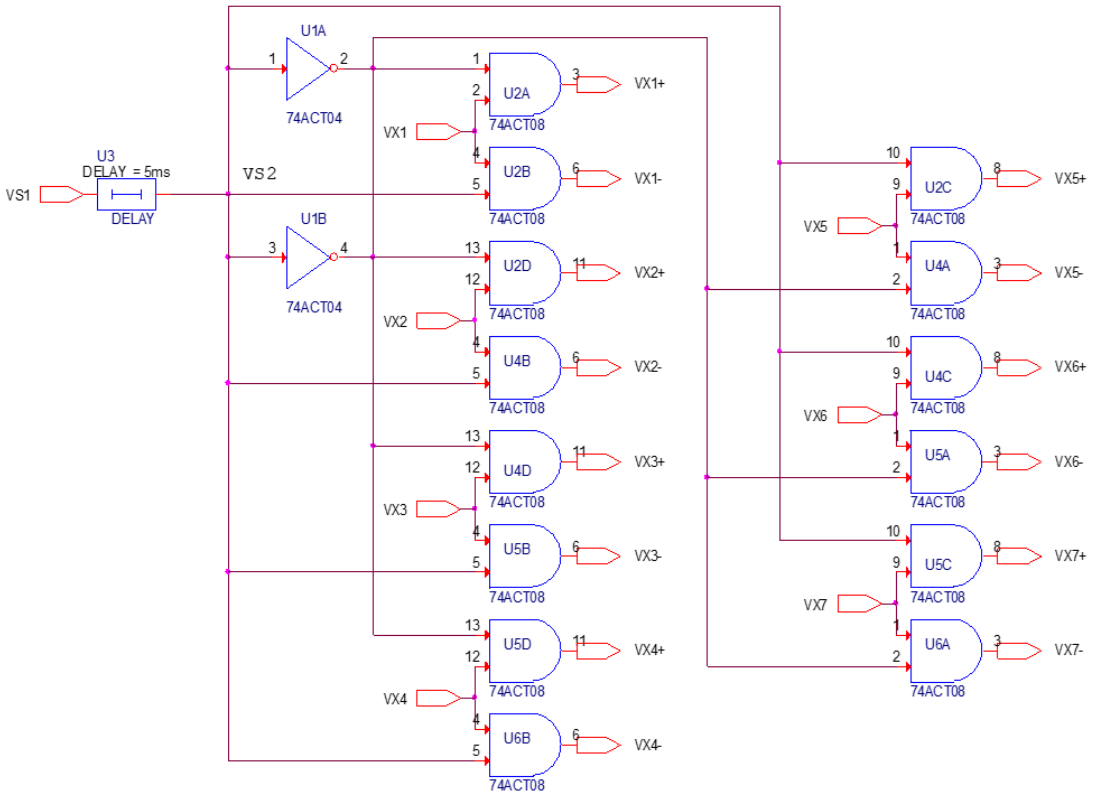

Figure 7. The triggering circuit of the BWSCB and BWSRB based SVC

2.2.3. Combined driving and power circuit of BWSCB-BWSRB based SVC

There are four types of thyristor arrays in Figure 4. Each one of them has a different current rating. Merging the positive and negative half-cycles switching devices in each branch into a single device and combining them with their corresponding driving circuits, result in seven bipolar switching devices X_1 to X_7 as shown in Figure 5.

Since X_1 has a current rating of I_{BB}, its device type is referred to as SCR ARR-1IB. X_2 and X_5 have the same current rating of $2I_{BB}$, thus their device type is referred to as SCR ARR-2IB. Subsequently, the device types of X_3, X_6 and X_4, X_7 are referred to as SCR ARR-4IB and SCR ARR-8IB respectively. Figure 8 shows the exact circuit diagram of the bipolar switching device X_1 which is of the type SCR ARR-1IB. In this figure, each thyristor is shunted by its own snubber circuit. The rms current I_S of 11 kV 50 Hz BWSCB and BWSRB based SVC can be expressed in terms of the switched capacitor bank rms current I_{CB} and the switched reactor bank rms current I_{RB} as (31).

$$I_S = I_{CB} + I_{RB} \tag{31}$$

I_{CB} and I_{RB} can be expressed in terms of controlling signals V_{X1} to V_{X7} as (32), (33).

$$I_{CB} = \frac{jI_{BB}}{5}(V_{X1} + 2V_{X2} + 4V_{X3} + 8V_{X4}) \tag{32}$$

$$I_{RB} = -\frac{jI_{BB}}{5}(2V_{X5} + 4V_{X6} + 8V_{X7}) \tag{33}$$

where, I_{BB} is defined in (21). Substituting (32) and (33) into (31) yields.

$$I_S = \frac{jI_{BB}}{5}(V_{X1} + 2V_{X2} + 4V_{X3} + 8V_{X4} - 2V_{X5} - 4V_{X6} - 8V_{X7}) \tag{34}$$

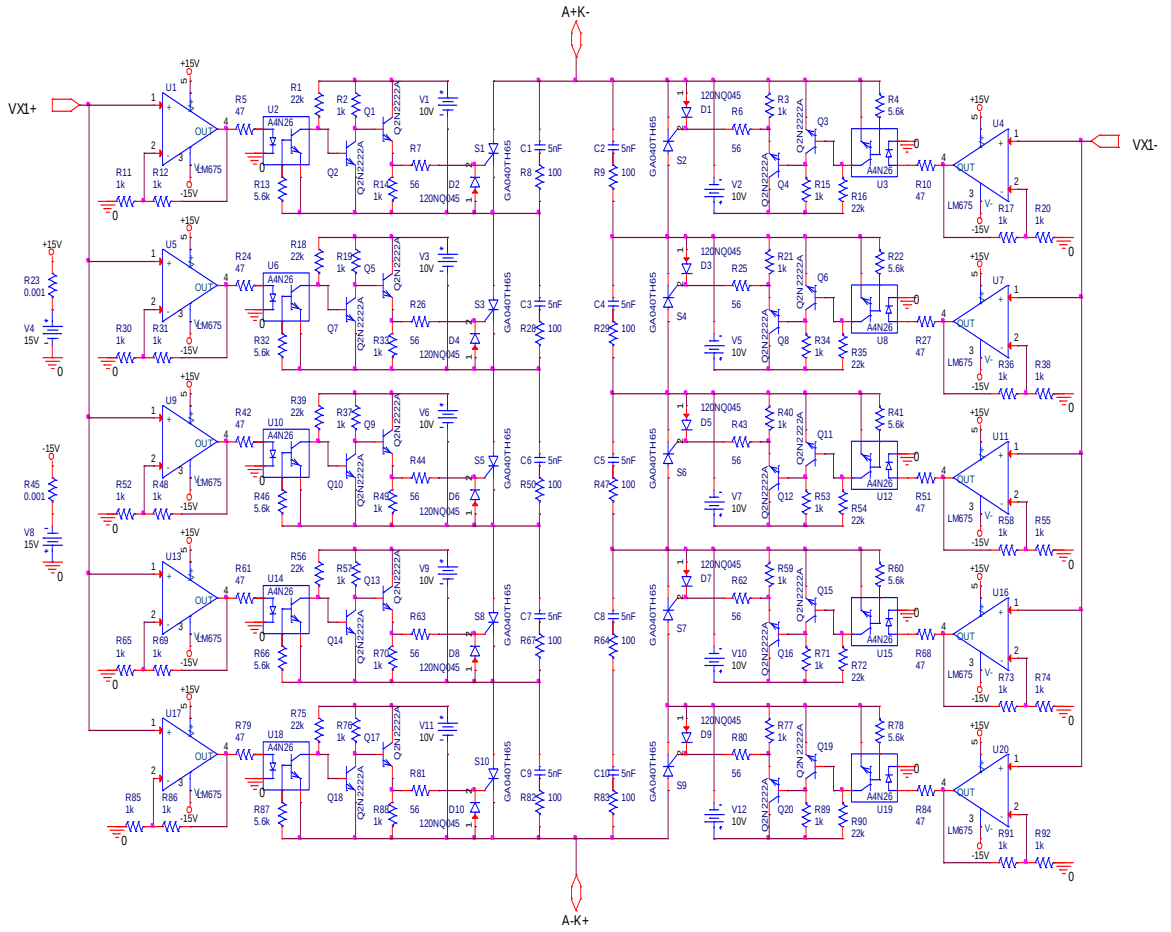

Figure 8. Combined driving and power circuit of X_1 anti-parallel thyristor array

2.3. Circuit design of the proposed 11 kV 50 Hz load currents balancing system for ungrounded loads

This system is designed such that it can correct to unity the 0.707 lagging power of a balanced three-phase load of 1,270 A (rms value). Such a strategy makes it possible for the load currents balancing system to involve the unbalance cases of about 30% of the line current in the 11 kV 50 Hz power distribution station. Figure 9 shows the load currents balancing system for ungrounded loads in 11 kV 50 Hz distribution network. The distribution station is represented here by an unbalanced ungrounded three-phase load. The power circuit of this compensating system is constructed of three combined driving and power circuits connected in delta-form. Each combined driving and power circuit is the same as that of the 11 kV 50 Hz BWSCB and BWSRB based SVC depicted in Figure 5. This load currents balancing system can be imagined as three 11 kV 50 Hz continuously and linearly controlled harmonic-free compensating susceptances connected in delta-form. The instantaneous load currents i_{LA}, i_{LB}, and i_{LC} are detected using three identical current transformers. The outputs of these current transforms are converted to the analogue voltages $k_1 i_{LA}$, $k_1 i_{LB}$, and $k_1 i_{LC}$. These voltages are processed by the computation circuit in the three-phase controlling circuit to produce three analogue signals proportional to the required compensating susceptances B_{SAB}, B_{SBC}, and B_{SCA}. These signals are $k_2 B_{SAB}$, $k_2 B_{SBC}$, and $k_2 B_{SCA}$. The computation circuit is represented by the electronic part "COMPUTATION CCT". The three-phase controlling circuit comprises in addition to the computation circuit, three current controlling circuits represented by the electronic parts "BINARY SVC CONTROLLING CCT", three triggering circuits represented by the electronic parts "TRIGGERING CCT", and the AC voltages detection circuit represented by the electronic part "AC VOLTAGES DETECTION CCT" which produces low level analogue signals proportional to the phase and line voltages.

The controlling and triggering circuits are as the same as those depicted in Figures 6 and 7, respectively. The currents i_{SA}, i_{SB}, and i_{SC} represent the instantaneous compensating currents of the static compensator built of the delta-connected BWSCB and BWSRB based SVCs. The currents i_A, i_B, and i_C represent the instantaneous line currents of the AC power system network. These currents are intended to be balanced and pure active. The AC voltage's detection circuit is shown in Figure 10. The potential

transformers are represented by three potential dividers. The potential dividers output signals k_3v_A, k_3v_B, and k_3v_C are proportional to power system instantaneous phase voltages v_A, v_B, and v_C respectively. According to this circuit, k_3 is computed as 3.2×10^{-4}. These voltages signals are processed through the difference amplifiers to obtain the voltage signals k_3v_{AB}, k_3v_{BC}, and k_3v_{CA} which are proportional to the AC power system instantaneous line voltages v_{AB}, v_{BC}, and v_{CA} respectively. These groups of voltage signals are necessary for both triggering and computation circuits.

The computation circuit is shown in Figure 11. In this circuit, the voltage signals k_1i_{LA}, k_1i_{LB}, and k_1i_{LC} are sampled at the negative slope zero-crossing points of k_3v_A, k_3v_B, and k_3v_C respectively. The sampled voltage signals are $-k_1\sqrt{2}|I_{LA}|sin\varphi_{LA}$, $-k_1\sqrt{2}|I_{LB}|sin\varphi_{LB}$, and $-k_1\sqrt{2}|I_{LC}|sin\varphi_{LC}$. The above compensating susceptances can be expressed in terms of the instantaneous line currents i_{LA}, i_{LB}, and i_{LC} and the latter signals are processed in summing amplifiers to compute k_2B_{SAB}, k_2B_{SBC}, and k_2B_{SCA} which are analogue voltages proportional to the required compensating susceptances. The maximum positive value of each analogue voltage of k_2B_{SAB}, k_2B_{SBC}, and k_2B_{SCA} is 10 V. The maximum magnitude of the capacitive susceptance is 733 A/15,556 V=0.0471 S which corresponds to a capacitive reactive current demand of 733 A (peak value). Consequently, the constant k_2 is computed by dividing the analogue voltage k_2B_S which corresponds to 10 V by the value of the compensating susceptance B_S as: $k_2=k_2B_S/B_S=10$ V/0.0471 S=212.22 VΩ.

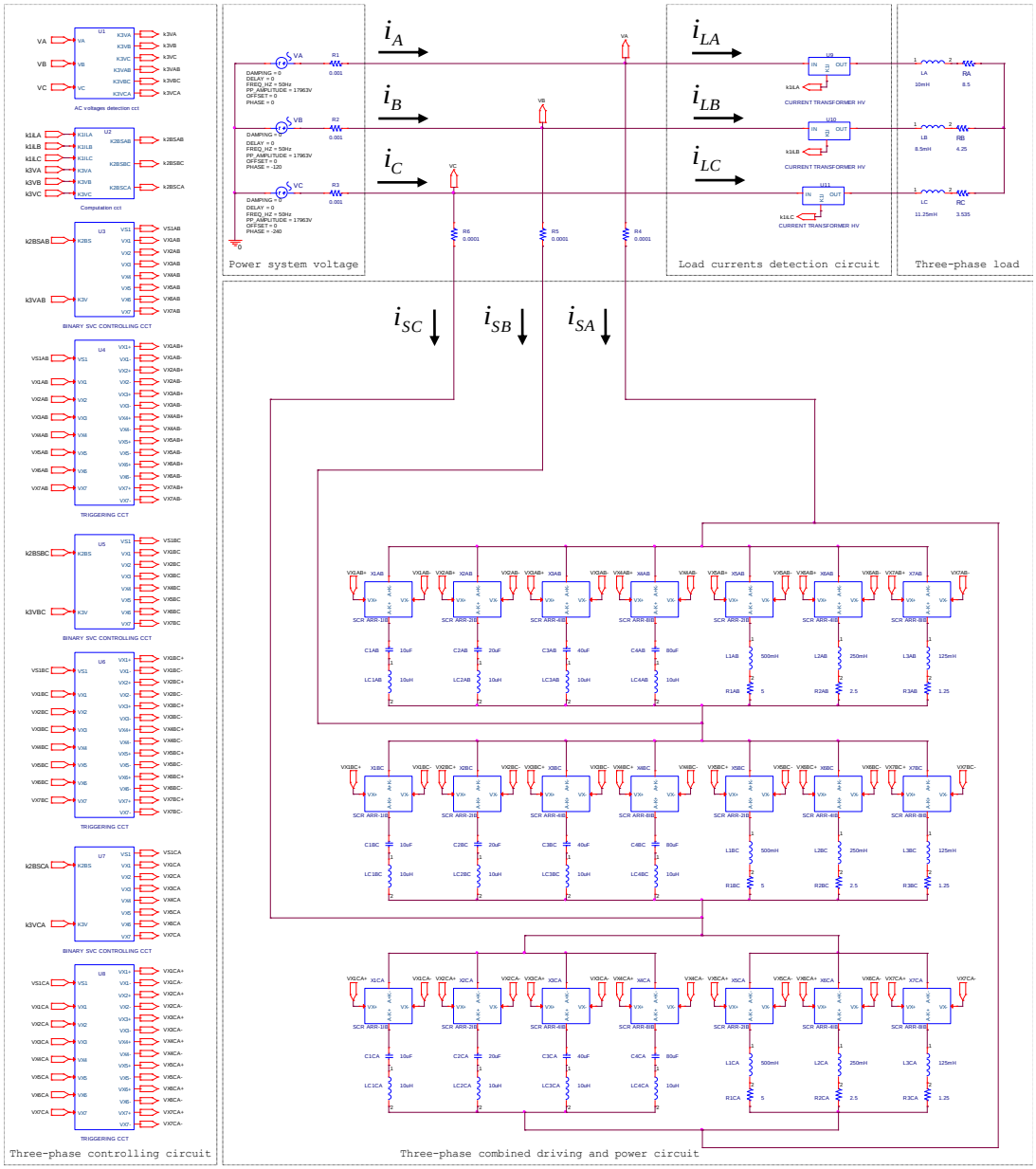

Figure 9. Circuit design of the proposed 11 kV 50 Hz load currents balancing system for ungrounded loads

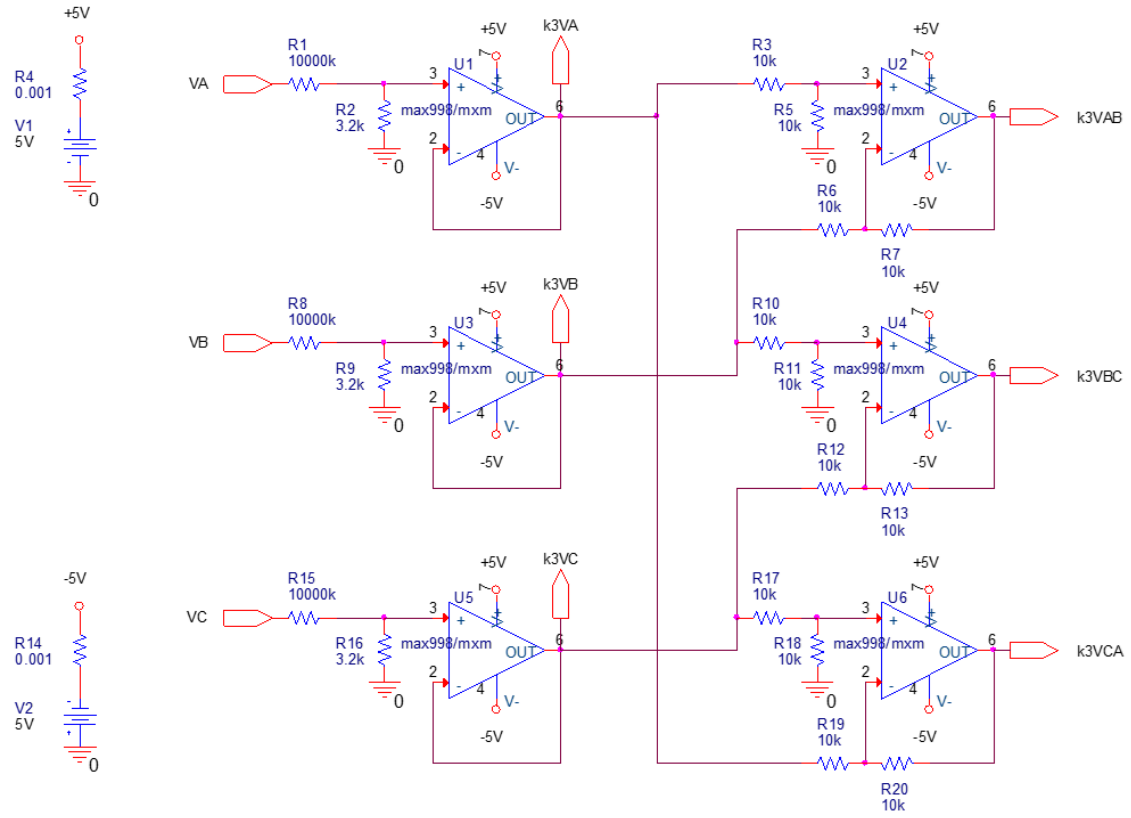

Figure 10. AC voltages detection circuit of 11 kV 50 Hz load currents balancing system

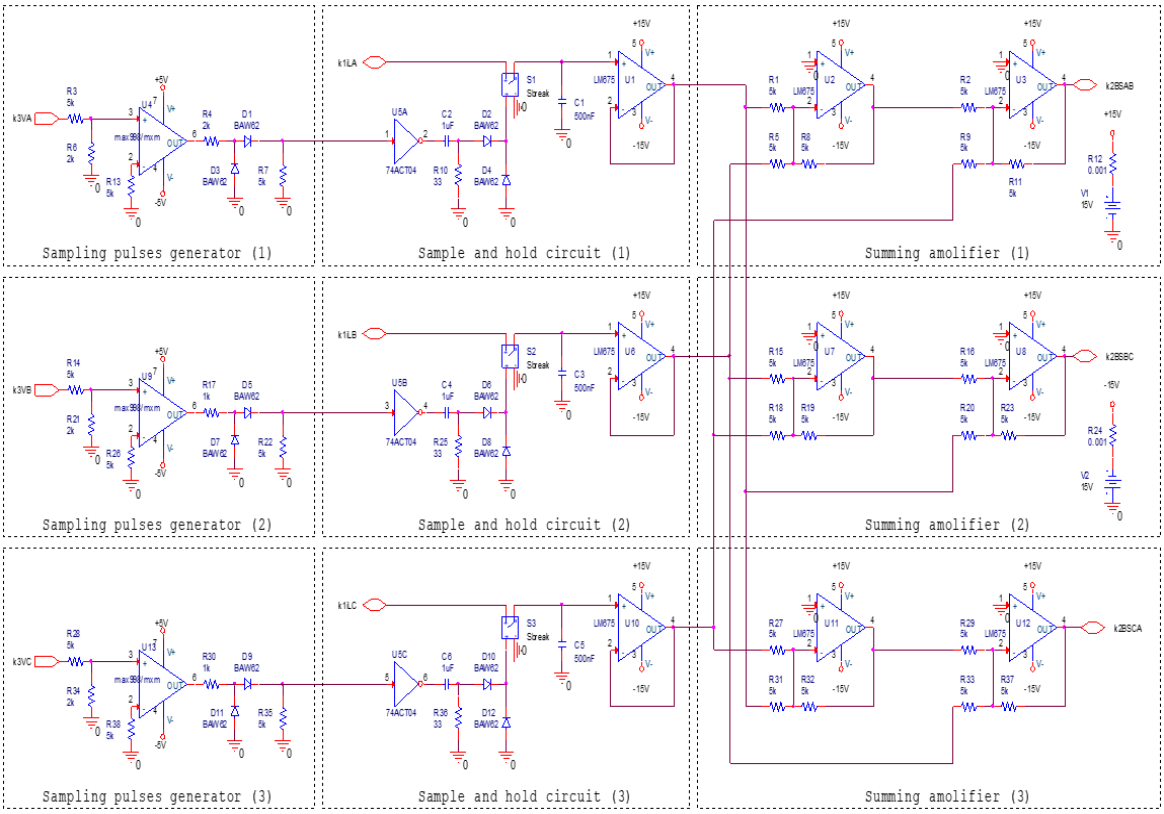

Figure 11. Computation circuit of 11 kV 50 Hz load currents balancing system

3. RESULTS AND DISCUSSION

Many tests were carried out to demonstrate the linearity and the control continuity of the compensator. Figure 12 shows the variations of the compensator reactive current as the reactive current demand varies from maximum inductive to maximum capacitive. The minus sign indicates the reactive current is inductive. The deviations of the actual response from the linear continuous response are negligible compared to the compensator reactive current rating, thus it can be said that the compensator current to some extent is linearly and continuously controlled.

The 11 kV 50 Hz BWSCB and BWSRB based SVC is characterized by fast response to the abrupt changes in reactive demand. This property is demonstrated in Figure 13. The figure shows the SVC treatment to a sudden change in reactive current demand from maximum capacitive to maximum inductive.

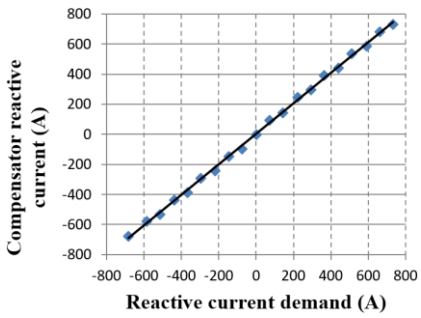

Figure 12. The reactive current of the 11 kV 50 Hz BWSCB and BWSRB based SVC against reactive current demand

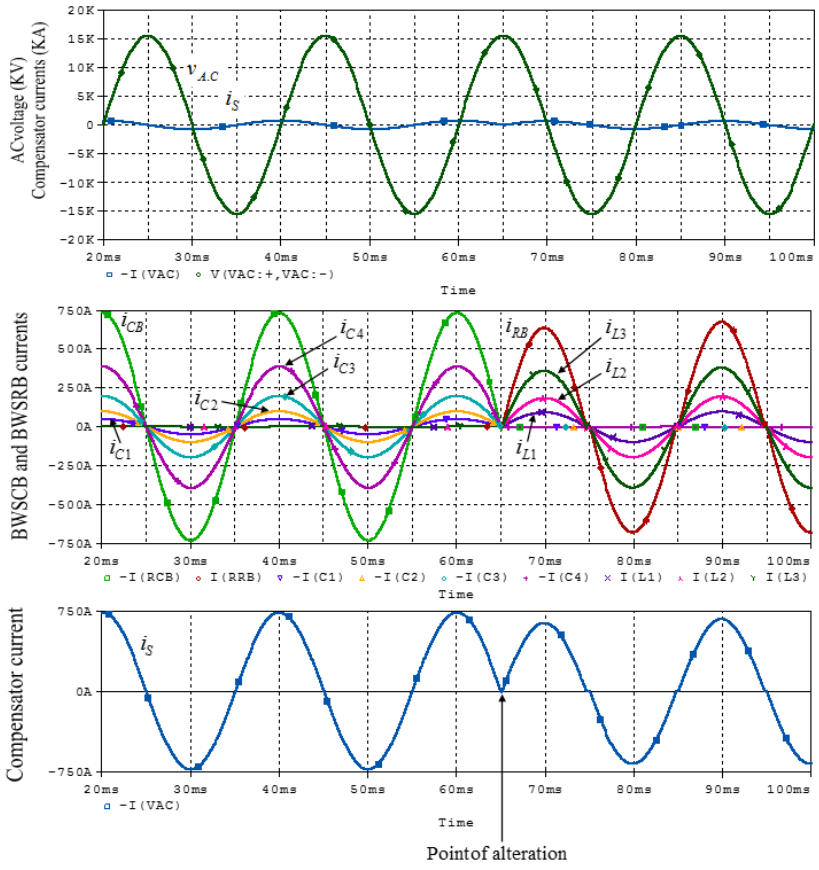

Figure 13. Treatment of the 11 kV 50 Hz BWSCB and BWSRB based SVC to sudden change in reactive current demand from maximum capacitive to maximum inductive. The change was at t=60 msec and the transition time was 5 msec

The load currents balancing systems shown in Figure 9 was tested on PSpice at different loading conditions to investigate its effectiveness and reliability during its treatment to unbalance cases and somewhat poor power factor loads. The system is designed for load currents balancing for an 11 kV 50 Hz distribution station in Iraq. The station involves five feeders. The average line current drawn from this station varies in the range of 1,200 to 1,300 A (rms values) depending on the daily loading conditions. Figure 14 shows the unity power factor correction of a balanced ungrounded load of 1,796 A (peak value) at 0.707 lagging power factor handled by the 11 kV 50 Hz load balancing system using BWSCB and BWSRB based SVCs.

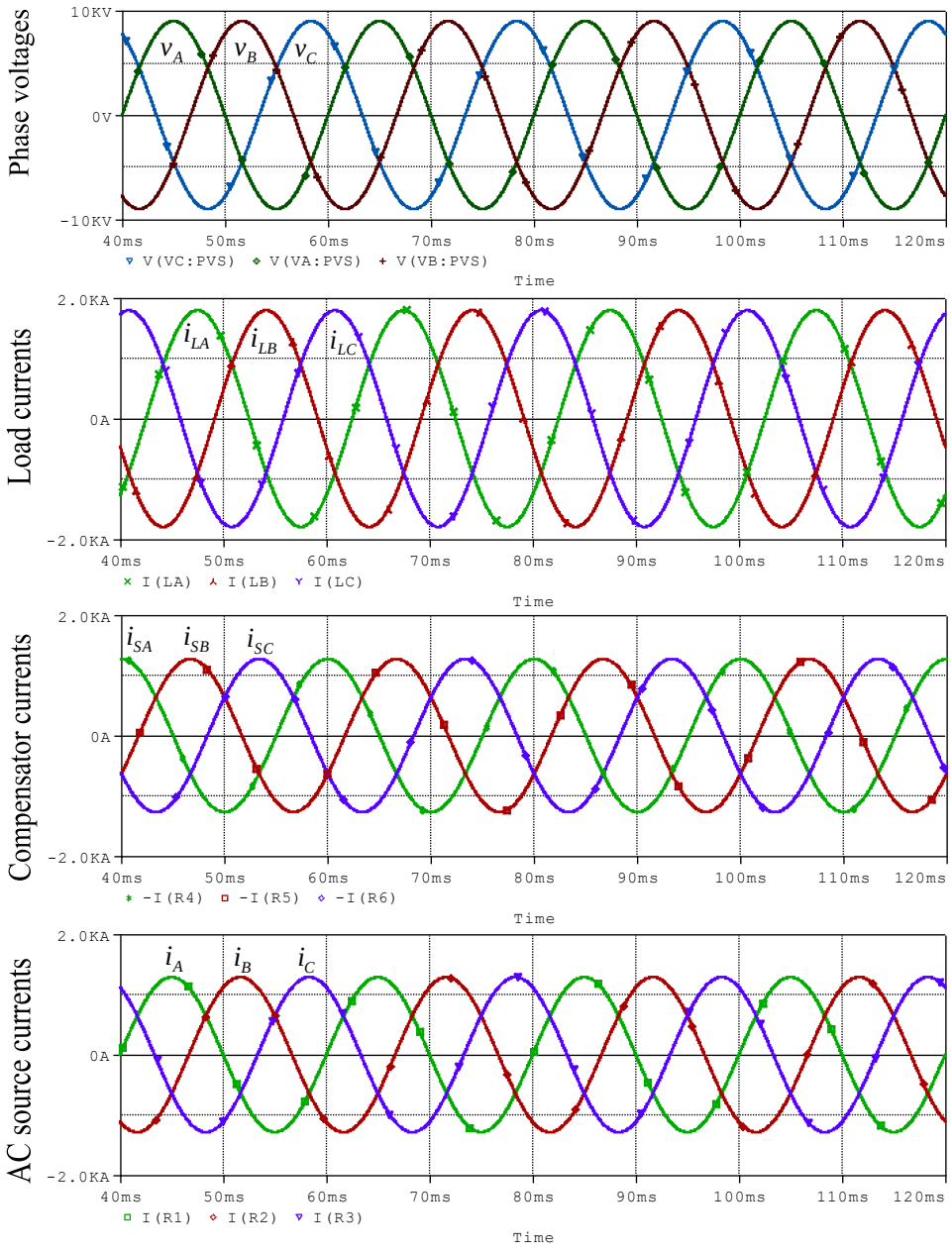

Figure 14. Unity power factor correction of a balanced ungrounded load of 1796 A (peak value) at 0.707 lagging power factor handled by the proposed balancing system

Figure 15 shows the treatment of a certain moderate unbalance. This unbalance case is within the distribution station rated current. The compensation process had resulted in balanced pure active currents i_A, i_B, and i_C drawn from the balanced three-phase AC source.

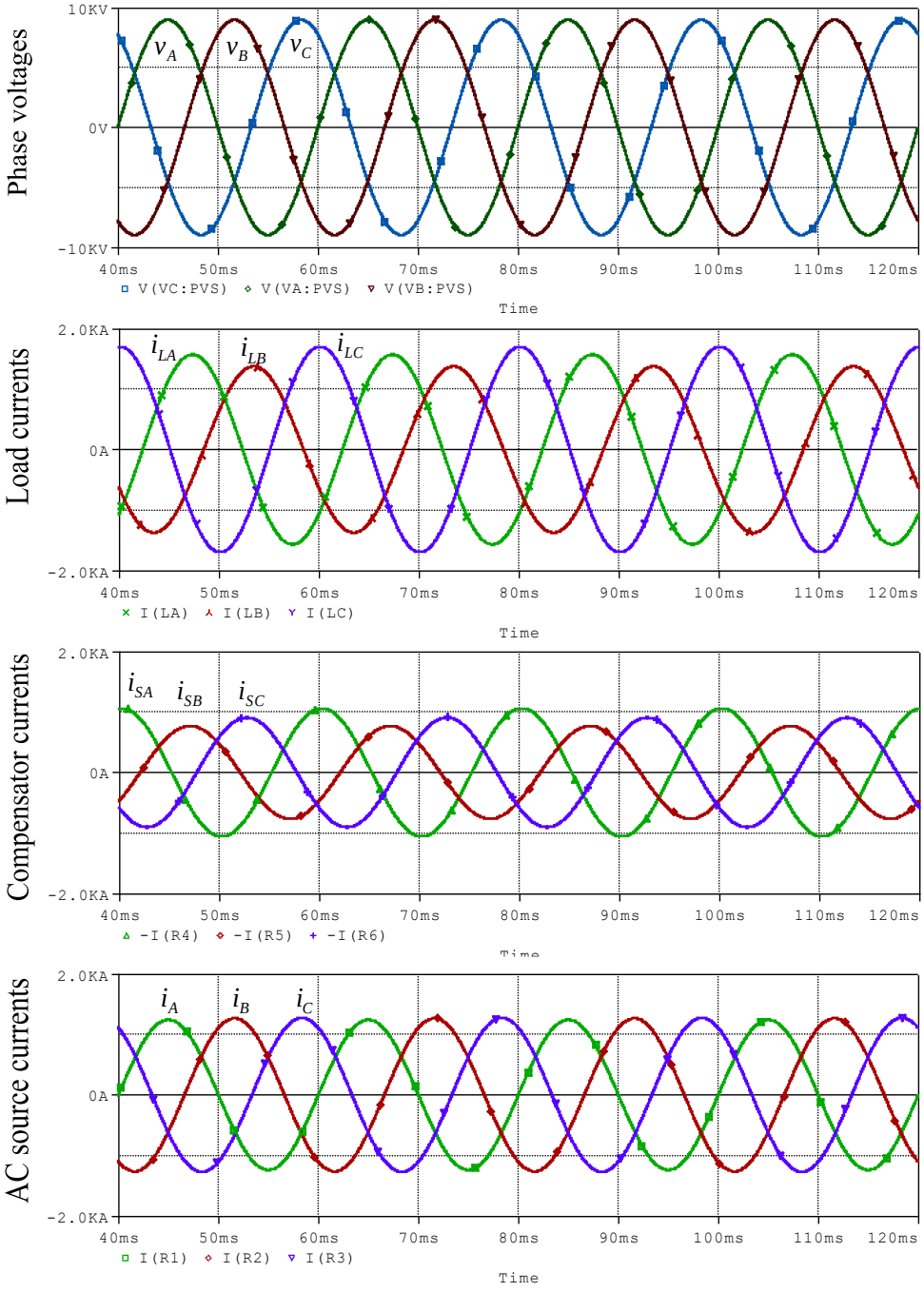

Figure 15. Balancing mechanism of a moderate load unbalance within the rated current of the distribution station handled by the 11 kV 50 Hz load currents balancing system using BWSCB and BWSRB based SVCs

The treatment of a somewhat severe unbalance case is shown in Figure 16. The above unbalance case can be considered severe, since there are significant phase and magnitude unbalance associating the load currents. The balancing process of this unbalance case had yielded balanced active currents i_A, i_B, and i_C drawn from the balanced three-phase AC power system.

The treatment of a severe load unbalance is shown in Figure 17. In this load unbalance, two of the load line currents were exceeding the current capability of the distribution station. It is obvious that the compensation requirements of the above load unbalance were greater than the compensator capability, thus the unbalance was not settled completely. But the compensation process had resulted in large mitigation of phase and magnitude unbalances associating the currents drawn from the AC source What is more, the AC source currents are all brought into the rating capability of the distribution station. This treatment has a

significant impact in the distribution system in Iraq, since the power consumption is somewhat uncontrollable due to the great lack in the available electrical energy there.

The compensating susceptance constructed of 11 kV 50 Hz BWSCB and BWSRB showed during PSpice investigations fast response to slow and abrupt variations in reactive current demand without any sort of harmonic association. In addition, its transient response time was short. This compensating susceptance has zero no load operating losses. The transformerless load currents balancing system constructed by connecting three identical 11 kV 50 Hz compensating susceptances in delta form has a reactive power rating of about 17.1 MVARs (capacitive or inductive). The system is capable to correct to unity the power factor of an Iraqi 11 kV 50 Hz distribution station delivering a balanced three-phase rms current of 1270 A at a 0.707 lagging power factor.

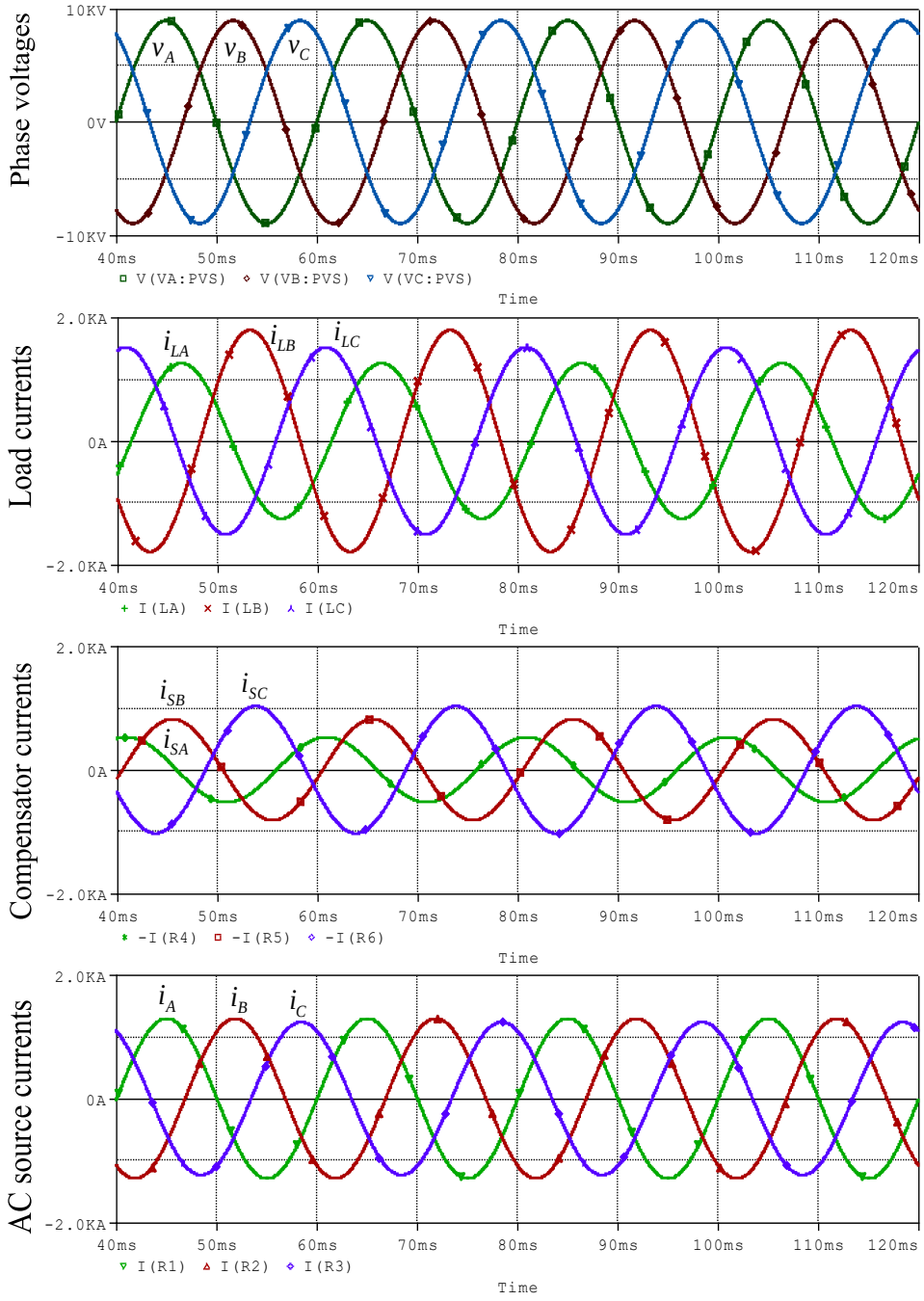

Figure 16. The balancing mechanism of a somewhat severe unbalance case within the distribution station rating handled by the 11 kV 50 Hz load currents balancing system using BWSCB and BWSRB based SVCs

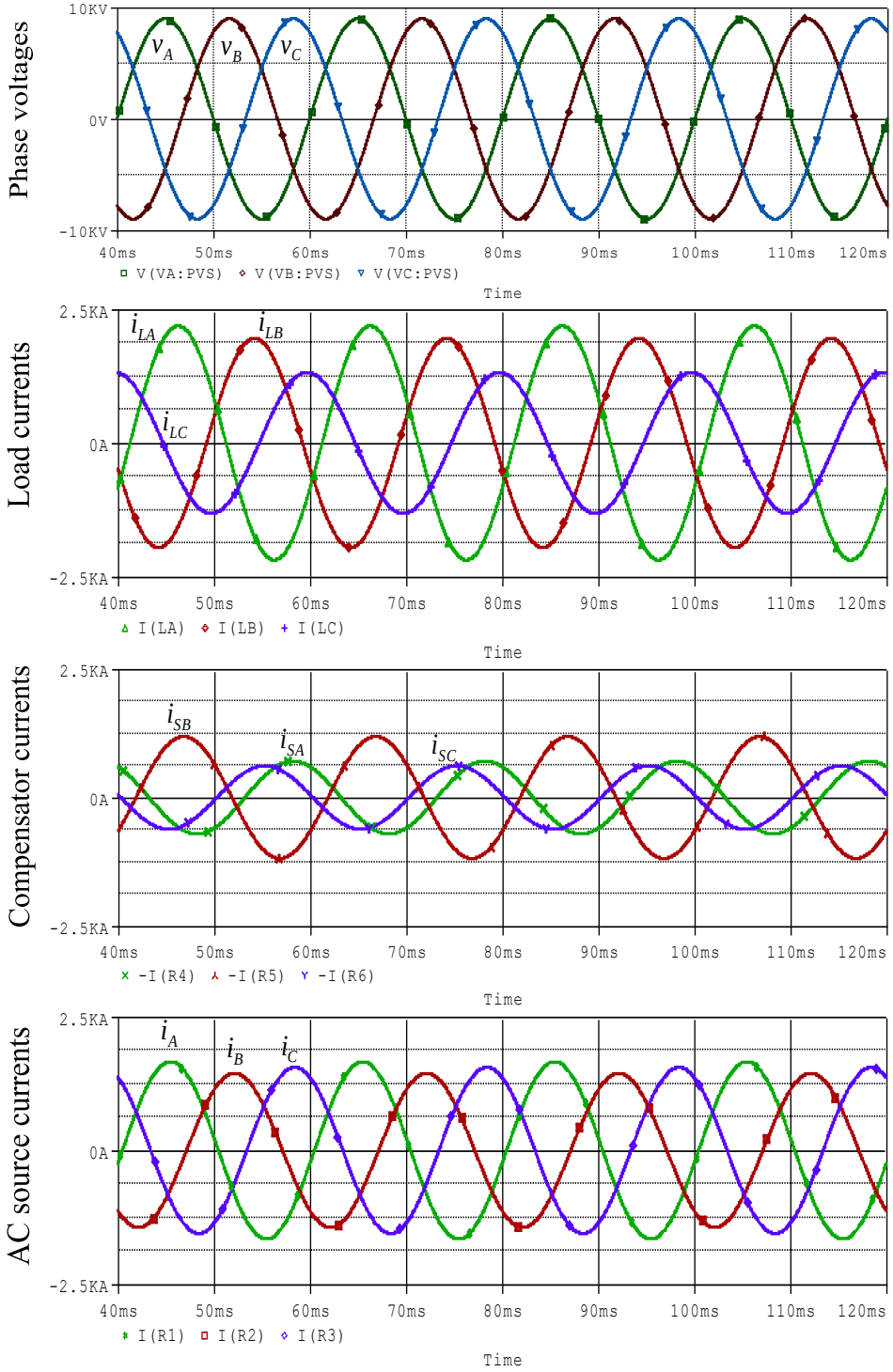

Figure 17. Balancing mechanism of a severe load unbalance beyond the distribution station rating handled by the 11 kV 50 Hz load currents balancing system using BWSCB and BWSRB based SVCs

4. CONCLUSION

The compensating susceptance constructed of 11 kV 50 Hz BWSCB and BWSRB showed during PSpice investigations fast response to slow and abrupt variations in reactive current demand without any sort of harmonic association. In addition, its transient response time was short. This compensating susceptance has zero no load operating losses. The transformerless load currents balancing system constructed by connecting three identical 11 kV 50 Hz compensating susceptances in delta form has a reactive power rating of about 17.1 MVARs (capacitive or inductive). The system is capable to correct to unity the power factor of

an Iraqi 11 kV 50 Hz distribution station delivering a balanced three-phase rms current of 1,270 A at a 0.707 lagging power factor. The system had showed excellent results in performing the task, which was designed for. In addition, the system had treated efficiently different load unbalances; some of them were exceeding the distribution station current rating and the permissible tolerance of load unbalance determined by the protection system installed in the station. The load unbalances which were within the load currents balancing capability had been recovered with balanced active line currents associated with significant reduction in their magnitudes. The system had greatly mitigated the severe load unbalances which were beyond its compensation capability.

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