

Comparative performance of modular with cascaded H-bridge three level inverters

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ABSTRACT

The conventional two-level inverter becomes no longer has the ability to cope with the high-power requirement, so this paper discusses two very common topologies of multilevel inverter like modular multilevel converter (MMC) and cascaded H-bridge (CHB) multilevel inverter for induction motor drive applications. This work attempts to investigate the comparison between MMC and CHB. The comparison is done in aspects of the configuration, concept of operation, advantages and disadvantages, the comparison is also considering output voltage (line to line) waveform, total harmonic distortion (THD) of the output line voltage waveform and the current drawn by both inverters. The performance of the inverters under carrier-based pulse width modulation (PWM) technique and mainly in-phase disposition (IPD), level shifted pulse width modulation is viewed. The paper discusses the comparison between the two multilevel inverters (MLIs) with motor drive applications especially induction motor. The operation of the motor is studied under certain value of load torque. The simulation results for the induction motor with the two inverters (modular multilevel and Cascaded H-bridge) for three numbers of levels using MATLAB/Simulink are provided). The obtained results are encouraging and promising especially in the improvement of the THD% results.

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1. INTRODUCTION

In recent years the industrial requirement for medium voltage high power or mega power apparatus has mightily increased. Induction motors are the most extensively used electrical machine in almost medium and high voltage industrial applications. That is because of its advantages like low cost, simple in construction, requires less maintenance, operates under various challenging environmental conditions (high temperature, noisy both signal and physical impairment) [1] and increased reliability. The control of the induction motor might not be extensive when varied directly from the line voltage. To obtain a wide variation in speed and torque, both voltage and frequency should be modified (ratio of the voltage and frequency should be approximately constant). This V/F control could be applied by using inverters. Lately, inverters are achieving attractiveness and extensively used for induction motor drive applications. Whereas two-level conventional inverters are no longer have the ability to cope with the high-power requirements. So multilevel inverters (MLIs) now are the heart and soul of numerous applications and gain the prominence in academia and industry. The concept of the multilevel inverter is producing high voltage wave by using a sequential connection of lower voltage rating semiconductor switches, like insulated-gate bipolar transistors (IGBT).

The semiconductor devices are swinging between on and off and generate a pattern which approximate to the sinusoidal wave [2], [3]. Every single switch can block its normal rating voltage since the entire output voltage of the inverter can be much higher. Multilevel inverters advantages are their ability to hold with high voltage with least voltage stress on the semiconductors switching devices (little dv/dt), high power quality, high efficiency, have a minor common-mode voltage to reduce stress on bearings of the motor and have a low total harmonic distortion (THD) in the generated voltage [4]–[8]. All these advantages made it more attractive.

However, the conventional multilevel inverters types like neutral point clamped and flying capacitor have a vital flaw which is the in rising the number of required in series IGBTs, clamped diodes and capacitors with the increasing of the voltage levels of the output. This more requirement of components definitely increase the cost, volume and require complex control [9]–[13]. While the cascaded H-bridge converter has layout with simple structure, great modularity and need the least component required to produce a specific voltage level (AC-side) compared to the other multilevel converters [14]. But cascaded H-bridge (CHB) inverter has awful disadvantage that is need a separate isolating DC bus for each cell.

The modular multilevel converter (MMC) not only has the same advantages of the CHB, but also it overcomes the CHB disadvantage and need just one DC bus for each phase. MMC is one of the top and the most promising topologies in multilevel converters family for medium and high voltage applications [15], [16] such as variable speed drives. The principle of this type is depend on string connection of modules (half bridge connection) inverter units to produce a sinusoidal voltage wave. At the other hand CHB, the principle of this inverter is basically depending on a sequent connection of single full bridge (H-bridge) inverter units to produce a sinusoidal voltage. The overall output voltage is the voltage generated by all cells which cascaded. Figure 1 shows the block diagram of the system. A DC-link is fed the inverter with DC voltage (DC-link may be the output of rectifier or photo voltaic PV panels), the inverter converts this DC to alternative current AC. The induction motor is loaded and fed through MMC/CHB inverters with the AC voltage.

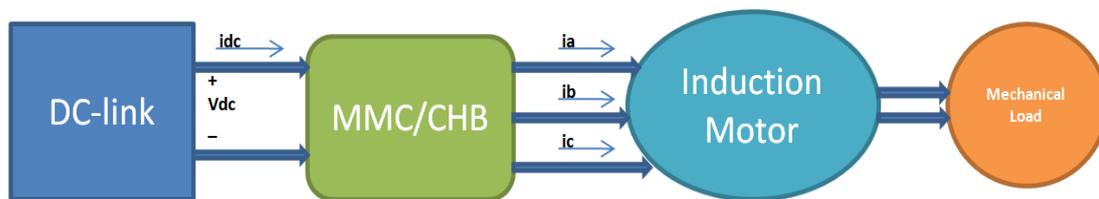


Figure 1. Block diagram of the proposed system

The aim of this research is to compare between three level MMC and CHB multilevel inverters used for induction motor drives. The next sections of the article are prepared as: section 2 present MMC inverter in terms of configuration, operation and advantages and disadvantages, section 3 illustrates the CHB inverter in terms of configuration, operation and advantages and disadvantages, while section 4 indicates the MLIs modulation techniques, and finally section 5 shows the simulation findings of produced voltage waveform, THD of the output line voltage waveform and the current drawn by both inverters via MATLAB/Simulink software and simulate under certain value of load torque. The topology of both inverters is shown in Figure 2(a) and (b).

2. MODULAR MULTILEVEL INVERTER

This section discusses the first inverter (modular type). The discussion is based on configuration, principle of operation and phase generated voltage waveform. The advantages and disadvantages of the MMC inverter are also included.

2.1. Configuration of three-level modular inverter

The consistence of the MMC is mainly three phase-leg connected in parallel. The structure is shown in Figure 2(a) where the DC link is referred as a split DC bus with a total magnitude of V_{dc} (input power of the modular converter). Each leg comprised by two arms (upper and lower arm). The Ac output is taken from the center point of each leg. The single arm is mainly consists of a numbers of sub-modules with identical construction and an inductor (L) to reduce the fault current and to suppress the circulating current. The number of the modules control the voltage levels number (stepped waveform).

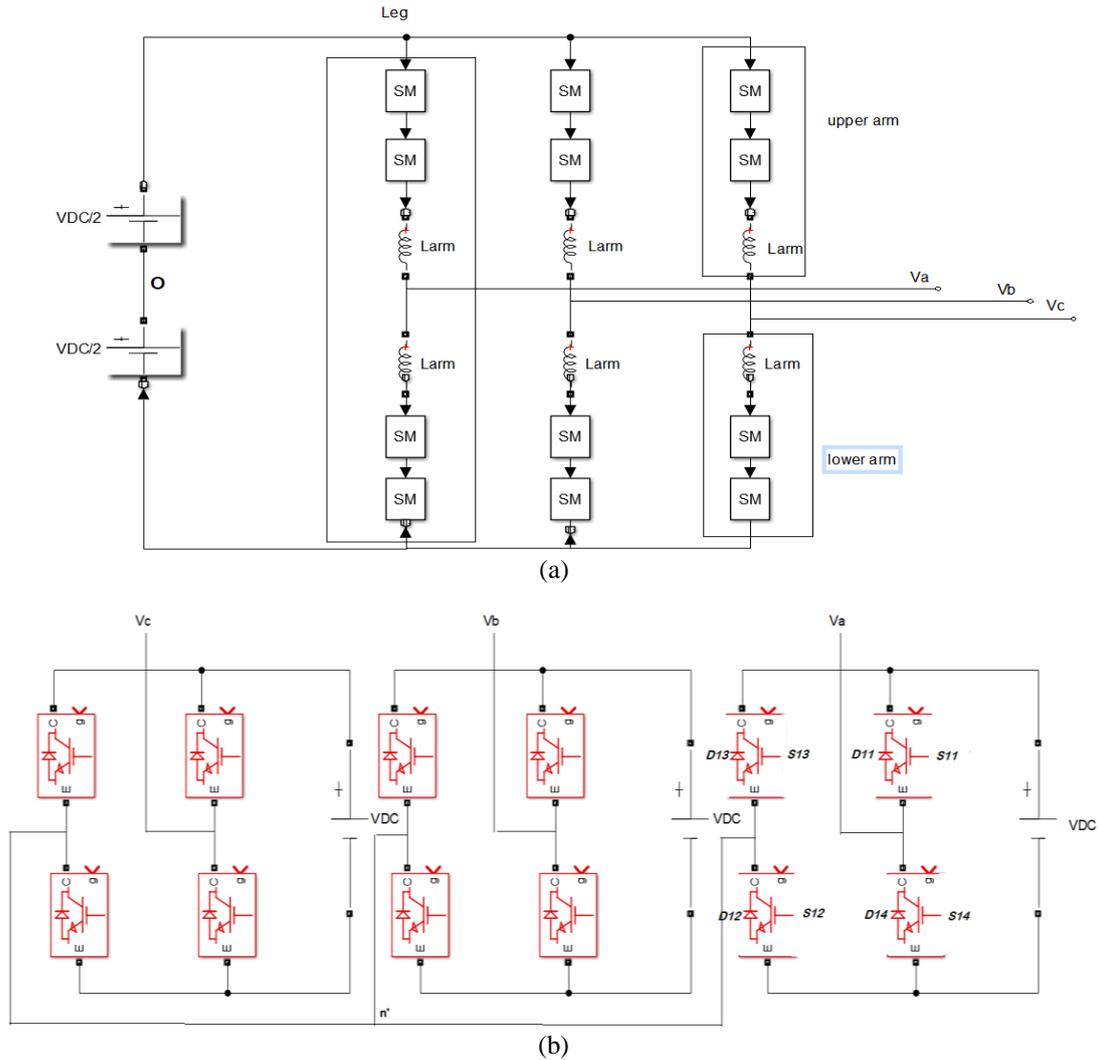


Figure 2. Two multilevel inverters topology (a) three level modular multilevel inverter and (b) three-level H-bridge inverter cell

2.1.1. Sub-module configuration and operation

The sub-module is the basic element of MMC and can has various forms using IGBTs. The common topologies of the module (half bridge sub-module-full bridge sub-module). This research will concentrate on the half bridge topology which mentioned in [17].

It is consists of two power semi-conductor switches (S1, S2) fired in complementary with anti-parallel diode (D1, D2) and capacitor C with average voltage equal to V_c . The half bridge output voltage terminals located at the center point between the two semi-conductors and the other terminal of switch S2. The output voltage defines as V_{sM} and has two levels 0 and $+V_c$ depending on the switching state of switches (S1, S2) and the direction of the current (i_{sm}) where V_c is the voltage on the capacitor. The sub module current is i_{sm} and the positive direction for it is when it flows from the center point into the sub-module and negative when it flows in the opposite direction. The switching states are shown in Table 1 [17].

Table 1. The different switching status for the half bridge sub module

| State | S1, S2 | S1 | D1 | S2 | D2 | Current direction | Capacitor state | V_{sM} |
|------------|--------|-----|-----|-----|-----|-------------------|-----------------|----------|
| Abnormal | (0,0) | OFF | ON | OFF | OFF | + | CHARGE | V_c |
| | | OFF | OFF | OFF | ON | - | BYPASS | 0 |
| Insert/On | (1,0) | OFF | ON | OFF | OFF | + | CHARGE | V_c |
| | | ON | OFF | OFF | OFF | - | DISCHARGE | V_c |
| Bypass/off | (0,1) | OFF | OFF | ON | OFF | + | BYPASS | 0 |
| | | OFF | OFF | OFF | ON | - | BYPASS | 0 |

2.2. Operation of three-level modular inverter

MMC generates the leveled output voltage by inserting or bypassing the sub-modules in and out the circuit. as an example, suppose N number of sub-module per leg 'a' with arm voltage ' V_{ao} ' as shown in Figure 1. As shown in (1) illustrate the average voltage of each capacitor of sub module V_c . The output voltage for each sub-module is V_{H1} , V_{H2} .

$$V_c = \frac{V_{DC}}{N} \quad (1)$$

From Figure 1 and by ignoring the voltage drop on the inductor so the pole voltage as a function of the upper and lower arm voltage by KVL is equal to (2) and (3). Then by summing (2) and (3) and divide the result by two so the equation becomes as (4). When N_{up} and N_{low} is the number of ON sub modules for the upper and lower arm respectively, so the voltage of the upper arm and lower arm by considering the capacitor average voltage and number of ON sub module as (5) and (6) respectively. Finally, by substituting (1), (5) and (6) in (4), so the pole voltage ' V_{ao} ' is equal to (7) Where $N = N_{up} + N_{low}$.

$$V_{ao} = -V_{up} + \frac{V_{DC}}{2} \quad (2)$$

$$V_{ao} = V_{low} - \frac{V_{DC}}{2} \quad (3)$$

$$V_{ao} = \frac{V_{low} - V_{up}}{2} \quad (4)$$

$$V_{up} = N_{up} * V_c \quad (5)$$

$$V_{low} = N_{low} * V_c \quad (6)$$

$$V_{ao} = \frac{V_{low} - V_{up}}{2} = \left(\frac{N_{low} - N_{up}}{N} \right) * \frac{V_{DC}}{2} \quad (7)$$

At $N+1$ levels of voltage can be created by the MMC with number of N sub-modules per arm. So as an example, for $N=2$ the arm voltage has three levels according to the inserted sub-modules. So based on (7), Table 2 summarize the multiple switching states and the corresponding out pole voltage.

Table 2. The output voltage for phase (a) for $N=2$ sub modules of MMC

| State | N upper | N lower | V upper | V lower | Vao |
|-------|---------|---------|---------|---------|---------|
| 1 | 0 | 2 | 0 | VDC | 0.5VDC |
| 2 | 1 | 1 | 0.5VDC | 0.5VDC | 0 |
| 3 | 2 | 0 | VDC | 0 | -0.5VDC |

2.3. Advantages and disadvantages of MMC inverter

MMC inverter is widely adopted in industry as a result of its advantages. However, MMC inverter poses few disadvantages that restrict its use. This section discusses some advantage and disadvantages of MMC as:

- Advantages: i) modular multilevel has simple and modular structure with identical configuration compared to the other types of MLI so can be scaled easily which makes it convenient for several levels of voltage; ii) high equivalent switching frequency generated by actual low switching frequencies of individual switching devices and high efficiency; iii) no need for bulky filter at the output cause of low THD; and iv) eliminates the need for the split DC bus and the isolating transformer.
- Disadvantage: the existence of the circulating current inside the converter due the mismatch between the input DC voltage and the sub-modules which inserted.

3. CASCADED H-BRIDGE MULTILEVEL INVERTER

This section illustrates the second inverter 'cascaded H-bridge' type. This inverter is unique and has a special position in multilevel inverters filed. The configuration of the H-bridge, principle of operation, phase output voltage waveform and advantages and disadvantages of the CHB multilevel inverter are taken into account.

3.1. Configuration of three level cascaded H-bridge inverter

The consistence of the CHB is mainly three H-bridge [18], [19]. The structure is shown in Figure 2(b) where the DC links are referred as a split DC buses with a magnitude of V_{dc} for each H-bridge. An m -level for CHB require $(2H+1)$ is an odd number, where H is the number of cells. These H-bridge have an identical construction. For the 3-level cascaded H-bridge (CHB) each leg or phase needs only single full bridge (H-bridge) to generate three voltages at the output ($+V_{dc}$, 0 , $-V_{dc}$). Each one consists of four power (2-pairs) semiconductor switches each pair works in complementary modes to prevent the short circuit.

The topology of the H-bridge is as Figure 2(b). Three different feasible switching states are available. At any time, a set of two switches is on for a three-level inverter as shown in Table 3. The positive value of voltage ($+V_{dc}$) can be achieved by two ways according to the direction of the current, if the current direction is positive so the current path will be through switches S11 and S12 (S11 and S12 are on '1'), else if the current direction is negative so the current path will be through diode D11 and D12 (D11 and D12 are on '1'). The zero and negative voltage (0 , $-V_{dc}$) can be achieved as shown in Table 3.

Table 3. The different switching status for H-bridge according to current direction

| State | S11 | D11 | S12 | D12 | S13 | D13 | S14 | D14 |
|-------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| Positive direction of current | | | | | | | | |
| $V_{an}' = +V_{dc}$ | ON | OFF | ON | OFF | OFF | OFF | OFF | OFF |
| $V_{an}' = 0$ | OFF | OFF | ON | OFF | OFF | OFF | OFF | ON |
| $V_{an}' = 0$ | ON | OFF | OFF | OFF | OFF | ON | OFF | OFF |
| $V_{an}' = -V_{dc}$ | OFF | OFF | OFF | OFF | OFF | ON | OFF | ON |
| Negative direction of current | | | | | | | | |
| $V_{an}' = +V_{dc}$ | OFF | ON | OFF | ON | OFF | OFF | OFF | OFF |
| $V_{an}' = 0$ | OFF | ON | OFF | OFF | ON | OFF | OFF | OFF |
| $V_{an}' = 0$ | OFF | OFF | OFF | ON | OFF | OFF | ON | OFF |
| $V_{an}' = -V_{dc}$ | OFF | OFF | OFF | OFF | ON | OFF | ON | OFF |

3.2. Advantages and disadvantages of CHB inverter

CHB inverter has several advantages over the other inverters. While it has an inherent disadvantage that may impedes its employment in some cases. This section discusses the advantage and disadvantages of CHB as:

- Advantages: i) this topology of MLI uses the minimum number of devices or components among all types of MLIS to get the same voltage's level with a good harmonic spectrum (no clamped diode or flying capacitors required) [12], [20]; ii) the separate fed of DC sources makes this type has no balancing problems in voltage; iii) good choice for high voltage applications cause of the high power rating result of the sequent connection of the H-bridge cell; and iv) each single H-bridge has the same configuration so modularized circuit structure is possible [20].
- Disadvantage: due to the separate fed DC supply for each cell, high number of sources is required (hence large number of isolating transformers).

4. MULTILEVEL MODULATION TECHNIQUES

Despite of many modulation approaches produced for multilevel case, only few techniques found their way to the industries. Among these approaches especially pulse width modulation (PWM) is commonly used. The PWM for the conventional inverter voltage source inverter (VSI) principle which described is extended and used in multilevel inverters with m -levels, but there is little difference. The m -level inverter needs number of carriers equal to $(m-1)$ waves to compare with the sinusoidal reference wave (multi carrier PWM), each carrier introduces between two voltage levels. Multi carrier PWM could be classified into two categories [21]–[23]: i) level-shifted PWM (LS-PWM) and ii) phase-shifted PWM (PS-PWM).

4.1. LS-PWM

As its name, the multi carrier waves are disposed in vertical levels or shifts and have the same amplitude and frequency (A_c , f_c). The carrier wave amplitude is the multi carrier PWM is equal to $(1/n-1)$ times in the carrier of the conventional inverter (two levels). For 3-level inverter two triangle carrier wave are used to compare with the 3-sinusoidal reference waves with 120-degree shift. If the reference waveform amplitude is greater than all carriers so a switching order is sent to change the switches position to produce positive voltage level, if the reference waveform amplitude is lower than the highest above zero carrier but greater than the other carrier so a switching order is sent to change the switches position to produce 0 voltage level, if the amplitude of the reference waveform is lower than all carriers so a switching order is sent to change the switches position to produce negative voltage level. Level-shifted PWM could be classified based

on phase disposition (in-phase disposition (IPD)-phase opposite disposition (POD)-alternative phase opposite disposition (APOD)) as [24]–[26]. In this work IPD level shifted PWM is chosen to be simulated.

5. SIMULATION AND RESULTS

The modular and cascaded H-bridge three level inverter models are done via MATLAB/Simulink. Figures 3(a) and (b) presents the layout of the simulation configuration for both inverters MMC and CHB respectively. Noting that in Figure 3(a) the half-bridge sub-modules are compacted in subsystems for simplicity and have the same configuration.

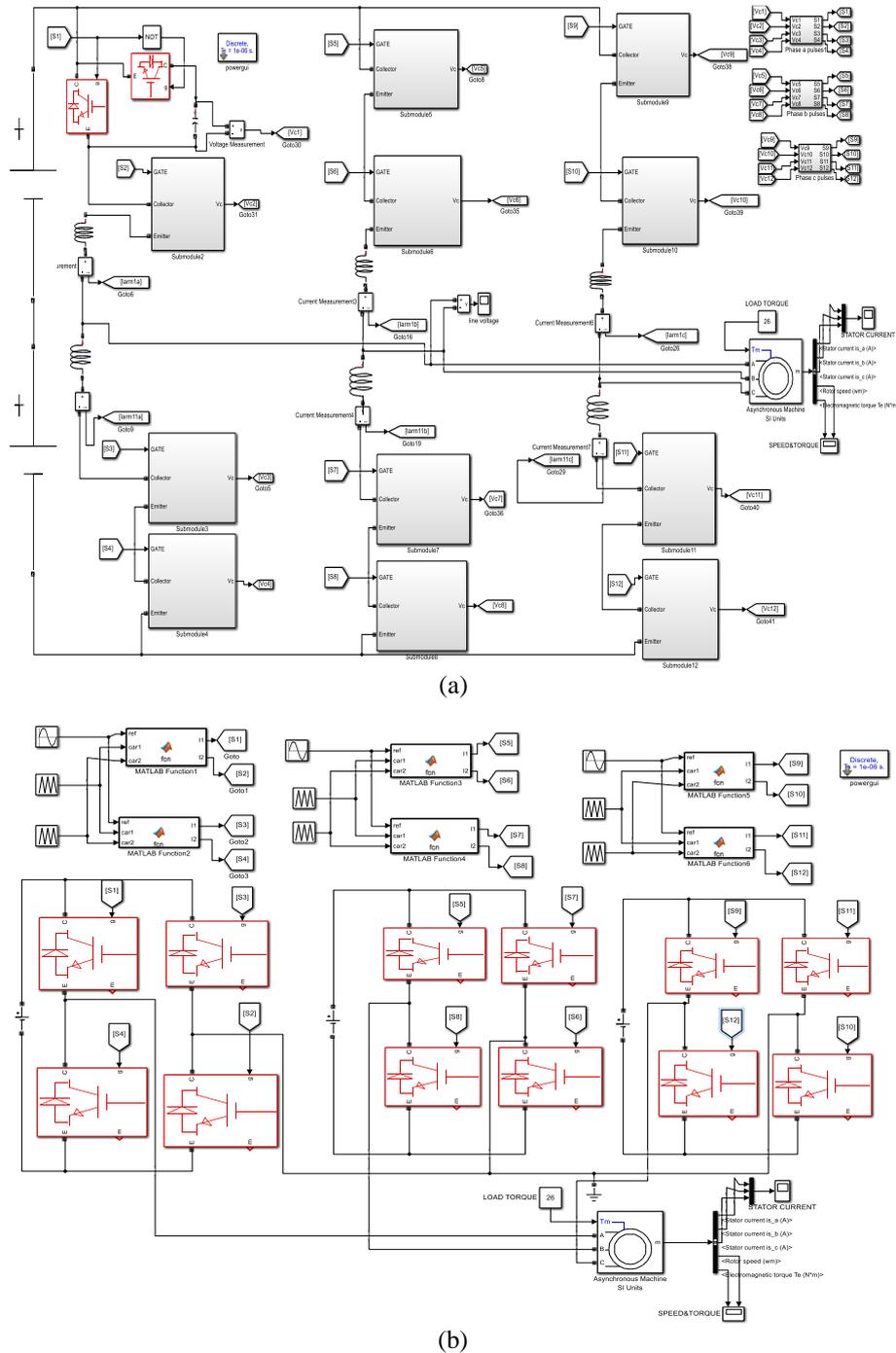


Figure 3. Two multilevel inverters MATLAB simulation, (a) three level modular multilevel inverter and (b) three-level H-bridge inverter

The both inverters output waveform quality, the motor speed, the motor torque, the three-phase stator current and the total harmonic distortion of the line voltage are introduced at 26 Nm torque are demonstrated in Figures 4(a) to (d) and Figures 5(a) to (d). The three level MMC simulation parameters are: A DC-link of 460 V, the capacitors of the sub module are $1100 \times 10^{-6} \text{F}$ each, and 5 kHz switching frequency. The parameter used for simulation of the CHB is DC-link of 230 V per each phase. The induction motor has 400 V rating, 5.4 HP, 4-poles, 50 Hz, 1430 rpm.

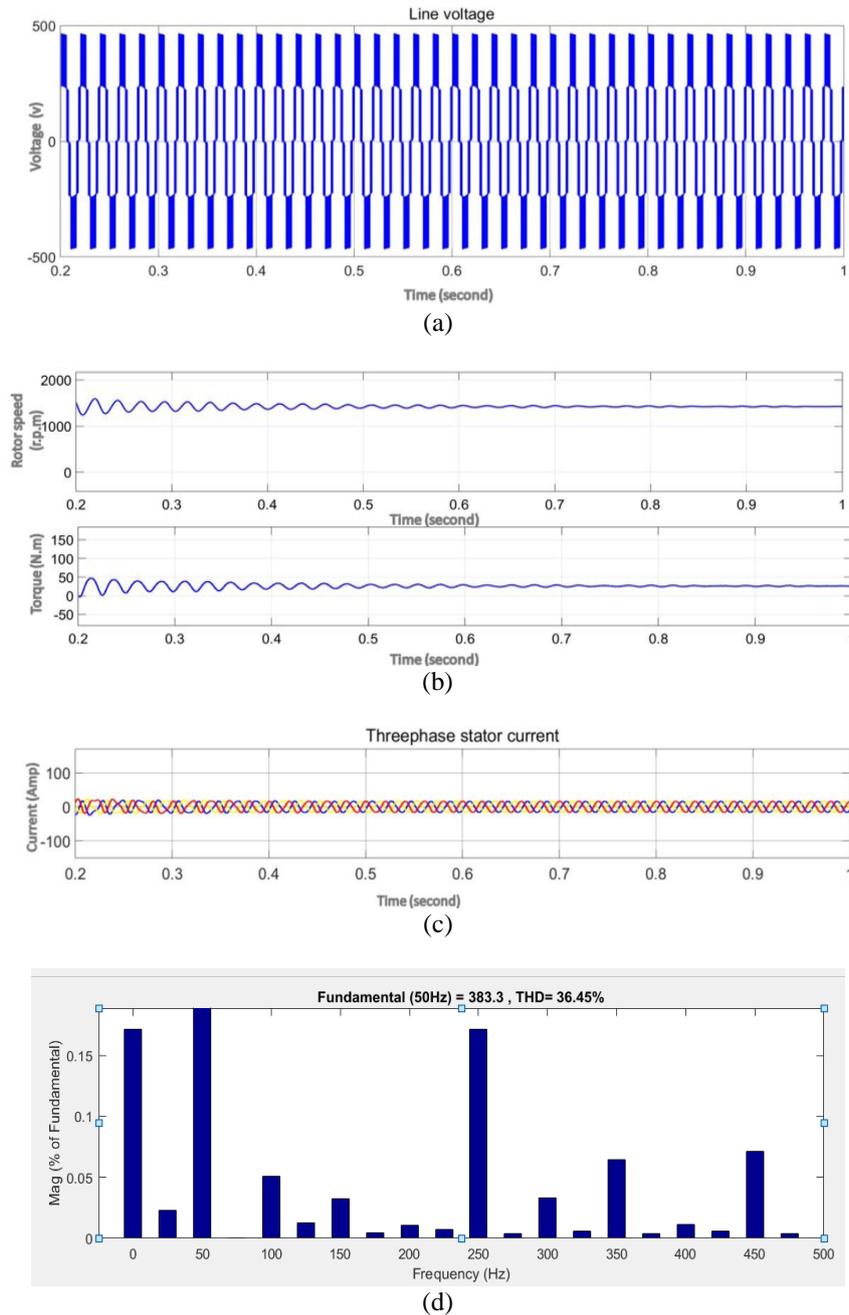


Figure 4. The simulation wave forms of MMC, (a) the line voltage (V), (b) motor speed (rpm) and electromagnetic torque (Nm), (c) the stator current (A), and (d)THD

It is obvious from Figures 4(a) to (d) and Figures 5(a) to (d) that the output line voltages of both inverters are swings in steps to draw a waveform similar and close to the sinusoidal waveform which results a high quality for the output wave, a low voltage stress (dv/dt) on the switching devices, require minimum rating for switches so decrease the cost and the volume of the inverter. The magnitude of the max output line

voltage of CHB is twice the DC-link fed each phase, while the max line voltage for MMC is equal to the DC-link fed the whole phases. MMC needs only one DC-link, unlike the CHB which need a DC-link for each cell. The three-phase stator current act almost like a balanced sinusoidal wave (except the transient period) and it is approximately the same for both inverters. The speed and torque curves do not much differ for the inverters; they oscillate for around 0.6 second then reach the steady state. The THD of the output line voltage is about 37% (the THD of CHB is a little higher) which considered acceptable regards to only three levels topology.

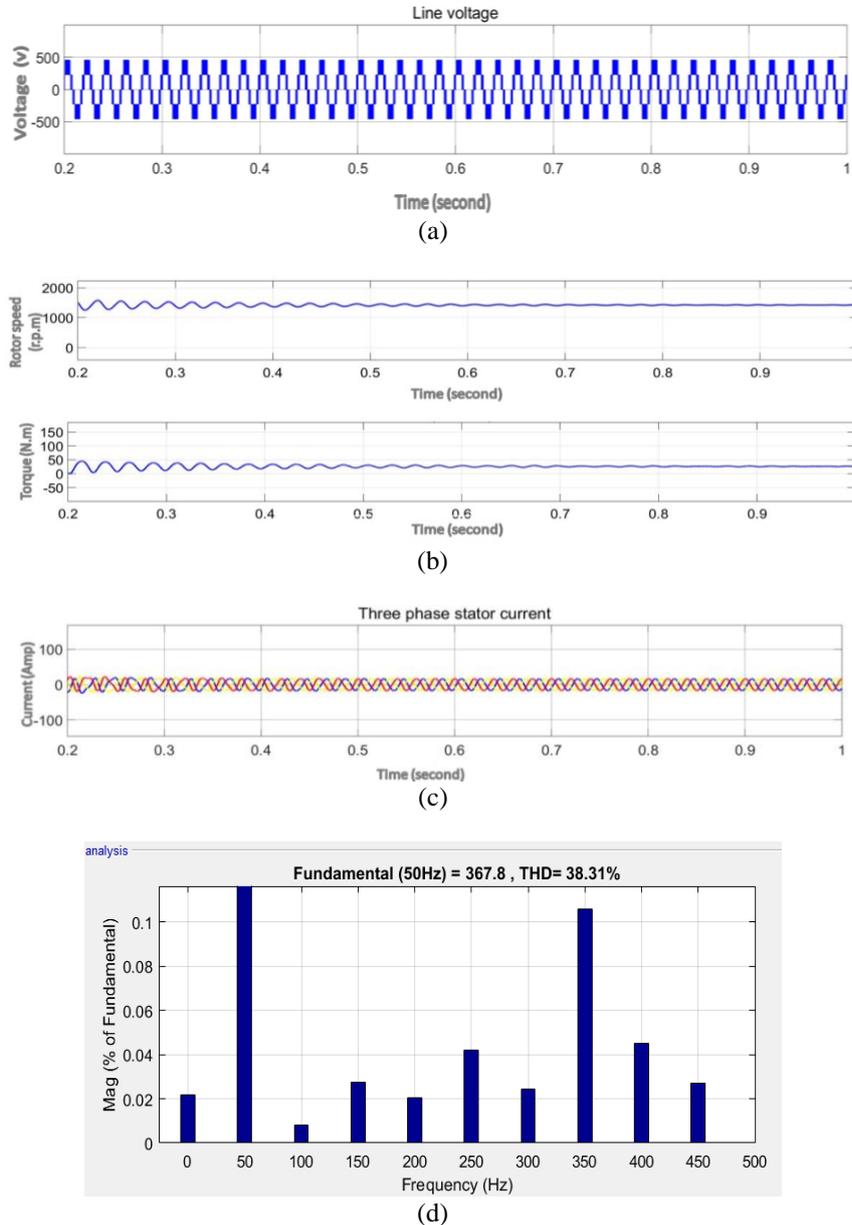


Figure 5. The simulation waveforms of CHB (a) the line voltage (V), (b) motor speed (rpm) and torque (Nm), (c) the stator current (A), and (d)THD

6. CONCLUSION

This paper aims to compare between the three-level modular multilevel inverter and cascaded H-bridge with IM using MATLAB/Simulink. The comparison has been introduced in terms of the configuration, concept of operation, advantages and disadvantages, THD of the produced line voltage waveform and the current drawn by both inverters. The THD of the three level inverters have good harmonic

spectrum which almost 37 %, while the conventional two-level inverter is usually higher. This low THD minimize the electromagnetic interference and decrease the cost and size of the bulk filter. The THD spectrum is improved with increasing number of levels. Hence, using the multilevel inverters especially MMC and CHB is considered an attractive candidate for Induction Motor applications.

REFERENCES

- [1] T. Amanuel, A. Ghirmay, H. Ghebremeskel, R. Ghebrehiwet, and W. Bahlibi, "Comparative analysis of signal processing techniques for fault detection in three phase induction motor," *Journal of Electronics and Informatics*, vol. 3, no. 1, pp. 61–76, Apr. 2021, doi: 10.36548/jei.2021.1.006.
- [2] T. Muhammad, A. U. Khan, H. Jan, M. Y. Usman, J. Javed, and A. Aslam, "Cascaded symmetric multilevel inverter with reduced number of controlled switches," *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 8, no. 2, pp. 795–803, Jun. 2017, doi: 10.11591/ijpeds.v8.i2.pp795-803.
- [3] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Transactions on Industry Applications*, vol. 37, no. 2, pp. 637–641, 2001, doi: 10.1109/28.913731.
- [4] E. Babaei, S. Alilu, and S. Laali, "A new general topology for cascaded multilevel inverters with reduced number of components based on developed h-bridge," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 8, pp. 3932–3939, Aug. 2014, doi: 10.1109/TIE.2013.2286561.
- [5] M. F. Kangarlu and E. Babaei, "A generalized cascaded multilevel inverter using series connection of submultilevel inverters," *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 625–636, Feb. 2013, doi: 10.1109/TPEL.2012.2203339.
- [6] J.-H. Kim, S.-K. Sul, and P. N. Enjeti, "A carrier-based PWM method with optimal switching sequence for a multilevel four-leg voltage-source inverter," *IEEE Transactions on Industry Applications*, vol. 44, no. 4, pp. 1239–1248, 2008, doi: 10.1109/TIA.2008.926201.
- [7] O. Lopez *et al.*, "Comparison of the FPGA implementation of two multilevel space vector PWM algorithms," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 4, pp. 1537–1547, Apr. 2008, doi: 10.1109/TIE.2008.917159.
- [8] E. Babaei and S. S. Gowgani, "Hybrid multilevel inverter using switched capacitor units," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 9, pp. 4614–4621, Sep. 2014, doi: 10.1109/TIE.2013.2290769.
- [9] N. Devarajan and A. Reena, "Reduction of switches and DC sources in cascaded multilevel inverter," *Bulletin of Electrical Engineering and Informatics (BEEL)*, vol. 4, no. 3, pp. 186–195, Sep. 2015, doi: 10.11591/eei.v4i3.320.
- [10] M. M. Hasan, A. Abu-Siada, and M. S. A. Dahidah, "A three-phase symmetrical DC-link multilevel inverter with reduced number of DC sources," *IEEE Transactions on Power Electronics*, vol. 33, no. 10, pp. 8331–8340, Oct. 2018, doi: 10.1109/TPEL.2017.2780849.
- [11] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A review," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 135–151, Jan. 2016, doi: 10.1109/TPEL.2015.2405012.
- [12] N. Prabaharan and K. Palanisamy, "A comprehensive review on reduced switch multilevel inverter topologies, modulation techniques and applications," *Renewable and Sustainable Energy Reviews*, vol. 76, pp. 1248–1282, Sep. 2017, doi: 10.1016/j.rser.2017.03.121.
- [13] G. Jayaraju and G. S. Rao, "Intelligent controller based power quality improvement of microgrid integration of photovoltaic power system using new cascade multilevel inverter," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 9, no. 3, pp. 1514–1523, Jun. 2019, doi: 10.11591/ijece.v9i3.pp1514-1523.
- [14] A. Marzoughi, R. Burgos, D. Boroyevich, and Y. Xue, "Investigation and comparison of cascaded H-bridge and modular multilevel converter topologies for medium-voltage drive application," in *IECON 2014-40th Annual Conference of the IEEE Industrial Electronics Society*, Oct. 2014, pp. 1562–1568, doi: 10.1109/IECON.2014.7048710.
- [15] B. Gemmel, J. Dorn, D. Retzmann, and D. Soerangr, "Prospects of multilevel VSC technologies for power transmission," in *2008 IEEE/PES Transmission and Distribution Conference and Exposition*, Apr. 2008, pp. 1–16, doi: 10.1109/TDC.2008.4517192.
- [16] S. Kouro *et al.*, "Recent advances and industrial applications of multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010, doi: 10.1109/TIE.2010.2049719.
- [17] Y. Shunfeng, "Control and operation of modular multilevel converters," PhD Thesis, Nanyang Technological University, 2018.
- [18] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez, "A survey on cascaded multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010, doi: 10.1109/TIE.2009.2030767.
- [19] L. Nanda, A. Dasgupta, and U. K. Rout, "A comparative analysis of symmetrical and asymmetrical cascaded multilevel inverter having reduced number of switches and DC sources," *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 8, no. 4, pp. 1595–1602, Dec. 2017, doi: 10.11591/ijpeds.v8.i4.pp1595-1602.
- [20] N. Farokhnia, S. H. Fathi, N. Yousefpoor, and M. K. Bakhshizadeh, "Minimisation of total harmonic distortion in a cascaded multilevel inverter by regulating voltages of DC sources," *IET Power Electronics*, vol. 5, no. 1, pp. 106–114, 2012, doi: 10.1049/iet-pel.2011.0092.
- [21] A. Tsunoda, Y. Hinago, and H. Koizumi, "Level- and phase-shifted PWM for seven-level switched-capacitor inverter using series/parallel conversion," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 8, pp. 4011–4021, Aug. 2014, doi: 10.1109/TIE.2013.2286559.
- [22] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: a theoretical analysis," *IEEE Transactions on Power Electronics*, vol. 7, no. 3, pp. 497–505, Jul. 1992, doi: 10.1109/63.145137.
- [23] T. Venkat and S. Periasamy, "A new seven level symmetrical inverter with reduced switch count," *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 9, no. 2, pp. 921–925, Jun. 2018, doi: 10.11591/ijpeds.v9.i2.pp921-925.
- [24] Z. Jing, H. Xiangning, and Z. Rongxiang, "A novel PWM control method for hybrid-clamped multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2365–2373, Jul. 2010, doi: 10.1109/TIE.2009.2027915.
- [25] A. Alexander S, "Development of solar photovoltaic inverter with reduced harmonic distortions suitable for Indian sub-continent," *Renewable and Sustainable Energy Reviews*, vol. 56, pp. 694–704, Apr. 2016, doi: 10.1016/j.rser.2015.11.092.
- [26] Y. Babkrani, A. Naddami, and M. Hilal, "A smart cascaded H-bridge multilevel inverter with an optimized modulation techniques increasing the quality and reducing harmonics," *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 10, no. 4, pp. 1852–1862, Dec. 2019, doi: 10.11591/ijpeds.v10.i4.pp1852-1862.

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