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Conducted electromagnetic interference mitigation in super-lift Luo-converter for electric vehicle applications

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ABSTRACT

In this article, a digital chaotic pulse width modulation (DCPWM)-dependent electromagnetic interference (EMI) noise attenuating procedure has been implemented. With the aid of a field programmable gate array (FPGA), a randomized carrier frequency modulation with a fixed duty cycle has been generated through chaotic carrier frequency, and this process is called DCPWM. Conducted EMI suppression is achieved in a 200 kHz, 40 W elementary positive output super lift Luo (EPOSLL) converter using the DCPWM technique. The results are compared and validated with periodic PWM over DCPWM in simulation and hardware with electromagnetic compatibility (EMC) standards. Besides, 9 dBV (2.81 V) of conducted EMI noise has been minimized in the DCPWM approach against periodic pulse width modulation method for the EPOSLL converter in electric vehicles applications.

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1. INTRODUCTION

Electromagnetic interference (EMI) is an obnoxious noise that degrades the functioning of power electronics-based equipment used in daily life such as home appliances and various industries by emitting both conducted and radiated electromagnetics into the environment [1]. Due to the sudden increase in current and voltage caused by the fast-switching process in the circuits, EMI noise has been generated in various direct current to direct current (DC-DC) converters. EMI filters are the most common technique used to mitigate the problems caused by conducted EMI. With the use of different resistance values, this filter is used to block the undesirable signal while allowing the desired signal. However, to incorporate an EMI filter, an additional cost, area, and weight have been considered a drawback [2]–[4]. Electromagnetic shielding is the second method to mitigate the EMI. In this method, an enclosure is made around the device, and in that way, the EMI has been minimized by disconnecting the communication of the EMI to the atmosphere. But the connection of cables for input as well as output through sockets may reduce the effectiveness of EMI shielding [5]. In switched-mode power supplies (SMPS), a metal packaged case has been used to cover the entire assembly to mitigate the EMI, but the additional cost is required, and there are also some possibilities of EMI leakage through some other accessories like the display unit, cable, and light-emitting diode (LED) lights [6]. The next popular method among the researchers is the randomization technique, which varies the width or position of the pulse randomly. In that way, the surging value of the spectrum is stretched, and EMI noise has been mitigated. But generating a random pulse is difficult because in that way the circuits become complicated. Digital chaotic pulse width modulation (DCPWM) is the modernistic approach to alleviate the EMI during the switching process [7]. The elementary positive output super lift Luo (EPOSLL) converter is new in the area of DC-DC converters with voltage lifting techniques for high gain, positive output, and more efficiency in electric vehicles

(EV) applications. In this technique, the voltage has been lifted three times by the input voltage at a duty cycle of 0.5 [8]–[11]. In this circuit, a power MOSFET is used as a fast ON/OFF switch. This creates EMI, which is then reduced by using the DCPWM technique. This paper will discuss the advantages of DCPWM-based EMI mitigation over the periodic pulse width modulation (PWM) technique on the EPOSLL converter used in EV applications. Because of the high switching frequency, EMI has been generated, reducing the system's efficiency. This digital approach is very easy and accurate for the EMI mitigation process to improve the efficiency and reliability of the DC-DC converters.

2. ELEMENTORY POSITIVE OUTPUT SUPER-LIFT LUO CONVERTER

The EPOSLL converter evolved from the Luo converter, which acts based on the theory of voltage amplifying technique. The input is advanced by three times with respect to the duty cycle and the gain is also increasing. Figures 1(a) and 1(b) explains the circuit operation of the EPOSLL converter.

2.1. During ON condition

In the closed position is switch S, diodes D_1 and D_2 is ON and OFF respectively, the capacitor voltage VC_1, and the inductor current I_{L1} also increases through V_{in}. As a result, VC_1 and V_L are moving in the loop, yielding V_{C1} as ($V_{in}+V_L-V_o$). In that way, the desired voltage is developed in the loop, as shown in Figure 1(a) [12]–[14]. Based on the duty cycle of the pulse, the voltage gain ratio is increased to the desired level to energize the auxiliary systems in the EV.

2.2. During OFF condition

In the open position is switch S, diodes D_1 and D_2 is OFF and ON respectively, voltage V_o-2V_{in} decreases i_{L1}. So, the load receives the entire current. The gain has been increased by the duty cycle. The energy from inductor L_1 and capacitor C_1 is reached R through C_2. as shown in Figure 1(b). Here the gate pulse is in OFF position based on the duty cycle ratio.

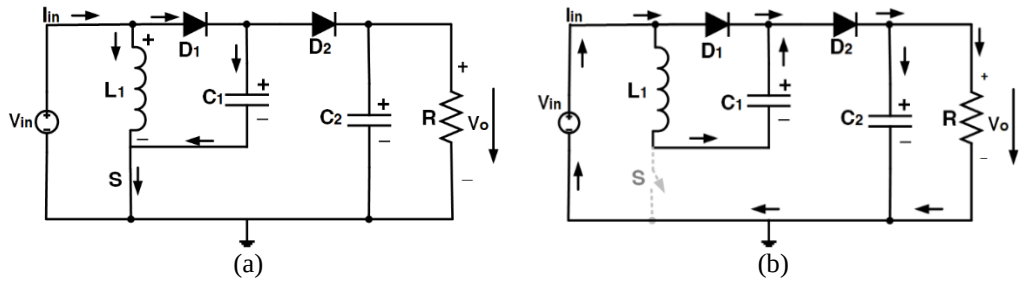

Figure 1. Modes of operation in (a) ON-condition and (b) OFF-condition

2.3. Mathematical model

The EPOSLL converter equivalent circuits during switch-ON and switch-OFF are shown in Figures 2(a) and 2(b). When switched ON, capacitor C_1 is energized from the input voltage V_{in}. The inductor current, i_{L1}, which is streaming over the inductor, is increased. During switch-OFF, the capacitor C_1 started to discharge, and in that way, the current gushing over the inductor L_1 decreased.

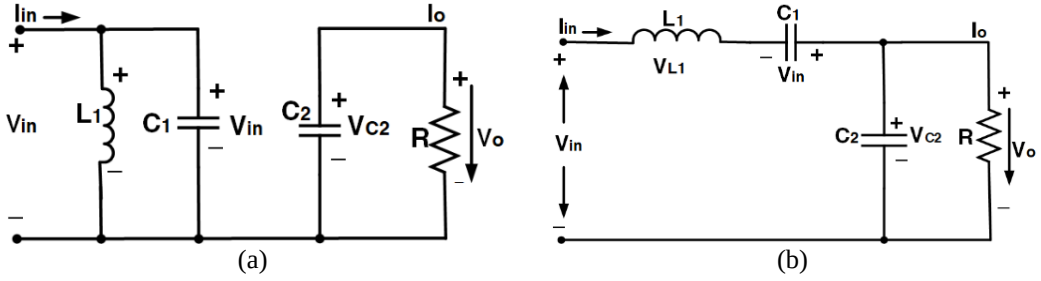

Figure 2. Equivalent circuits in (a) switch-ON state and (b) switch-OFF state

The ripple of inductor current i_{L1} is given by (1).

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT = \frac{V_o - 2V_{in}}{L_1} (1-k) \quad (1)$$

The voltage output is given by (2).

$$V_o = \frac{2-k}{1-k} V_{in} \quad (2)$$

The voltage moved gain is given by (3).

$$G = \frac{V_o}{V_{in}} = \frac{2-k}{1-k}; \text{ duty cycle k} = \frac{T_{on}}{T} \quad (3)$$

While *S* is ON, the gross currents flowing through the inductor and capacitor equals the input current I_{in}. During *S* is OFF, the input current equals the capacitor current I_{C1} and the inductor current i_{L1}, as shown in (4) to (6).

$$I_{in-off} = I_{L1-off} = i_{C1-off} \quad (4)$$

$$I_{in-on} = I_{L1-on} + i_{C1-on} \quad (5)$$

$$kTi_{C1-on} = (1-k)Ti_{C1-off} \quad (6)$$

If L_1 is numerous, i_{L1} is nearabout its average current. Therefore, the average I_{L1} is given by (7) and (8) when $I_{L1} = i_{L1}$,

$$i_{in-off} = i_{C1-off} = I_{L1} \quad (7)$$

$$i_{C1-on} = \frac{1-k}{k} I_{L1} \quad (8)$$

and the input current i_{in} is given by (9).

$$i_{in} = 2I_{L1} - kI_{L1} \quad (9)$$

Since the ratio of input voltage to current is given by (10).

$$\frac{V_{in}}{I_{in}} = K \frac{V_o}{I_o} = KR \text{ ; where K} = \left(\frac{1-k}{2-k}\right)^2 \quad (10)$$

The ratio of current i_{L1} through inductor L_1 is given by (11).

$$\xi_1 = \frac{\Delta i_{L1/2}}{I_{L1}} = \frac{k(2-k)TV_{in}}{2L_1 I_{in}} = \left(\frac{1-k}{2-k}\right)^2 \frac{R}{fL_1} \quad (11)$$

The output ripple voltage $\mathcal{V}_o$ is given by (12).

$$\Delta\mathcal{V}_o = \frac{\Delta Q}{C_2} = kT \frac{I_0}{C_2} = \frac{k}{fC_2} \frac{V_o}{R} \quad (12)$$

Therefore, $\mathcal{V}_o$ deviation is given by (13).

$$\varepsilon = \frac{k}{2RfC_2} \quad (13)$$

3. DIGITAL CHAOTIC PULSE GENERATION AND IMPLEMENTATION

Chaotic modulation is a type of spectrum spreading modulation. Fundamentally, chaotic modulation is about incorporating an external disturbance into pulse-width modulation (PWM), which redesigns the frequency or duty cycle of the pulses within a limit. Hence, energy peaks are spread, and the harmonics are continuously distributed [15]–[18].

3.1. Randomized carrier frequency modulation with fixed duty cycle

A randomized carrier frequency with a fixed duty cycle (RCFMFD) scheme is preferred to get the chaotic pulses by keeping the duty cycle constant, as shown in Figure 3. Low-frequency harmonics are generated when the randomization technique is applied. The peak spectral density was also reduced through this technique. In this method, the carrier frequency is randomized by varying the width of the carrier waves while keeping the duty cycle constant to get a constant DC output. Generating an irregular carrier frequency should be within a certain limit to get the best performance from EMI mitigation. So, the limit of the F_{sw} is sustained at ±1/3rd of the primary switching frequency. A linear feedback shift register is used to build the pseudo-random digit to get RCFMFD [19]–[22].

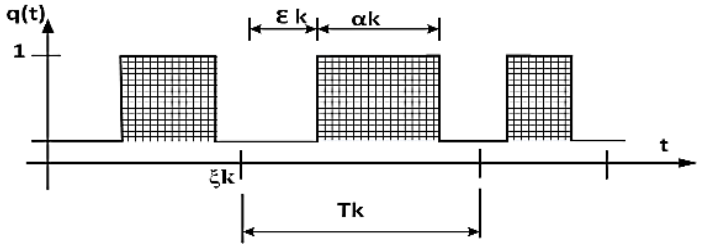

Figure 3. Randomized switching signal

T_k is k^{th} cycle duration, α_k is switch ON state, ε_k is the switch OFF state, d_k is the duty ratio, ξ_k is the k^{th} cycle initial time, $q(t)$ is the switching function. As cited in Figure 3, ξ_k is derived by (14).

$$\xi_k = \sum_{i=0}^{n-1} T_i, n = 1,2, \dots \dots T_o = 0 \quad (14)$$

The $q(t)$ is given by (15).

$$q(t) = \sum_{i=-\infty}^{\infty} T_i, j_k (t - \xi_k) \quad (15)$$

Where $j_k(t)$ is shown in (16).

$$j_k(t) = \begin{cases} 1, & for\ \xi_k \leq t \leq \xi_k + \alpha_k \\ 0, & otherwise \end{cases} \quad (16)$$

3.2. Pseudo-random number constructed by linear feedback shift register

Initially, the pseudo-random count is initiated with the support of a linear feedback shift register (LFSR) then the random switching pulse has been generated. The LFSR contains several shift registers to perform a linear function to adjust each rising edge of the clock pulse with the help of a logic gate called XOR. Seeds and taps are respectively called for the input initial stage and bit positions. Random numbers (2n-1) are composed by using LFSR. Here, the number of flip-flops is pointed out by n. when the LFSR has been locked, a sequence is generated from the initial stage. It is deterministic and finite [23]–[25].

3.3. Procedure to generate DCPWM using field programmable gate array (FPGA) controller

The RCFMFD scheme is applied to the LFSR to generate chaotic PWM pulses with the help of an FPGA controller board. The coding has been done with help from Verilog using Xilinx Design Suite 14.1 software. The generated pulse has been verified through the ISim simulator. The following steps describe the chaotic pulse generation using the RCFMFD scheme with a field programmable gate array (FPGA) controller.
Step 1: Seed values moved to the LFSR at each positive edge clock pulse.
Step 2: Random value 2n-1 generated by using XOR gates for a specific tap.
Step 3: A variable frequency is generated with the help of random values from the LFSR.
Step 4: PWM period and PWM ON are initiated and values are set with ±1/3rd of the switching frequency.
Step 5: PWN ON is calculated from each positive edge of the clock pulse and depends on the duty ratio.
Step 6: Increment the count to ON time by 1 during the clock positive edge. So, F_{sw} is 1.
Step 7: F_{sw} becomes 0 when the PWM ON value exceeds.
Step 8: Again, the counter value is initialized to 1 once PWM ON exceeds.
Step 9: By adding a new value, the PWM period is repeated again.
Step 10: Again step 6 is repeated for the next clock pulse.

4. PROPOSED EMI MITIGATION TECHNIQUE

The proposed EMI mitigation technique for the EPOSLL converter is shown in Figure 4. A line impedance stabilization network (LISN) is used to block EMI from outside sources. Periodic and digital chaotic PWM techniques are applied to that converter, and the results are tabulated for better EMI noise mitigation analysis.

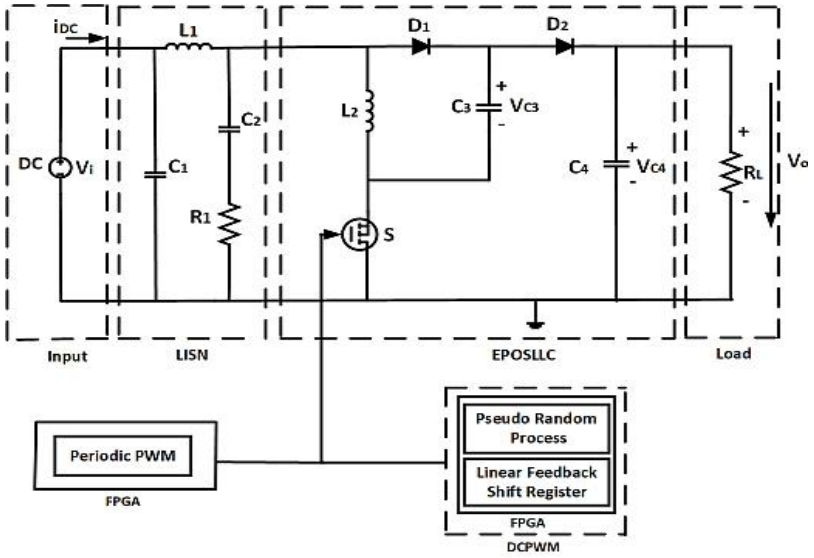

Figure 4. Schematic diagram of proposed EMI mitigation system on EPOSLL converter

4.1. Periodic PWM based EMI mitigation technique

Regulated power supply (RPS) gives the input of 12 V through LISN to the EPOSLL converter and the output of 36 V is obtained with the help of a periodic PWM pulse, which is given to the gate of the MOSFET. The Verilog code has been programmed to generate a periodic pulse which has been given to the gate terminal with the help of the spartan FPGA 3E controller board by interfacing with the TLP350 driver board. However, in the simulation, a Xilinx block set was utilized to deliver pulses to the MOSFET gate terminals, and the corresponding waveforms were captured using a scope.

4.2. Digital chaotic PWM based EMI mitigation technique

The 12 V is given as input to the EPOSLL converter through an RPS employing LISN. Through the voltage lifting technique, the EPOSLL converter circuit converts 12 V DC to 36 V DC. Due to the fast-switching process, EMI has been conducted to increase the gain. The chaotic PWM pulses have been generated using an FPGA, as already discussed in section 3 and the chaotic pulses have been applied to the gate terminal of the MOSFET through the driver board TLP350 to suppress the EMI in the EPOSLL converter.

5. SIMULATION RESULTS AND DISCUSSION

5.1. Periodic pulse width modulation

Figures 5(a) to 5(d) explain the simulated output waveforms of an EPOSLL converter for the specification of V_{in}=12 V, V_o=36 V, k=0.5, and switching frequency (F_{sw}) = 200 kHz using MATLAB R2020a. During, boost operation of EPOSLL converter, the spikes are produced at an initial stage, and the respected spectral peaks are also analyzed from the output voltage of the power spectral density waveform. The common-mode and differential- mode EMI noise was also obtained. The EMI test specifications are shown in Table 1.

5.2. Digital chaotic pulse width modulation

The DCPWM switching carrier pulses are triggered with the help of chaotic mapping using MATLAB Simulink 2020a to suppress the spectral peak values by giving random values of 1/3rd of the primary switching frequency and maintaining the duty cycle constant for the constant output voltage. So, the frequency range between 264 to 142 kHz has been triggered and given to the power MOSFET in the converter circuit. Figures 6(a) to 6(d) show the various waveforms obtained from the DCPWM approach.

Table 1. Specifications of EPOSLL converter EMI test

Parameters	Symbol	Value
Input voltage	V_{in}	12 V
Output voltage	V_o	36 V
Inductors	L_1, L_2	100 µH
Capacitors	C_1, C_2, C_3, C_4	30 µF
Switching frequency	Fs	200 kHz
Resistors	R_1, R_L	50 Ω
Power output	P_o	40 W
Duty cycle	d	0.5

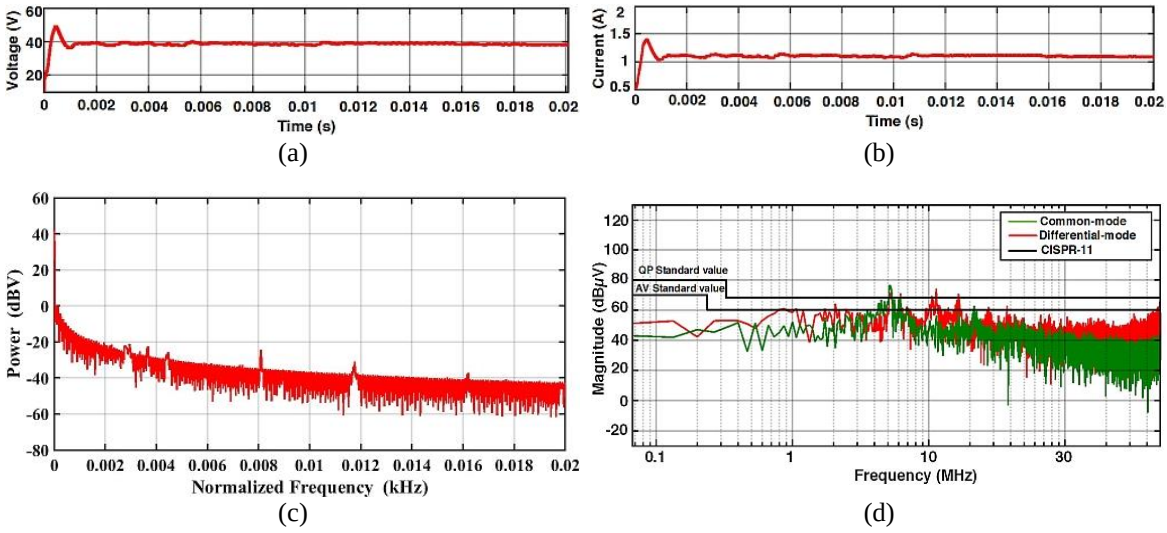

Figure 5. Periodic PWM process waveforms V_{in}=12 V, V_o=36 V, k=0.5: (a) output voltage, (b) output current, (c) PSD calculation from V_o, and (d) differential-mode and common-mode noise

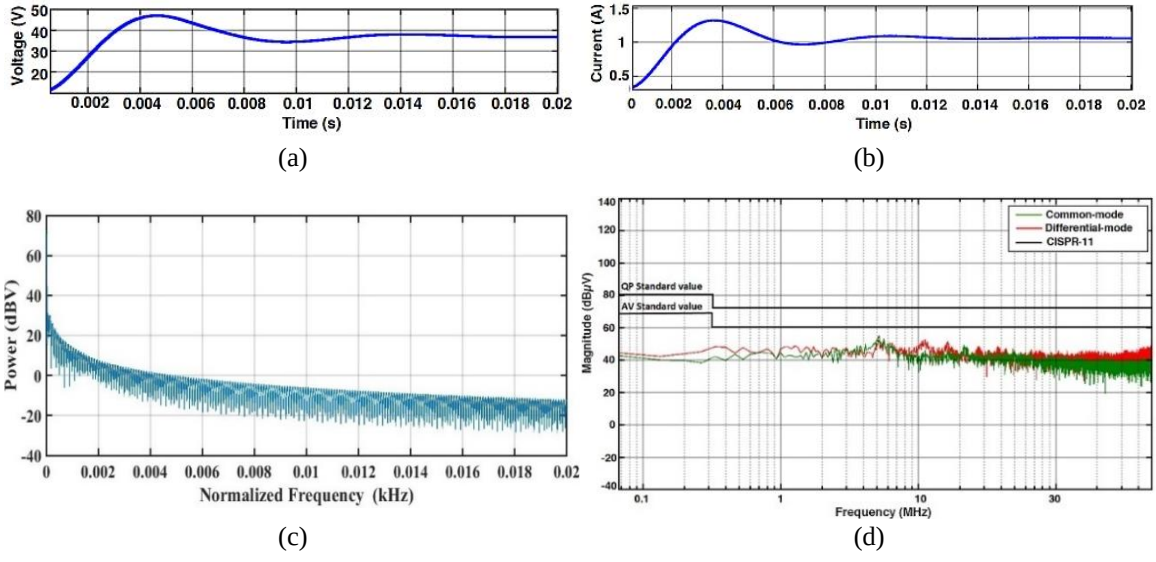

Figure 6. DCPWM process waveforms V_{in}=12 V, V_o=36 V, k=0.5: (a) output voltage, (b) output current, (c) PSD calculation from V_o, and (d) differential-mode and common-mode noise

6. EXPERIMENT IMPLEMENTATION AND RESULT DISCUSSION

6.1. Hardware setup and its working process

In this work, an EPOSLL converter hardware prototype has been fabricated. The hardware setup incorporates RPS, LISN, a Spartan 3E FPGA controller board, an optocoupler based driver circuit with EPOSLL converter, mixed signal oscilloscope (MSO), and end up with the load. Spartan 3E XC3S500E FPGA

board of 50 MHz is interfaced with software Xilinx ISE design suit 14 to promote periodic as well as chaotic pulses, and the developed pulses, are shown in Figures 7(a) and 7(b), are given to the driver circuit of the EPOSLL converter in periodic PWM and DCPWM methods. After the effective buildout of the hardware prototype, the EPOSLL converter has been tested with the designed parameters of V_{in}=12 V, V_o=36 V, k=0.5, and F_{sw}=200 kHz. The FFT of the output voltage is obtained from the duty cycle of 0.5, with input and output voltages of 12 and 36 V, respectively, as shown in Figures 7(c) and 7(d). Figure 7(e) depicts the entire hardware setup.

6.2. Hardware results comparison

During the periodic PWM method, the average peak noise is -48.41 dBV, which is nearly 3.79 mV as by implementing DCPWM, it is observed that the average peak noise is -59.64 dBV is equal to 1.04 mV. Through this observation, the suppression of 9 dBV (2.81 V) of conducted noise, has been achieved with the DCPWM technique compared to the periodic PWM technique. From Figures 7(c) and 7(d), P, Q, and R are the three different sample values that are noted for the effective analysis of DCPWM compared to the periodic PWM method as shown in Figure 7(f) and Table 2.

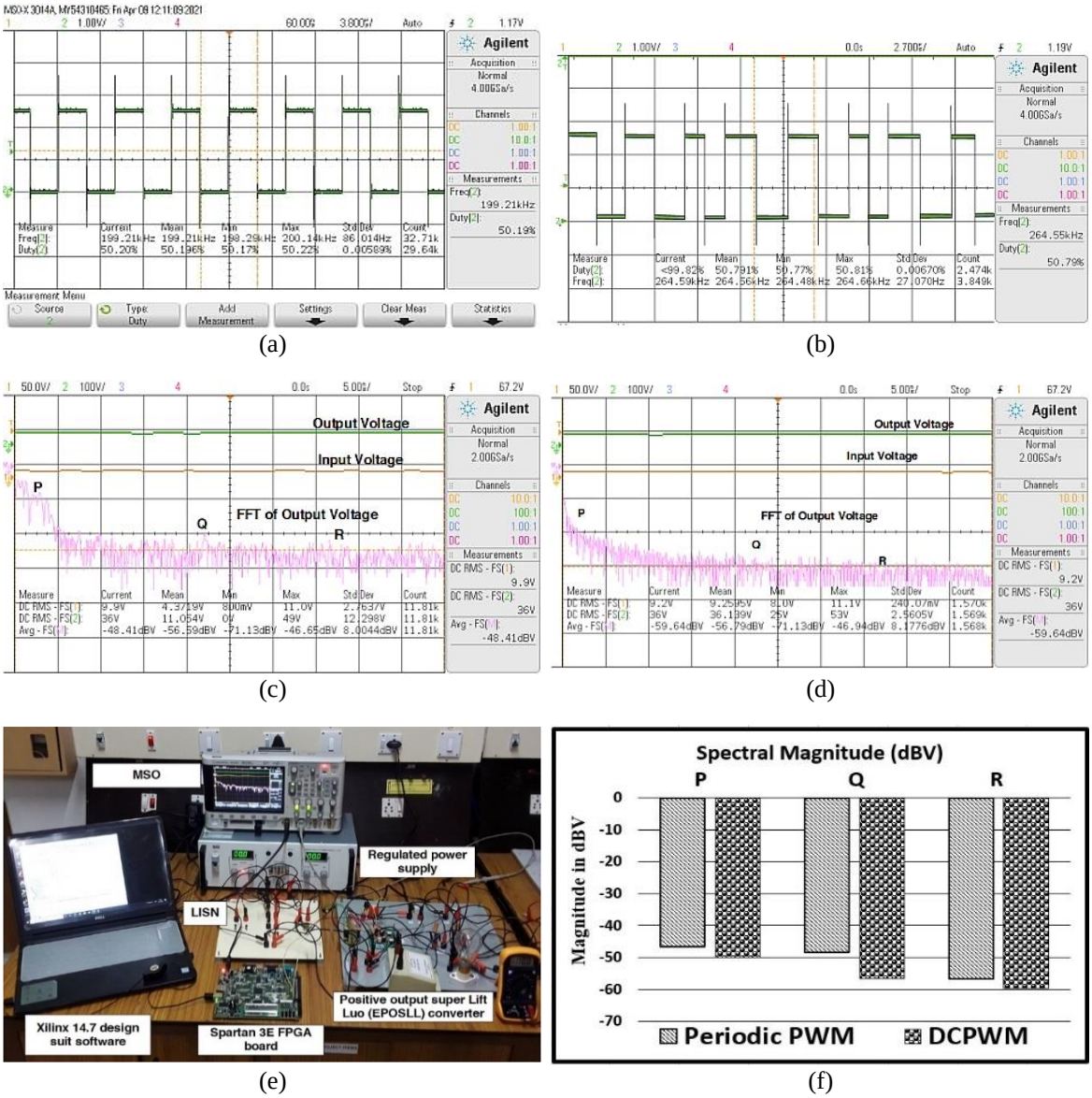

Figure 7. Hardware output for duty cycle k=0.5, F_{sw}=200 kHz, V_o=36 V: (a) periodic pulses, (b) digital chaotic pulses, (c) periodic PSD waveform, (d) digital chaotic PSD waveform, (e) hardware setup, and (f) power spectrum comparison chart

Table 2. Power spectrum comparison

	Magnitude levels (dBV)		
	P	Q	R
Periodic PWM	-46.65	-48.41	-56.59
DCPWM	-49.94	-56.64	-59.64

7. CONCLUSION

In this work, an EPOSLL DC-DC converter prototype model has been fabricated and verified with various input values to calculate the EMI mitigated level with the expected output value. Spartan 3E FPGA controller has been handled for the generation of periodic as well as chaotic pulses as an input to the MOSFET gate terminal through a TLP350 driver board. From that observation, the peak of PSD is suppressed better in the DCPWM method compared to the periodic PWM method. It has been calculated that 9 dBV (2.81 V) of conducted EMI noise has been weakened. Hence, the DCPWM methodology gives better results than other conventional methods for conducting EMI noise suppression platforms on EPOSLL DC-DC converters in EV applications.

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