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An efficient ultra-wideband digital transceiver for wireless applications on the field-programmable gate array platform

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ABSTRACT

The ultra-wideband (UWB) technology is a promising short-range communication technology for most wireless applications. The UWB works at higher frequencies and is affected by interferences with the same frequency standards. This manuscript has designed an efficient and low-cost implementation of IEEE 802.15.4a-based UWB-digital transceiver (DTR). The design module contains UWB transmitter (TX), channel, and UWB-receiver (RX) units. Convolutional encoding and modulation units like burst position modulation and binary phase-shift keying modulation are used to construct the UWB-TX. The synchronization and Viterbi decoder units are used to recover the original data bits and are affected by noise in UWB-RX. The UWB-DTR is synthesized using Xilinx ISE® environment with Verilog hardware description language (HDL) and implemented on Artix-7 field-programmable gate array (FPGA). The UWB-DTR utilizes less than 2% (slices and look-up table/LUTs), operates at 268 MHz, and consumes 91 mW of total power on FPGA. The transceiver achieves a 6.86 Mbps data rate, which meets the IEEE 802.15.4a standard. The UWB-DTR module obtains the bit error rate (BER) of 2×10^{-4} by transmitting 105 data bits. The UWB-DTR module is compared with similar physical layer (PHY) transceivers with improvements in chip area (slices), power, data rate, and BER.

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1. INTRODUCTION

In recent years, ultra-wideband (UWB) technology has been used in most short-range wireless communication applications. UWB system uses the IEEE 802.15.4a standard as one of the efficient interface mechanisms for low-data-rate transmission with precision-ranging features in wireless personal area networks (WPANs). The IEEE introduced the first 802.15.4a 2006 for low-data-rate WPANs and later updated it as IEEE 802.15.4-2015 [1]. The IEEE used another UWB standard IEEE 802.15.6-2012, for wireless body area networks (WBANs). The UWB standards are commonly used in impulse radio (IR) UWB physical layer (PHY) and frequency modulation (FM) UWB PHY's. Using UWB and other technology, short-range communication with a specific data rate and frequency band range is established. With a frequency band of 10.6 GHz, the IR-UWB (IEEE 802.15.4-2015) enables a data rate of 0.11-27 Mbps, and the IR-UWB (IEEE 802.15.6-2015) may provide data rates of 0.49 to 15 Mbps. The FM-UWB (IEEE 802.15.6-2012) enables a 0.25 Mbps data rate, and multiband (MB)-UWB enables a data rate of up to

480 Mbps. The Zigbee (IEEE 802.15.4) supports 0.02 to 0.25 Mbps data rates with a frequency of 868 MHz to 2.5 GHz. The Bluetooth technology (IEEE 802.15.1) supports data rates up to 1-24 Mbps and operates at 2.4 and 5 GHz bands [2].

The UWB system is standardized and compatible with the PHY, medium access control (MAC), and other upper layers. The IEEE 802.15.4z is enhanced from IEEE 802.15.4 to improve measurements' security and accuracy range. The IEEE UWB PHY is operated in two modes: high-rate pulse (HRP) and low-rate pulses (LPR). Most of the system is utilized in HPR mode rather than LPR because LPR-based UWB PHY is incompatible with other IEEE standards [3]. The IR-UWB is a single-band carrier system that transmits input streams directly into waveforms, covering the entire spectrum. The IR-UWB has many advantages: low-cost, multiple access, low power spectral density, lower-power consumption, high data rate, fading removal feature, channel capacity improvements, higher multi-path resolution, and availability in the form of wide unlicensed bands [4]. The frequency-shifted reference (FSR) based UWB transceiver (TR) is introduced to remove the delay elements in UWB TR. However, the complexity of the FSR TR is high and offers moderate performance. So, the code shifted reference (CSR) based UWB TR is introduced to separate the data pulses sequence from reference sequences through time-shift features or Walsh codes sequences [5], [6]. The security enhancement [7] and advanced error correction codes (ECC) mechanism [8] for bit error rate (BER) improvements have been incorporated in recent times to improve the performance of the UWB system. UWB system is mainly used in most of the wireless personal area network (PAN) and body area network (BAN) applications apart from that, the healthcare system, high-speed chip-to-chip communications, Internet of things (IoT) applications, network bio-sensors applications, radio-frequency identification (RFID) system, and industrial and scientific applications [6]–[10]. The UWB-based monopole antenna [11] with super compact features is designed for small IoT devices. This monopole antenna operates up to 12.56 GHz at a return loss of -10 dB. The modified circular printed monopole (MCPM) antenna [12] is designed with ultra-miniaturized features for UWB applications. The MCPM antenna operates up to 11 GHz and achieves a peak gain of 3.2 dB.

In this manuscript, the IEEE 802.15.4a-based efficient UWB digital transceiver (DTR) system architecture on the field-programmable gate array (FPGA) platform using burst position modulation (BPM) with binary phase-shift keying (BPSK) and Viterbi decoding techniques. The contribution of the proposed work is listed as follows.

- The transmitter and receiver units use the digital frequency synthesizer (DFS) module generation for in-phase and quadrature phase (Q) generation. The DFS offers less area and improves the system performance than the oscillator-based signal generation.
- The UWB transceiver supports the range of 3 to 10 GHz frequency bands by configuring the data bits in the physical service data unit (PSDU).
- The obtained data rate met the IEEE 802.15.4a standards and was used further in wireless PAN applications.
- The proposed UWB-TR offers low-cost FPGA implementation, with less chip area resources (slices), utilization of, and less power consumed, and also works at a moderate data rate with better BER.

The manuscript's organization is as follows: the recent works of the UWB architectures are discussed in section 1. The proposed UWB-DTR hardware architecture with a detailed explanation of architectures is in section 2. Section 3 discusses the proposed work simulation, synthesis results, and comparative discussion. Lastly, it concludes the overall work with improvements and highlights its future scope in section 4.

The existing PHY TR architectures and their performance metrics for various applications with different platforms are explained as follows. Santhi *et al.* [13] presented the multi-band (MB)-based orthogonal frequency division multiplexing (OFDM) UWB TR with asynchronous pipelined architecture on the FPGA platform. The transceiver module used fast Fourier transformation and Viterbi decoding architecture to speed up the system. The architecture consumed more chip resources, including 48 digital signal processor (DSP) elements. A pulse position modulation (PPM) based UWB baseband TR on both software (MATLAB) and hardware (FPGA) platforms [14] could achieve up to 10^{-3} BER on the hardware platform. An application-specific integrated circuit (ASIC) implementation of the IR-UWB-based band TR [15] was interfaced with the analog front-end (AFE) module via a serial peripheral interface (SPI). The work investigated an ASIC device's chip resources and power consumption to know the performance realization. The system consumed 120 mW dynamic power with a 2,264 mm^2 area on-chip. Olonbayar *et al.* [16] presented 802.15.4a-based multi-rate IR-UWB baseband TR designed and implemented on the FPGA platform. The design used a PPM-BPSK modulation scheme and analyzed the baseband's different data rates. The data detection was achieved using hamming codes. The transmitted and received burst signals were varied with 160 kHz. The same architecture was implemented on the ASIC environment using 250 nm technology [17].

Shanthi and Krishnamurthi [18] presented a 14-band frequency synthesizer for the MB-OFDM UWB TR system. The delay-locked loop (DLL) based frequency synthesizer reduced the interference issues and provides an efficient signal to improve the BER. Costa [19] presented the UWB system designed using the continuous-time binary value (CTBV) approach in an FPGA environment. The work demonstrated the pulse generation and detection of FPGA and analyzed the propagation delay and line distance estimation. The UWB TR worked at 5.5 Mbps with a minimum load distance of 26 m. The IR-UWB TR with ultra-low-power features for wireless sensor networks (WSN) designed on the ASIC platform [20] used the on-off keying (OOK) technique for modulation and demodulation. The system achieved 3.86 mW of total power on 65 nm technology and is used further for WSN-based health monitoring applications. Gimeno *et al.* [21] presented the IR-UWB TR for high-speed chip-to-chip communications in ASIC environments. The system used OOK, PPM, and PPM2 modulation techniques and analyzed the BER versus signal to noise ratio (SNR). The system used a radio-frequency (RF) front-end and analog baseband for data transmission and reception. The work achieved 15 mW of power with an energy efficiency of 6 pJ/bit at 2.5 Gbps.

An adaptive beaming method was adopted for the IR-UWB TR system by Qiu *et al.* [22]. The transmitter (TX) mainly contained injected locked voltage-controlled oscillator (IL-VCO) and delta-sigma delay locked-loop (DLL) for TX signal generation. The adaptive receiver (RX) unit used beamforming with a self-tuning mechanism for detecting correct bits. The TX and RX units consumed 67 and 151 mW of total power using 18 nm complementary metal-oxide-semiconductor (CMOS) technology. A differential code shifted reference (DCSR) encoding and decoding mechanism was designed by Jayaprakash and Samundiswary [23] for UWB-TR. The DCSR module utilized less area and power than the CSR-based FPGA system. Kopta and Enz [24] presented the frequency modulation-based UWB TR for IoT applications. The TX consumed 575 µW of power, while RX consumed 267 µW while transmitting and receiving 100 Kbps signals. Tantiparimongkol and Phasukkit [25] presented the IR-UWB pulse generation unit for obstacle human detection on the FPGA platform. The design used a digital clock manager, delay tree, and edge combiner for pulse generation. The system achieved a bandwidth of 2.07 GHz with a pulse duration of 540 ps. Wang *et al.* [26] presented a detailed review of the recent UWB TR system architectures and their applications. The IR-UWB and FM-UWB discussed in detail concludes that the IR-UWB TR is promising for secured IoT mobile applications in the future.

2. PROPOSED UWB DIGITAL TRANSCEIVER

The UWB PHY transceiver is designed per IEEE 802.15.4a [27]. The UWB PHY operates in sub gigahertz (250 to 750 MHz) and 3 to 10 GHz bands. The low-band high-rate pulse (HRP) UWB works with a frequency band of 3.244 to 4.742 GHz, and the high-band HRP UWB performs with a frequency band of 5.944 to 10.234 GHz. The HRP UWB system-based physical protocol data unit (PPDU) mainly contains the preamble and data unit parts). The representation of the UWB PPDU format [25] is shown in Figure 1. The preamble contains the preamble and the start of the frame delimiter (SFD) as a synchronization header (SHR). The data unit includes the physical layer header (PHR) and PSDU. The UWB digital transceiver architecture is represented in Figure 2 as part of PSDU. It contains TX, additive white Gaussian noise (AWGN) as a channel, and RX units.

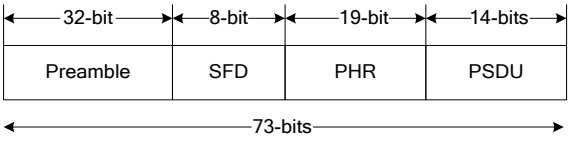

Figure 1. UWB PPDU format

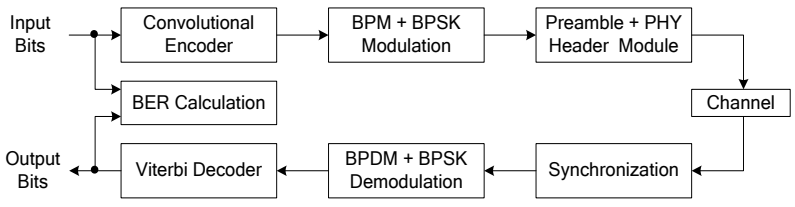

Figure 2. Hardware architecture of the UWB DTR module

2.1. UWB transmitter unit

The UWB transmitter mainly includes a convolutional encoder (CE), BPM, BPSK modulation, preamble, and PHR data units. The CE is mainly performing the encoding operation with generator polynomials $C_0 = [101]_2$ and $C_1 = [111]_2$. The code rate of CE is ½ with constraint length (K) three. Initially, all the states in CE are set to zero. Based on PPDU data transmission, The C_0 and C_1 bits will be generated. The CE hardware architecture contains a 3-bit shift register and two XOR operations. The input data bits are fed as the stream of data bits in CE. These bits are convolved to output bits based on encoding logic. The two output bits are depending previous input bits stored in the shift register and the present input bit. These two C0 and C1 bits are parity and systematic, respectively. The BPM unit receives the parity bit, and the BPSK unit receives the systematic bit for further modulation.

The hardware architecture of the BPM and BPSK modulation is represented in Figure 3. The BPM unit mainly contains a DFS unit, sawtooth wave generation unit, and multiplexor unit shown in Figure 3(a). The DFS produces the sinusoidal signal, and a 10-bit counter generates the sawtooth signal. The sawtooth signal is subtracted from the DFS signal to produce the burst position signal. The parity bit from the CE is used in the multiplexor, which acts as a select line. If the parity bit is one, the subtracted output is considered the final BPM signal; otherwise, the inverted output (subtracted) is regarded as a 1-bit BPM signal. The BPSK modulation hardware architecture is illustrated in Figure 3(b). It mainly contains DFS, data flip-flop, multiplexor, and adder units. The DFS unit produces a sinusoidal signal, considered the in-phase (I), and an inverted sinusoidal signal, which is viewed as a Q signal. The systematic bit from CE is used as a select line in the multiplexor. If the systematic bit is one, then the in-phase (I) is considered; otherwise, the Q signal is considered with delay. The I and Q signals are added to generate the 12-bit BPSK modulated signal.

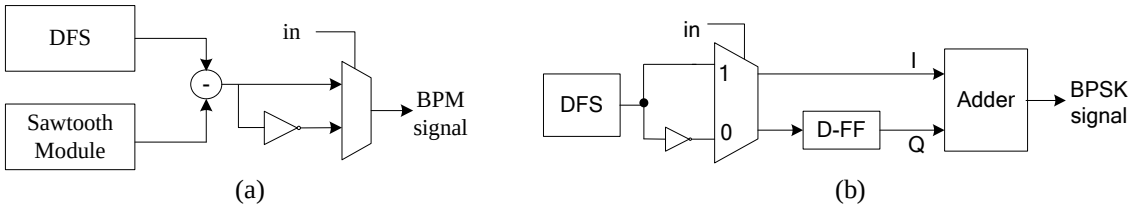

Figure 3. The architecture of (a) BPM and (b) BPSK modulation units used in UWB-TX

The preamble and SFD are generated based on the IEEE 802.15.4a standard [25]. The preamble is generated using 31-bit ternary codes as code sequences. The code index is one, and the supported UWB channel number (0, 1, 8, 12) is used to select the code sequence. The 8-bit SFD bits are generated based on spread codes and set as "48" in hexadecimal format. The PHR format is illustrated in Figure 4. The 19-bit PHR contains a 2-bit data rate, 7-bit frame length, 1-bit ranging packet, 1-bit header extension, 2-bit preamble time, and 6-bit check bits. The data rate is set with "01" for UWB-compliant PHY implementation. The 7-bit frame length indicates the number of octants used in PSDU, which requests the system to transmit. The ranging packet is set with 0. The header extension bit is set to 0 for future extensions. The preamble length in SHR is represented by preamble duration bits and default set with '01". The 6-bit check bits are used to detect the errors caused by noise. After the calculation, the 19-bit PHR obtains the value of "40C56" in hexadecimal format. Finally, the UWB Transmitter contains the concatenation of the 32-bit Preamble, 8-bit SFD, 19-bit PHR, 1-bit BPM, 12-bit BPSK modulated signal, and 1-bit unused bit to form the 73-bit transmitted signal.

2-bits	7-bits	1-bit	1-bit	2-bit	6-bit
Data rate	Frame Length	RP	HE	Preamble Time	Check Bits

Figure 4. PHR format [25]

2.2. UWB receiver unit

The UWB receiver unit has a synchronization unit, burst position demodulation (BPDM), BPSK demodulation unit, and Viterbi decoder (VD) units. The UWB receiver receives the 73-bit corrupted data and

performs the synchronization, de-mapping, and decoding operations to return the original data bit sequences. The received 73-bits are decomposed. Instead, the least significant bit (LSB) 13 bits (data part) is used for de-mapping with synchronization. The hardware architecture of the BPSK demodulation and BPDM units is illustrated in Figure 5. The synchronization mechanism is incorporated in both BPDM and BPSK demodulation to recover original bits from corrupted data. The BPSK demodulation contains the DFS, two delay units, and a comparator. The generated DFS (Q) signal is inverted first and later delayed with two flip-flops to maintain synchronization between the received data and the global clock. The comparator compares the 12-bit data with the delayed Q signal to obtain the BPSK demodulated signal (out) shown in Figure 5(a).

The burst position signal is generated from DFS and sawtooth signal. The burst position signal and received 1-bit data are delayed one clock cycle to maintain synchronization with the global clock. The BPDM signal is generated by comparing the delayed received bit with the delayed burst position signal, represented in Figure 5(b). These de-mapped signals (1-bit BPSK demodulated signal and 1-bit BPDM signal) are used further in the VD to recover the final data bits with a decoding mechanism.

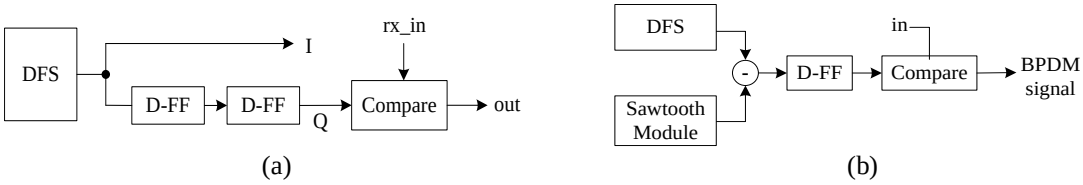

Figure 5. The architecture of (a) BPSK demodulation and (b) BPDM units used in UWB-RX

The hardware architecture of the VD is illustrated in Figure 6. The VD unit mainly contains the counter, branch metric unit (BMU), add-compare-select unit (ACSU), traceback unit (TBU), and shift register. The BMU received the 2-bit and was used to calculate the branch metrics. The hard decision-based VD is used for branch metric (BM) calculation. The BMU performs the essential XOR operation using received and expected data bits and counts the differed bits to calculate the Hamming distance. The ACSU is also called a path metric unit (PMU). The ACSU receives the BM data and performs the path metric calculation using add, compare, and select operations.

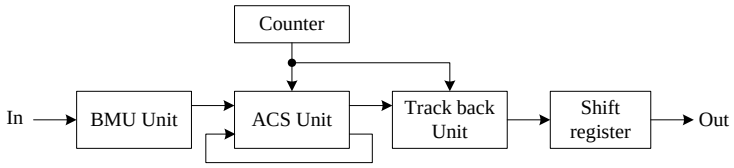

Figure 6. Viterbi decoder hardware architecture

In the VD design, 8 ACSU's are used to find the decision bits. The received 2-bit BM data are added with new path metric data to find the lower and upper data. The lower data bits are compared with the upper bits to see the new path metric data and find the decision. Each ACSU produces the 2-bit decision bits. So, 16 decision bits are used further in the TBU of the trellis state. The TBU receives the 16-bit decision values with a counter to trace the best possible path. The TBU contains the memory unit to store the decision bit's history from the ACSU. The decision bits are stored in a memory unit based on the counter values. The 16 stored memory values act as decision vectors for each trellis state at each time (clock cycle). The decision vector is used further to reconstruct the best possible trellis path. Lastly, the shift register received the TBU data and shifted right to produce the correct 1-bit output. The received 1-bit data from VD and 1-bit input data are compared to realize the BER. The input data is delayed based on latency compared with the received data. If both the data bits are equal, there is no error; else error bit will be produced.

3. RESULTS AND DISCUSSION

The UWB digital transceiver architecture results are discussed in this section. The UWB-DTR module is designed using Verilog hardware description language on Xilinx ISE® 14.7 environment and

implemented on Artix-7 (XC7A100T-3CSG324) FPGA. The simulation results are carried out using ModelSim 10.5 simulator. The UWB TX, AWGN channel, and UWB RX units are integrated to form the UWB DTR module. The simulation results of the UWB-DTR module are illustrated in Figure 7. The global clock (*clk*) is activated with an active-low reset (*rst*). The 1-bit data input (*din*) stream is feeding in a sequence. Based on UWB-DTR module operations, The 1-bit data output (*dout*) is obtained with a delay of 39 clock cycles. To estimate the BER, the delayed input (*delayed_din*) is introduced to match the received 1-bit *dout*. If the delayed input and received output (*dout*) are equal, the error signal will be low; otherwise, the error signal will be high. The error counter (*error_count*) is introduced to estimate the unmatched bits. The main counter forecasts the number of input bits to be transmitted. The 8-bit noise is added in every clock cycle with transmitted output.

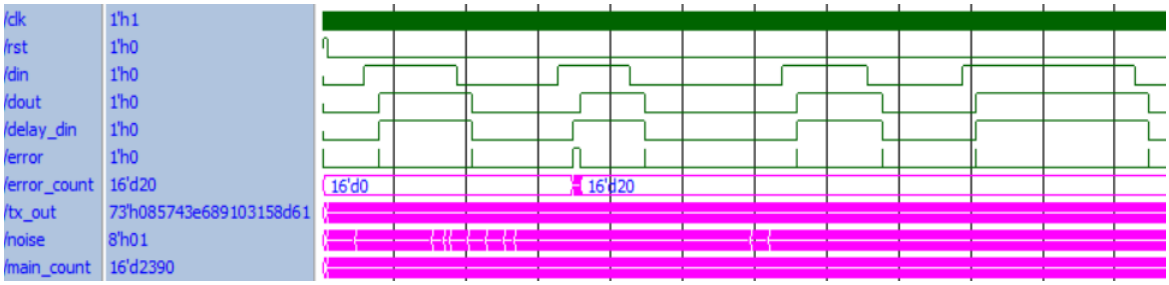

Figure 7. Simulation results of the UWB-DTR module

The UWB-DTR module resource utilization results after synthesis on Artix-7 FPGA, tabulated in Table 1. The UWB-TX unit has 74 slices and 155 look-up tables (LUTs), operates at 268.17 MHz, and uses 87 mW of total power. Similarly, The UWB-RX unit has 166 slices and 562 LUTs, operates at 268.18 MHz, and uses 87 mW of total power. The integrated UWB-TR module utilizes 209 slices and 876 LUTs, operates at 267.37 MHz, and consumes 91 mW of total power on Artix-7 FPGA. Using an XPower analyzer, the total power is estimated based on a frequency of 31.2 MHz.

Table 1. Resource Utilization results for UWB-DTR module on Artix-7

Resources	UWB TX	UWB RX	UWB TR
Slices	74	166	209
LUTs	155	562	876
Max. Frequency (MHz)	268.17	268.182	267.376
Total power (mW)	87	87	91

The UWB-DTR module performance results include latency in terms of clock cycles (CC), throughput (Mbps), hardware efficiency (Kbps/Slice), BER, and percentage error efficiency are tabulated in Table 2. The latency of 39 clock cycles is obtained after receiving the first output bit using the UWB-RX unit and is analyzed using the ModelSim simulator. The throughput is estimated based on input bits, obtained maximum frequency, and latency. So, throughput (*Mbps*)=(*input width*max. frequency*)/*latency*. The UWB-DTR achieves a 6.86 Mbps throughput or data rate. The hardware efficiency of the UWB-DTR module achieves 31.5 Kbps/Slice. The BER is calculated based on the number of errors obtained by the number of bits transmitted. The total number of error bits is 20 for 100,000 bits. So UWB-DTR module achieves a BER of 2×10^{-4} with a system efficiency of 99.98 % for 10^5 bits.

Table 2. Performance results for the UWB-DTR module

Latency (CC)	Throughput (Mbps)	Efficiency (Kbps/Slice)	BER	System Efficiency
39	6.86	31.5	2×10^{-4}	99.98 %

The resource utilization of the UWB-DTR (submodules) on Artix-7 is represented in Figure 8. The BPSK modulator and VD unit consume more chip area resources (slices and LUTs) on the sides of the UWB-TX and UWB-RX units on the Artix-7 Chip. The CE and VD unit obtain better operating frequencies of 1519.5 and 350.128 MHz on the UWB-TX and UWB-RX units, respectively, on the Artix-7 chip.

The comparison of the different PHY transceivers with the proposed UWB-DTR on hardware platforms is tabulated in Table 3. The PHY TR module selected IEEE standards, modulation, or technique adopted and obtained performance metrics like slice, frequency, power, data rate, and BER parameters on selected FPGAs that are considered for comparative analysis. The proposed module combines BPM with BPSK modulation for improved performance metrics than the different PHY TR techniques. The model drive architecture [28] is incorporated into the UWB-DTR module to improve the reliability features.

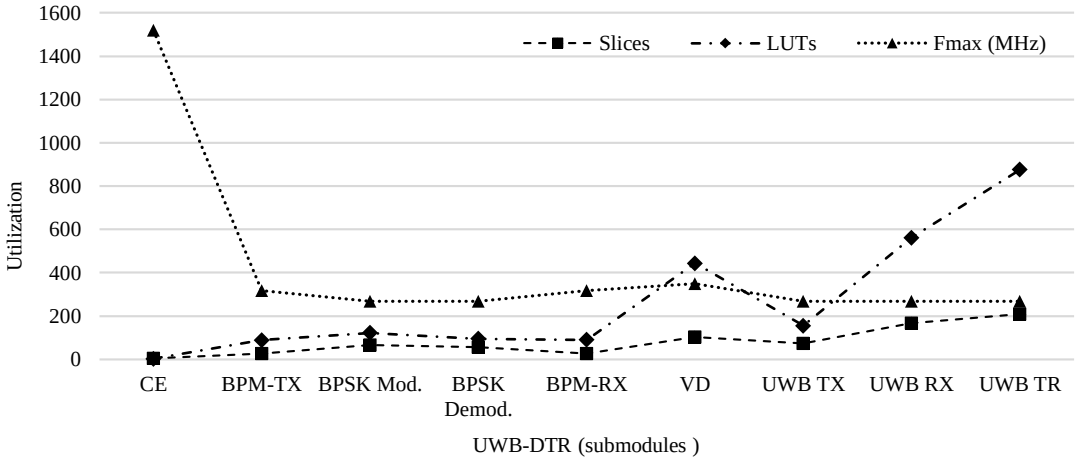

Figure 8. Resource utilization of the UWB-DTR (submodules) on Artix-7

Table 3. Comparative results for different PHY Transceivers on the FPGA platform

Reference Designs	PHY TR	IEEE Std.	Techniques	FPGA	Slices	Freq. (MHz)	Power (mW)	Data rate (Mbps)	BER
[29]	IR-UWB	802.15.4a	PPM	Virtex-4	1012	100	NA	NA	NA
[30]	IR-UWB	802.15.4a	PPM	Spartan-3	1821	134	NA	3	Up to 10^{-3}
[31]	IR-UWB	802.15.4 2015	MPPM	Virtex-6	2711	120	NA	2	Up to 10^{-3}
[32]	NB-PHY	802.15.6	BCH	Virtex-6	2668	100	117	0.971	Up to 10^{-3}
[33]	IR-UWB	802.15.4a	DWPT	Virtex-7	557	99	514	NA	NA
[34]	HB-PHY	802.15.6	Walsh	Artix-7	1084	32	114	6	Up to 10^{-3}
[35]	PHY	802.15.4	O-QPSK	Artix-7	224	270	171	4.3	$<10^{-4}$
Proposed	UWB- DTR	802.15.4a	BPM + BPSK	Artix-7	209	268	91	6.86	$2x10^{-4}$

4. CONCLUSION AND FUTURE WORK

In this manuscript, the IEEE 802.15.4a-based UWB-DTR hardware architecture is designed and implemented on Artix-7 FPGA for WPANs applications. The UWB-DTR mainly offers low-cost implementation, consumes low power, and operates at a better data rate with less BER. The UWB-DTR used BPM-BPSK modulation techniques with a Viterbi decoding mechanism to transmit and receive data streams in sequence. The timing synchronization mechanism is introduced on the UWB-RX side to recover the corrupted data using the Viterbi decoding method. The simulation results prove that the designed architecture receives the original data sequence within 39 clock cycles with minimal error. The UWB-DTR system utilizes <2% chip resources at 268 MHz by consuming 91 mW of total power on Artix-7 FPGA. The UWB-DTR system achieves a data rate of 6.86 Mbps, matching the IEEE 802.15.4a standard. The UWB-DTR system achieves the BER of 2×10^{-4} by transmitting 10^5 input data bits. Compared with similar physical layer transceivers, the UWB-DTR module outperforms them in chip area (slices), power, data rate, and BER. The UWB-DTR module will be incorporated with a security algorithm to improve the system's security and performance metrics.

REFERENCES

[1] R. Chávez-Santiago, I. Balasingham, and J. Bergsland, "4 ultrawideband technology in medicine: A survey," *Journal of Electrical and Computer Engineering*, vol. 2012, pp. 1–9, 2012, doi: 10.1155/2012/716973.

[2] V. Niemela, J. Haapola, M. Hamalainen, and J. Iinatti, "An ultra wideband survey: Global regulations and impulse radio research based on standards," *IEEE Communications Surveys & Tutorials*, vol. 19, no. 2, pp. 874–890, 2017, doi: 10.1109/COMST.2016.2634593.

[3] D. Coppens, A. Shahid, S. Lemey, B. Van Herbruggen, C. Marshall, and E. De Poorter, "An overview of UWB standards and organizations (IEEE 802.15.4, FiRa, Apple): Interoperability aspects and future research directions," *IEEE Access*, vol. 10, pp. 70219–70241, 2022, doi: 10.1109/ACCESS.2022.3187410.
[4] R. Hazra and A. Tyagi, "A survey on various coherent and non-coherent IR-UWB receivers," *Wireless Personal Communications*, vol. 79, no. 3, pp. 2339–2369, Dec. 2014, doi: 10.1007/s11277-014-1988-4.
[5] H. Nie and Z. Chen, "Performance evaluations for differential code-shifted reference ultra-wideband (UWB) radio," in *2009 IEEE International Conference on Ultra-Wideband*, Sep. 2009, pp. 274–278, doi: 10.1109/ICUWB.2009.5288719.
[6] H. Nie and Z. Chen, "Code-shifted reference transceiver for impulse radio ultra-wideband systems," *Physical Communication*, vol. 2, no. 4, pp. 274–284, Dec. 2009, doi: 10.1016/j.phycom.2009.08.004.
[7] M. Ko and D. L. Goeckel, "Wireless physical-layer security performance of UWB systems," in *2010 - MILCOM 2010 Military Communications Conference*, Oct. 2010, pp. 2143–2148, doi: 10.1109/MILCOM.2010.5680483.
[8] J. Sidorenko, V. Schatz, N. Scherer-Negenborn, M. Arens, and U. Hugentobler, "Error corrections for ultrawideband ranging," *IEEE Transactions on Instrumentation and Measurement*, vol. 69, no. 11, pp. 9037–9047, 2020, doi: 10.1109/TIM.2020.2996706.
[9] J. F. Schmidt, D. Neuhold, C. Bettstetter, J. Klaue, and D. Schupke, "Wireless connectivity in airplanes: challenges and the case for UWB," *IEEE Access*, vol. 9, pp. 52913–52925, 2021, doi: 10.1109/ACCESS.2021.3070141.
[10] S. Kueppers, T. Jaeschke, N. Pohl, and J. Barowski, "Versatile 126–182 GHz UWB D-band FMCW radar for industrial and scientific applications," *IEEE Sensors Letters*, vol. 6, no. 1, pp. 1–4, Jan. 2022, doi: 10.1109/LSENS.2021.3130709.
[11] A. J. Abdullah Al-Gburi *et al.*, "Super compact UWB monopole antenna for small IoT devices," *Computers, Materials & Continua*, vol. 73, no. 2, pp. 2785–2799, 2022, doi: 10.32604/cmc.2022.028074.
[12] A. A.-G. Ahmed Jamal, I. Imran Mohd, and Z. Zahriladha, "An ultra-miniaturized MCPM antenna for ultra-wideband applications," *Journal of Nano- and Electronic Physics*, vol. 13, no. 5, pp. 5012–5014, 2021, doi: 10.21272/jnep.13(5).05012.
[13] M. Santhi, S. Tungala, C. Balakrishna, and G. Lakshminarayanan, "Asynchronous pipelined MB-OFDM UWB transceiver on FPGA," in *TENCON 2009 - 2009 IEEE Region 10 Conference*, Nov. 2009, pp. 1–5, doi: 10.1109/TENCON.2009.5396050.
[14] K. S. Mohammed, "FPGA implementation of PPM I-UWB baseband transceiver," in *Proceedings of the European computing conference*, 2009, pp. 663–674.
[15] D. Kreiser and S. Olonbayar, "Design and ASIC implementation of an IR-UWB-baseband transceiver for IEEE 802.15.4a," in *2011 International Conference on Wireless Communications and Signal Processing (WCSP)*, Nov. 2011, pp. 1–6, doi: 10.1109/WCSP.2011.6096880.
[16] S. Olonbayar, D. Kreiser, and R. Kraemer, "Performance and implementation of a multi-rate IR-UWB baseband transceiver for IEEE802.15.4a," in *2013 IEEE International Conference on Ultra-Wideband (ICUWB)*, Sep. 2013, pp. 231–237, doi: 10.1109/ICUWB.2013.6663854.
[17] S. Olonbayar, D. Kreiser, and R. Kraemer, "FPGA and ASIC implementation and testing of IR-UWB baseband transceiver for IEEE802.15.4a," in *2014 IEEE International Conference on Ultra-WideBand (ICUWB)*, Sep. 2014, pp. 456–461, doi: 10.1109/ICUWB.2014.6959025.
[18] T. Shanthi and V. Krishnamurthi, "FPGA based frequency synthesizer for 14-band MB-OFDM UWB transceivers," in *2016 International Conference on Emerging Trends in Engineering, Technology and Science (ICETETS)*, Feb. 2016, pp. 1–4, doi: 10.1109/ICETETS.2016.7603072.
[19] T. d. S. M. Costa, "UWB using programmable logic," Faculdade De Engenharia Da Universidade Do Porto, 2016.
[20] B. Benamrouche, A. Rumeau, and D. Dragomirescu, "Ultra-low power IR-UWB transceiver for wireless sensors network," in *2017 International Semiconductor Conference (CAS)*, Oct. 2017, pp. 285–288, doi: 10.1109/SMICND.2017.8101227.
[21] C. Gimeno, D. Flandre, and D. Bol, "Analysis and specification of an IR-UWB transceiver for high-speed chip-to-chip communication in a server chassis," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 6, pp. 2015–2023, Jun. 2018, doi: 10.1109/TCSI.2017.2765312.
[22] L. Qiu, S. Liu, Z. Fang, and Y. Zheng, "An adaptive beamforming technique for UWB impulse transceiver," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 3, pp. 417–421, Mar. 2019, doi: 10.1109/TCSII.2018.2866614.
[23] A. Jayaprakash and P. Samundiswary, "Design and analysis of differential code shifted reference encoder and decoder for UWB transceiver," in *2018 International Conference on Control, Power, Communication and Computing Technologies (ICCPCCT)*, Mar. 2018, pp. 13–17, doi: 10.1109/ICCPCCT.2018.8574221.
[24] V. Kopta and C. C. Enz, "A 4-GHz low-power, multi-user approximate zero-IF FM-UWB transceiver for IoT," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 9, pp. 2462–2474, Sep. 2019, doi: 10.1109/JSSC.2019.2917837.
[25] L. Tantiparimongkol and P. Phasukkit, "IR-UWB pulse generation using FPGA scheme for through obstacle human detection," *Sensors*, vol. 20, no. 13, p. 3750, Jul. 2020, doi: 10.3390/s20133750.
[26] B. Wang, H. Song, W. Rhee, and Z. Wang, "Overview of ultra-wideband transceivers—system architectures and applications," *Tsinghua Science and Technology*, vol. 27, no. 3, pp. 481–494, Jun. 2022, doi: 10.26599/TST.2021.9010044.
[27] L. S. Committee and Others, "Part 15.4: wireless medium access control (MAC) and physical layer (PHY) specifications for low-rate wireless personal area networks (LR-WPANs)," *IEEE Computer Society*, 2003.
[28] M. El Ayadi, Y. Rhazali, and M. Lahmer, "A proposed methodology to automate the software manufacturing through artificial intelligence (AI)," *Procedia Computer Science*, vol. 201, pp. 627–631, 2022, doi: 10.1016/j.procs.2022.03.082.
[29] C. G. Gavrincea, X. Artiga, A. Moragrega, C. Ibars, and M. di Renzo, "Flexible FPGA-DSP solution for an IR-UWB testbed," in *2009 IEEE International Conference on Ultra-Wideband*, Sep. 2009, pp. 413–417, doi: 10.1109/ICUWB.2009.5288795.
[30] A. Lecointre, D. Dragomirescu, and R. Plana, "Design and hardware implementation of a reconfigurable mostly digital IR-UWB radio," *Romanian Journal of Information Science and Technology*, vol. 11, no. 4, pp. 295–318, 2008.
[31] Y. Shimizu, D. Anzai, and J. Wang, "FPGA implementation of UWB-IR receiver for in-body to out-of-body communication performance evaluation," in *2014 XXXIth URSI General Assembly and Scientific Symposium (URSI GASS)*, Aug. 2014, pp. 1–3, doi: 10.1109/URSIGASS.2014.6930110.
[32] P. Mathew, L. Augustine, D. Kushwaha, V. Desalphine, and A. David Selvakumar, "Implementation of NB PHY transceiver of IEEE 802.15.6 WBAN on FPGA," Jan. 2015, doi: 10.1109/VLSI-SATA.2015.7050452.
[33] C. H. Kizil, C. Diou, C. Tanougast, and D. Singer, "Hardware implementation of UWB-IR transceiver and receiver based on wavelet packet transform for networked bio-sensors," in *2016 International Conference on Bio-engineering for Smart Technologies (BioSMART)*, Dec. 2016, pp. 1–4, doi: 10.1109/BIOSMART.2016.7835608.
[34] M. Park *et al.*, "Low-power, high data-rate digital capsule endoscopy using human body communication," *Applied Sciences*, vol. 8, no. 9, Aug. 2018, doi: 10.3390/app8091414.
[35] S. P. Guruprasad and B. S. Chandrasekar, "Design and implementation of 802.15.4 transceiver for wireless personal area networks (WPANs) on FPGA," *International Journal of Innovative Technology and Exploring Engineering*, vol. 9, no. 3, pp. 2085–2089, Jan. 2020, doi: 10.35940/ijitee.C8926.019320.

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