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An efficient asynchronous spatial division multiplexing router for network-on-chip on the hardware platform

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ABSTRACT

The quasi-delay-insensitive (QDI) based asynchronous network-on-chip (ANoC) has several advantages over clock-based synchronous network-on-chips (NoCs). The asynchronous router uses a virtual channel (VC) as a primary flow-control mechanism however, the spatial division multiplexing (SDM) based mechanism performs better over input traffics over VC. This manuscript uses an asynchronous spatial division multiplexing (ASDM) based router for NoC architecture on a field-programmable gate array (FPGA) platform. The ASDM router is configurable to different bandwidths and VCs. The ASDM router mainly contains input-output (I/O) buffers, a switching allocator, and a crossbar unit. The 4-phase 1-of-4 dual-rail protocol is used to construct the I/O buffers. The performance of the ASDM router is analyzed in terms of lower urinary tract symptoms (LUTs) (chip area), delay, latency, and throughput parameters. The work is implemented using Verilog-HDL with Xilinx ISE 14.7 on artix-7 FPGA. The ASDM router achieves $< 1\%$ chip area and obtains 0.8 ns of latency with a throughput of 800 Mfps. The proposed router is compared with existing asynchronous approaches with improved latency and throughput metrics.

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1. INTRODUCTION

Network-on-chip (NoC) is constructed using hundreds of processing elements (PEs) or cores for multiprocessing system-on-chip (MPSoC) applications. The drawbacks of the bus-based architectures are overcome with NoC architecture with better interconnection solutions. The synchronous NoCs are scalable, fast, and have less area overhead. These synchronous NoCs were designed using electronic design automation (EDA) tools, assuming the timing closure. The leakage and process variation issues are common while constructing the synchronous NoCs using complementary-metal-oxide semiconductor (CMOS) technology [1]. The asynchronous logic and quasi-delay-insensitive (QDI) circuits provide prominent solutions for the above channelings. The QDI-based asynchronous circuits tolerate the process variations and gain acceptance to reduce the power consumption, area-overhead, and timing-closure in NoC architecture [2]. The intellectual property (IP) or PEs are synchronous and communicate asynchronously in globally asynchronous locally synchronous (GALS) architecture. The GALS system offers low-latency and high throughput designs by maintaining robustness in timing domain interfaces. The GALS is constructed using two design approaches: i) the pausable clocking method and ii) the first-in-first-out (FIFO) design. The pausable clocking method pauses the clock during data transfer from/to asynchronous domains to avoid metastability issues. The FIFO designs synchronize the synchronous and asynchronous circuits using standard synchronizers. The FIFO designs offer better throughput by avoiding the synchronizer's latency [3].

The virtual channel (VC) flow control is a commonly used control mechanism in most router architectures. The VC provides distinct buffers for storing the data in each frame. Each router port uses multiple VCs to construct the frames for flit delivery in a time-division manner. The allocated frame with a VC is temporarily stalled in the router to improve the throughput. The VC-based asynchronous router leads to additional area and speeds overhead. So, Song and Edwards [4] introduced the first spatial division multiplexing (SDM) flow-control approach in 2010 for throughput improvements in asynchronous on-chip networks. The scalable asynchronous routers are constructed using QDI logic and an adaptive routing algorithm with minimal timing assumptions. These routers are suitable for GALS systems and provide better network performance than synchronous routers [5]. The GALS clock scheme replaces the balanced clock trees in multi-synchronous NoCs to improve latency and power consumption. The construction of asynchronous routers using EDA tools is challenging because most of the used digital circuits are synchronous [6], [7]. The asynchronous NoC-based Router uses a congestion–aware routing approach with minimal process variation delay to improve the throughput and delay parameters [8]. The different fault models are introduced in asynchronous routers to realize the network errors and failure rates [9]. The compact delay-insensitive (CDI) and physical wire-delay information approaches are used to improve the speed of the asynchronous router in NoCs [10]–[12].

The existing works of asynchronous routers are described as follows: Song and Edwards [13], [14] present the asynchronous spatial division multiplexing (ASDM) router to analyze the area and latency parameters. The VC and SDM-based routers are designed to realize the performance metrics. The SDM router provides better throughput with less overhead than VC based router. The area, latency, and throughput parameters are estimated for different payload lengths. In addition, the 2-Stage Clos switches-based SDM router is designed to reduce the area by replacing the crossbar switch with the 2-stage Clos switch. Nguyen and Tran [15] present the asynchronous FIFO design for multi-synchronous NoCs. GALS based NoC designs face data transferring issues and are rectified using asynchronous FIFOs in NoCs. The FIFOs performance metrics are improving using register-based memory and token-ring-based structures.

Kotleas *et al.* [16] describe the asynchronous router with a synchronization mechanism for Time-division multiplexing (TDM) based NoCs. The TDM-based scheduling approach minimizes the router's switching activity time. Eldin *et al.* [17] explain the Congestion aware routing method with Process variation (PV) delay (CRPD) for asynchronous NoC design. The PDCR offers scalable and low-cost design using an adaptive routing algorithm and improves the delay and throughput parameters. Imai *et al.* [18] compare synchronous and asynchronous NoC routers. The work analyzes the features like baseline designs, buffer allocations, design evaluation, transition signaling, and optimization approaches for both routers. The asynchronous routers are suitable for small data packet transmission, whereas synchronous routers are suitable for transferring large data packet transmission.

Russell *et al.* [19] present asynchronous bundled–data routers for GALS-based NoC. The asynchronous router contains input and output interface units used for data synchronization. The work analyzes the router's timing loops and constraints with verification. Ho *et al.* [20] present the QDI-based Quad-rail sense-amplifier half-buffer (SAHB) methods with asynchronous logic for NoC router construction. The Quad rail SAHB approach reduces the transistors switch count and power consumption. The router provides high robustness under process-voltage-temperature (PVT) conditions. Ax *et al.* [21] describe the synchronous, mesochronous, and asynchronous NoCs architecture comparison for GALS-based Multiprocessing systems on chips (MPSoCs). The work analyzes the cluster node for different NoCs and performance metrics, including area, power, latency, and throughput parameters. Weber *et al.* [22] present asynchronous communication (end-to-end) via a synchronous NoC module. The NoC name is Arke, configurable to 2D/3D mesh, and supports packet and circuit switching approaches. The Arke NoC is interfaced with asynchronous circular FIFO for end-to-end data communication.

Etman *et al.* [23] describe the synchronous and asynchronous NoC architectures for the dark silicon era. The dark silicon synchronous and asynchronous (DSSA) based NoC provides a better latency solution against many hops from source to destination. Swain *et al.* [24] describe the synchronous and asynchronous NoC architectures with their performance realization for consumer electronics devices. Glint *et al.* [25] present the asynchronous NoC simulator (ANSim), which offers metastability, better design space, and fast simulation time with heterogeneous features. Wasif *et al.* [26] present the synchronous-asynchronous-based circuit-switched NoC module with energy-efficient features. The NoC router offers a better reduction in power and lags with more latency. Patil and Sandi [27] present the asynchronous router for NoC with buffer-less features. The router uses an arbiter and routing algorithm to transfer data from source to destination addresses. An efficient ASDM router is constructed for NoC designs in this manuscript. The contribution of the proposed router is highlighted as follows: i) the ASDM router offers low latency and high throughput with less area overhead on the FPGA platform, ii) the ASDM router uses only asynchronous circuit primitives (AND, OR, NAND, NOR, and BUF) without using clock counterparts, iii) the ASDM router can be configurable to any bandwidth size and number of VCs without changing the body of the router

architecture, and iv) the router is compared with existing asynchronous router architecture with network performance improvements.

The proposed ASDM router and its sub-modules are analyzed with detailed architectures in section 2. Section 3 discusses the results and performance comparison of the router. Lastly, section 4 concludes the overall work with futuristic scope.

2. ASYNCHRONOUS SDM ROUTER

The asynchronous SDM router is illustrated in Figure 1. The ASDM router mainly contains input and output (I/O) buffers of size 'B', a crossbar unit, and a switching allocator unit. The data width (bandwidth) of the port in the ASDM router is 'W' bits. Each I/O buffer is divided internally into 'C' virtual circuits. So, the crossbar unit is constructed with a CB x CB size, and each router port has a bandwidth of W/C bits. The switching allocator is used to configure the requests from input buffers with the help of the arbitration mechanism. The crossbar unit produces the required signals to output the buffer to realize the performance metrics. In this work, the router is configured as B=5, C=1 or 2, W=16 or 32, and port bandwidth W/C=16 or 32.

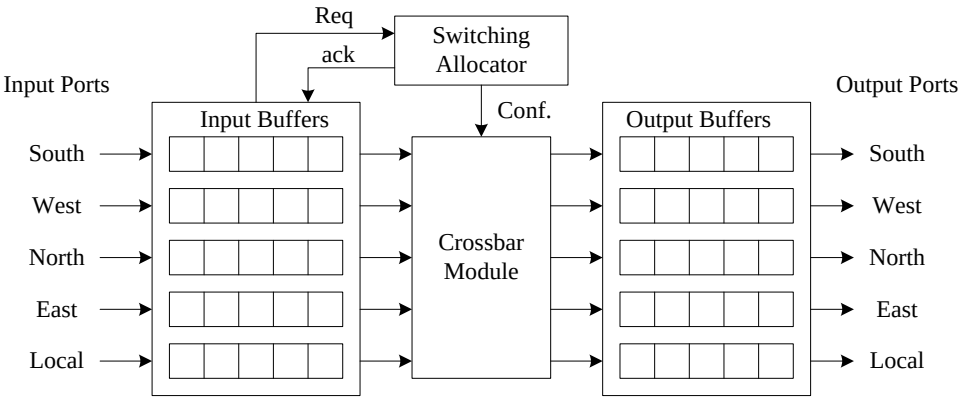

Figure 1. Asynchronous SDM router architecture

The input buffer mainly contains four pipeline stages, a sub-channel controller, and a routing decision module. The input buffer architecture is illustrated in Figure 2. The input buffer has five 32-bit inputs (south, west, north, east, and local), acknowledge output, end of frame (EOF) signal, and 8-bit local address (XY) at the input side.

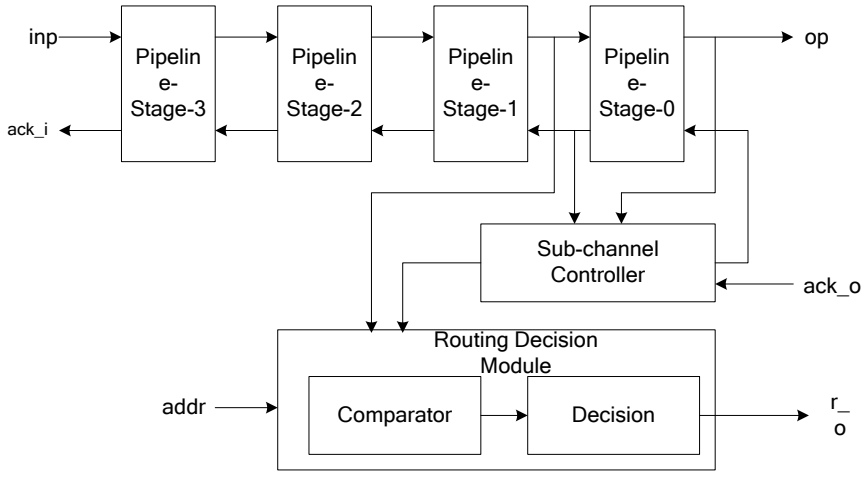

Figure 2. Input buffer architecture

The input buffer generates the five 32-bit outputs, acknowledge input, end of frame (EOF) signal, and requests outputs at the output side. Each pipeline stage is constructed using a 4-bit 4-phase dual-rail pipeline unit. Each pipeline stage receives the four inputs along acknowledge signal and generates the same at the output side.

The routing decision module receives the local XY and pipeline XY addresses and generates the routing decision. The routing decision is obtained by comparing the two 4-bit addresses (local and pipeline). The four comparators are used to create the raw decoded data. The raw decoded data was used further until the last tail flit received from all the sub-channels to generate the decoded data. These decoded data are used to create the arbiter request. The sub-channel controller is used to control the pipeline stages and also the routing decision module. The sub-channel controller receives the output acknowledge signal and decision signal to generate the input acknowledge signal and EOF bit. The description of pipeline stage is explained in the next section.

The asynchronous circuits are used in the router construction along with sequential modules like latches and registers for handshaking mechanisms than global clocks. The 4-phase 1-of-4 handshaking protocol is used in router architecture. The 4-phase protocol is level-triggering all the gates used in asynchronous circuits. The bundled data is used to pipeline the encoded data in binary format. The 4-phase 1-of-4 protocol utilizes less area and power than the dual-rail protocol. The Muller C-element is one most primitive used in QDI circuits. The symmetric form 2-input C-element is represented in Figure 3 and is used as a latch to store the data. The corresponding transition table of the C-element is tabulated in Table 1. The C-element acts as an AND gate with memory. The input values are set to 0/1, and the output is set to 0/1. The output retains its previous value when the input values differ during the intermediate stage.

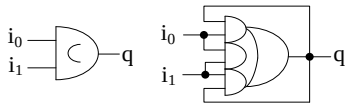

Figure 3. Two-input C-element

Table 1. Transition table

i_0	i_1	q pre	q next
0	0	-	0
1	1	-	1
0	1	q	q
1	0	q	q

The 4-bit 4-phase dual-rail pipeline stage is represented in Figure 4. It is constructed using four individual 1-bit dual-rail pipeline stages. The 4-bit 4-phase dual-rail pipeline has four inputs and outputs along with input-output acknowledge signals (ack_i and ack_o). The input data for each pipeline stage is divided into four slices. Each slice is allocated into the four-bit level pipeline in bitwise order. The C-element generates the common intermediate acknowledge signal synchronized in each slice.

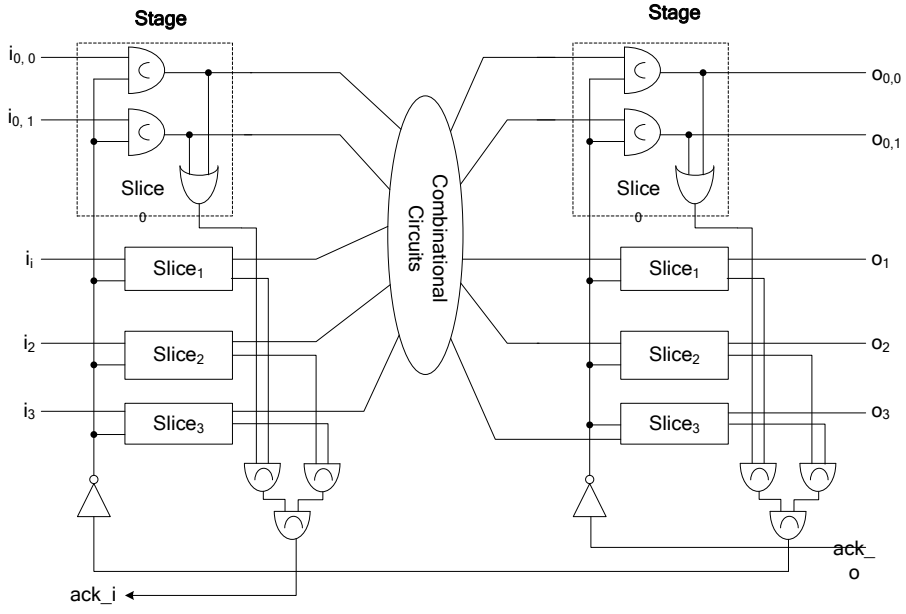

Figure 4. 4-bit 4-phase dual-rail pipeline

Once all the data is released from each slice, reset the signal otherwise, send the corresponding valid acknowledge signal. The completion detection circuit is constructed in each pipeline stage by integrating the C-element with the OR gate. The summary of resource utilization of the input buffer on Artix-7 FPGA is tabulated in Table 2. The 4-stage pipeline unit utilizes 67 LUTs, routing decision module uses 20 LUTs. Two-input C-element with plus input (C2P) utilizes 1 LUT, and the sub-channel controller uses 5 LUTs on Artix-7 FPGA. The corresponding combinational path delay (ns) is also mentioned in Table 2.

Table 2. Resource summary of the input buffer submodules

Modules	Slice- LUTS	Delay (ns)
4-stage pipeline	67	1.552
Routing decision module	20	2.352
C2P unit	1	0.893
Sub-channel controller	5	2.174

The crossbar unit receives all the five input buffer outputs, configuration bits from the allocator, and EOF bits and acknowledges output signals at the input side. The crossbar unit produces the five outputs, EOF output bits, and acknowledges input signals at the output side. The south inputs from X+1, north inputs from X-1, west inputs from Y-1, and east inputs from Y+1 locations are received from crossbar operations. The input signals are ANDed with configuration bits to generate the intermediate-stage output. These intermediate-stage outputs are ORed to create each output signal. The exact process applies to each virtual channel circuit.

The switching allocator receives the five requests from input buffers, generates configuration signals to the crossbar unit, and acknowledges signals to the input buffers. The switching allocator unit mainly contains five-match allocators and an OR gate is illustrated in Figure 5. Each match allocator receives the requests from input buffers, produces the configuration bits to the crossbar unit, and acknowledges the signal to input buffers. The match allocator uses two mutex arbitration units. The Mutex arbiter mechanism receives many requests and produces the grants-based mutex unit. Each mutex unit receives the request and delivers the grant signal using basic NAND and NOR gate primitives.

The output buffer's functionality is the same as the input buffer, with few changes in I/O ports, as illustrated in Figure 6. The pipeline stages produce the four 32-bit outputs, and the working functionality is the same as the 4-phase 1-of-4 dual-rail pipeline unit. The acknowledge input is produced by performing the OR operation using EOF bit of pipeline stage-2 and acknowledge output of the pipeline stage-3. The output buffer is not required to measure the performance metrics; theoretically, it is not required.

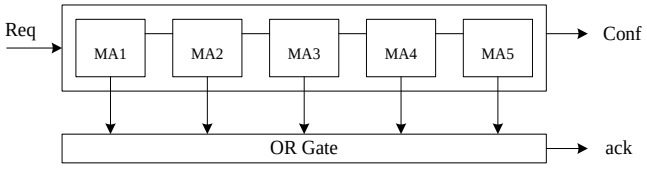

Figure 5. Switching allocator architecture

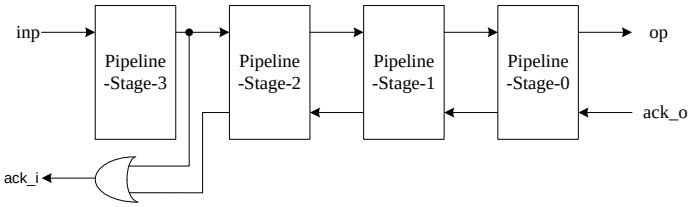

Figure 6. Output buffer architecture

3. RESULTS AND DISCUSSION

The ASDM router and its submodules results are discussed in this section, along with a performance comparison. The ASDM router is designed using Verilog-HDL on Xilinx ISE 14.7 environment and

implemented on Artix-7 FPGA. The Artix-7 FPGA contains a device XC7A100T and CSG 324 as a package with a speed grade of -3. The ASDM router is constructed using I/O buffers, a Crossbar unit, and an allocator. Resource utilization of the ASDM router and its submodules on Artix-7 FPGA is tabulated in Table 3. The Input buffer utilizes slice-LUTs of 51 and obtains a delay of 8.348 ns. The crossbar unit uses 45 LUTs with a delay of 1.606 ns. The switching allocator receives 69 LUTs with a delay of 12.656 ns. The output buffer obtains 113 LUTs with a delay of 7.414 ns. The Graphical representation of the ASDM router and its modules utilization is illustrated in Figure 7. The Slice LUTs are represented in Figure 7(a), and the delay for all the submodules and ASDM router is in Figure 7(b). The ASDM Router utilizes LUTs of 255 and obtains a delay of 58.138 ns. All the submodules are interconnected with each other in the ASDM router. The ASDM router uses more internal wires to interconnect all the submodules.

Table 3. Resource utilization of the ASDM router and its submodules on artix-7 FPGA

Modules	Slice- LUTS	Delay (ns)
Input buffer	51	8.348
Output buffer	113	7.414
Crossbar XY	45	1.606
Switching allocator	69	12.656
ASDM router	255	58.138

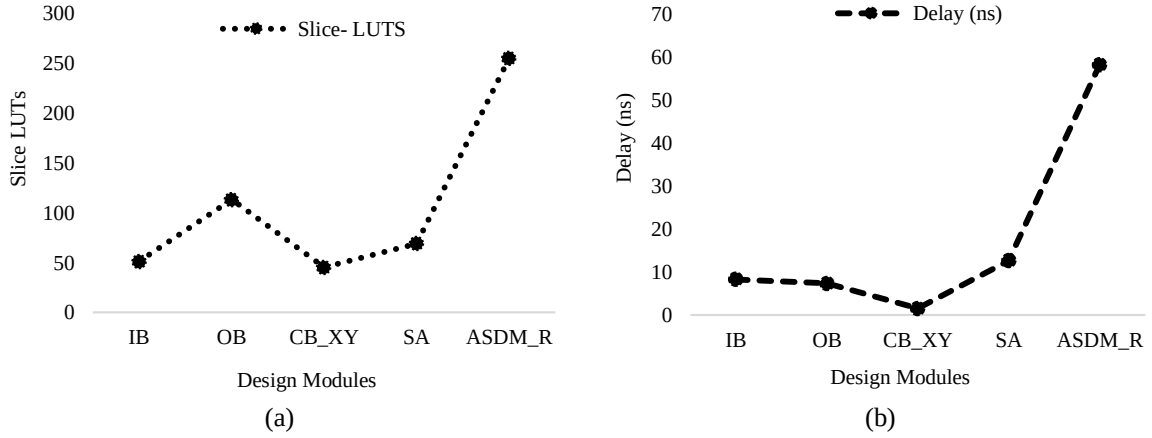

Figure 7. ASDM router and its modules resource utilization in terms of (a) area (LUTs) and (b) delay (ns)

The ASDM router utilization for different data widths and VCs is tabulated in Table 4. The graphical representation of ASDM router performance at different VCs is illustrated in Figure 8. The ASDM router utilizes 255 LUTs with a delay of 58.138 ns at a data width of 16 and VC=1. Similarly, the ASDM router uses 338 LUTs with a delay of 39.679 ns at a data width of 32 and VC=1. When VC is 2, the ASDM router utilizes 842 LUTs with 378.41 ns delay at a data width of 16, and the ASDM router uses 1011 LUTs with 267.215 ns delay at a data width of 32. If the ASDM router's data width increases, the delay value will be reduced drastically. When the data width and number of VC increases, then the router's chip area LUTs will also increase. The ASDM router is constructed using only asynchronous circuits without any sequential circuits (clock-dependent module).

Table 4. ASDM router utilization on different data widths and VCs

VCs	VC = 1		VC = 2	
Data width	16	32	16	32
Slice-LUTS	255	338	842	1011
Delay (ns)	58.138	39.679	378.41	267.215

The performance metrics comparison of the proposed ASDM router with existing approaches is tabulated in Table 5. The performance comparison includes implementation technology, asynchronous protocols, QDI supporting features, flow control mechanism, and latency and throughput parameters. The throughput is measured in terms of Megaflits per second (Mfps). The ASDM router is designed [13] using

130 nm technology. The ASDM router supports QDI based pipelined approach with wormhole and SDM flow control mechanisms. The ASDM router [13] uses a 4-phase 1-of-4 dual-rail protocol and obtains a latency of 228 ns with a throughput of 442 Mfps. The asynchronous router [17] is designed using a congestion-aware routing approach on 32 nm technology. The router [17] uses a 4-phase protocol with QDI support and a wormhole flow control mechanism. The asynchronous router [17] obtains a latency of 47.8 ns with a throughput of 28.8 Mfps. The asynchronous router [20] is designed using QDI based sense amplifier half-buffer SAHB approach on 65 nm technology. The router uses a 4-phase protocol with QDI support and uses both the VC and wormhole flow control approaches. The router [20] obtains a latency of 5.69 ns with a throughput of 258 Mfps.

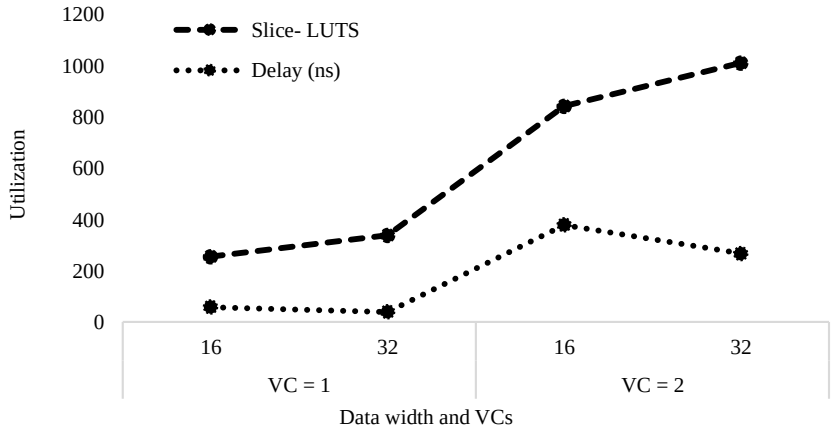

Figure 8. Graphical representation of ASDM router at different VCs

Table 5. Performance metrics comparison of proposed ASDM router with existing approaches

Router Designs	Technology (nm)	Async. protocols	QDI support	Flow Control	Latency (ns)	Throughput (Mfps)
Song and Edwards [13]	130	4-phase 1-of-4	Yes	WH, SDM	228	442
Eldin *et al.* [17]	32	4-phase router	Yes	WH	47.8	28.8
Ho *et al.* [20]	65	4-phase 1-of-4	Yes	VC, WH	5.69	258
Swain *et al.* [24]	90	4-phase router	No	VC, WH	28	800
Wasif *et al.* [26]	65	4-phase 1-of-4	No	CS	0.7	470
Patil and Sandi [27]	28	4-phase router	No	WC	5	560
Proposed ASDM Router	28	4-phase 1-of-4	Yes	WH, SDM	0.8	800

The asynchronous NoC-based router [24] is designed on 90 nm technology. The router uses a 4-phase protocol, and VC and wormhole flow control approaches. The router [24] obtains a latency of 28 ns with a throughput of 800 Mfps. The asynchronous circuit-switched router [26] is designed on 65 nm technology. The router uses a 4-phase 1-of-4 protocol and a circuit switching flow control approach. The router [26] obtains a latency of 0.7 ns with a throughput of 470 Mfps. The asynchronous NoC-based router [27] is designed on 28 nm technology. The router uses a 4-phase router protocol and a wormhole flow control approach. The router [27] obtains a latency of 5 ns with a throughput of 560 Mfps. The proposed ASDM router is designed on 28 nm technology. The ASDM router uses a 4-phase 1-of-4 protocol and wormhole and SDM flow control mechanisms. The ASDM router obtains a latency of 0.8 ns with a throughput of 800 Mfps. The proposed ASDM router utilizes less latency and improves throughput than existing asynchronous router architectures.

4. CONCLUSION

An efficient asynchronous SDM router is presented in this manuscript for NoC architectures on the FPGA platform. The asynchronous circuits use basic gate primitives to construct the ASDM router. The ASDM router offers low-latency and high throughput architecture with less chip area overhead. The ASDM router uses an SDM flow control mechanism with a 4-phase 1-of-4 dual-rail protocol. The ASDM router

divides its I/O buffers into several virtual circuits. The I/O buffers are constructed using a 4-phase 1-of-4 dual-rail protocol using C-elements. The Switching allocator provides configuration bits and acknowledge signal-based input requests in the router. The router and sub-modules are synthesized individually to realize its resource utilization on Artix-7 FPGA. The ASDM router's chip area (LUts) and combinational path delay are analyzed in detail. The router performance is analyzed by changing the bandwidth and VCs. The ASDM Router obtains 0.8 ns latency for 800 MHz throughput by utilizing < 1% chip area. The ASDM router is compared with existing routers with better improvements in latency and throughput parameters. In the future, construct the mesh topology-based NoC architecture with different sizes to realize the performance metrics.

REFERENCES

[1] X.-T. Tran, J. Durupt, Y. Thonnart, F. Bertrand, V. Beroulle, and C. Robach, "Implementation of a design-for-test architecture for asynchronous networks-on-chip," in *First International Symposium on Networks-on-Chip (NOCS'07)*, May 2007, pp. 216–216, doi: 10.1109/NOCS.2007.24.

[2] W. J. Bainbridge and S. J. Salisbury, "Glitch sensitivity and defense of quasi delay-insensitive network-on-chip links," in *2009 15th IEEE Symposium on Asynchronous Circuits and Systems*, May 2009, pp. 35–44, doi: 10.1109/ASYNC.2009.18.

[3] Y. Thonnart, E. Beigné, and P. Vivet, "Design and implementation of a GALS Adapter for ANoC based architectures," in *2009 15th IEEE Symposium on Asynchronous Circuits and Systems*, May 2009, pp. 13–22, doi: 10.1109/ASYNC.2009.13.

[4] W. Song and D. Edwards, "Improving the throughput of asynchronous on-chip networks with SDM," *Proc. of the UK Electronics Forum*, 2010.

[5] A. Alhussien, C. Wang, and N. Bagherzadeh, "A scalable delay insensitive asynchronous NoC with adaptive routing," in *2010 17th International Conference on Telecommunications*, 2010, pp. 995–1002, doi: 10.1109/ICTEL.2010.5478830.

[6] T. N. K. Jain, M. Ramakrishna, P. V. Gratz, A. Sprintson, and Gwan Choi, "Asynchronous bypass channels for multi-synchronous NoCs: a router microarchitecture, topology, and routing algorithm," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 30, no. 11, pp. 1663–1676, Nov. 2011, doi: 10.1109/TCAD.2011.2161190.

[7] C. T. Muller, E. Kasapaki, R. B. Sorensen, and J. Sparso, "Synthesis and layout of an asynchronous network-on-chip using standard EDA tools," in *2014 NORCHIP*, Oct. 2014, pp. 1–6, doi: 10.1109/NORCHIP.2014.7004742.

[8] R. Ezz-Eldin, M. A. El-Moursy, and H. F. A. Hamed, "Novel routing algorithm for minimum on delay with process variation and congestion in asynchronous NoC," in *2015 IEEE 17th International Conference on High Performance Computing and Communications, 2015 IEEE 7th International Symposium on Cyberspace Safety and Security, and 2015 IEEE 12th International Conference on Embedded Software and Systems*, Aug. 2015, pp. 411–416, doi: 10.1109/HPCC-CSS-ICESS.2015.58.

[9] P. M. Yaghini, A. Eghbal, H. Pedram, and H. R. Zarandi, "Investigation of transient fault effects in an asynchronous NoC router," in *2010 18th Euromicro Conference on Parallel, Distributed and Network-based Processing*, Feb. 2010, pp. 540–545, doi: 10.1109/PDP.2010.21.

[10] N. Onizawa, A. Matsumoto, T. Funazaki, and T. Hanyu, "High-throughput compact delay-insensitive asynchronous NoC router," *IEEE Transactions on Computers*, vol. 63, no. 3, pp. 637–649, Mar. 2014, doi: 10.1109/TC.2013.81.

[11] T. Hanyu, Y. Watanabe, and A. Matsumoto, "Accurate and high-speed asynchronous network-on-chip simulation using physical wire-delay information," in *2013 IEEE 43rd International Symposium on Multiple-Valued Logic*, May 2013, pp. 266–271, doi: 10.1109/ISMVL.2013.11.

[12] Y. Thonnart, P. Vivet, S. Agarwal, and R. Chauhan, "Latency improvement of an industrial SoC system interconnect using an asynchronous NoC backbone," in *2019 25th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC)*, May 2019, pp. 46–47, doi: 10.1109/ASYNC.2019.00014.

[13] W. Song and D. Edwards, "Asynchronous spatial division multiplexing router," *Microprocessors and Microsystems*, vol. 35, no. 2, pp. 85–97, Mar. 2011, doi: 10.1016/j.micpro.2010.08.007.

[14] Wei Song, D. Edwards, J. Garside, and W. J. Bainbridge, "Area efficient asynchronous SDM routers using 2-stage clos switches," in *2012 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Mar. 2012, pp. 1495–1500, doi: 10.1109/DATE.2012.6176710.

[15] T.-T. Nguyen and X.-T. Tran, "A novel asynchronous first-in-first-out adapting to multi-synchronous network-on-chips," in *2014 International Conference on Advanced Technologies for Communications (ATC 2014)*, Oct. 2014, pp. 365–370, doi: 10.1109/ATC.2014.7043413.

[16] I. Kotleas, D. Humphreys, R. B. Sorensen, E. Kasapaki, F. Brandner, and J. Sparso, "A loosely synchronizing asynchronous router for TDM-scheduled NOCs," in *2014 Eighth IEEE/ACM International Symposium on Networks-on-Chip (NoCS)*, Sep. 2014, pp. 151–158, doi: 10.1109/NOCS.2014.7008774.

[17] R. Ezz-Eldin, M. A. El-Moursy, and H. F. A. Hamed, "Process variation delay and congestion aware routing algorithm for asynchronous NoC design," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 3, pp. 909–919, Mar. 2016, doi: 10.1109/TVLSI.2015.2434853.

[18] M. Imai, T. Van Chu, K. Kise, and T. Yoneda, "The synchronous vs. asynchronous NoC routers: an apple-to-apple comparison between synchronous and transition signaling asynchronous designs," in *2016 Tenth IEEE/ACM International Symposium on Networks-on-Chip (NOCS)*, Sep. 2016, pp. 1–8, doi: 10.1109/NOCS.2016.7579330.

[19] P. Russell, J. Doge, C. Hoppe, T. B. Preusser, P. Reichel, and P. Schneider, "Implementation of an asynchronous bundled-data router for a GALS NoC in the context of a VSoC," in *2017 IEEE 20th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS)*, Apr. 2017, pp. 195–200, doi: 10.1109/DDECS.2017.7934579.

[20] W.-G. Ho, K.-S. Chong, K. Z. L. Ne, B.-H. Gwee, and J. S. Chang, "Asynchronous-logic QDI quad-rail sense-amplifier half-buffer approach for NoC router design," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 1, pp. 196–200, Jan. 2018, doi: 10.1109/TVLSI.2017.2750171.

[21] J. Ax, N. Kucza, M. Vohrmann, T. Jungeblut, M. Porrmann, and U. Ruckert, "Comparing synchronous, mesochronous and asynchronous NoCs for GALS based MPSoCs," in *2017 IEEE 11th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC)*, Sep. 2017, pp. 45–51, doi: 10.1109/MCSoC.2017.19.

[22] I. I. Weber, F. G. Moraes, L. L. de Oliveira, and E. A. Carara, "Exploring asynchronous end-to-end communication through a synchronous NoC," in *2018 31st Symposium on Integrated Circuits and Systems Design (SBCCI)*, Aug. 2018, pp. 1–6, doi: 10.1109/SBCCI.2018.8533228.

[23] R. W. Etman, S. Hesham, K. Hoffman, M. A. A. El Ghany, and D. Goehringer, "Analysis of synchronous-asynchronous NoC for

the dark silicon era," in *2018 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC)*, Oct. 2018, pp. 1–7, doi: 10.1109/NORCHIP.2018.8573470.
[24] A. K. Swain, A. K. Rajput, and K. K. Mahapatra, "Network on chip for consumer electronics devices: an architectural and performance exploration of synchronous and asynchronous network-on-chip-based systems," *IEEE Consumer Electronics Magazine*, vol. 8, no. 3, pp. 50–54, May 2019, doi: 10.1109/MCE.2019.2892243.
[25] T. Glint, J. Sah, M. Awasthi, and J. Mekie, "ANSim: a fast and versatile asynchronous network-on-chip simulator," in *2020 IEEE 38th International Conference on Computer Design (ICCD)*, Oct. 2020, pp. 619–622, doi: 10.1109/ICCD50377.2020.00107.
[26] S. A. Wasif, S. Hesham, D. Goehringer, K. Hofmann, and M. A. Abd El Ghany, "Energy efficient synchronous - asynchronous circuit-switched NoC," in *2020 9th International Conference on Modern Circuits and Systems Technologies (MOCAST)*, Sep. 2020, pp. 1–4, doi: 10.1109/MOCAST49295.2020.9200298.
[27] T. Patil and A. Sandi, "Design and implementation of asynchronous NoC architecture with buffer-less router," *Materials Today: Proceedings*, vol. 49, 2022, pp. 756–763. doi: 10.1016/j.matpr.2021.05.282.

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