

Modeling of magnetic sensitivity of the metal-oxide-semiconductor field-effect transistor with double gates

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ABSTRACT

In this paper, we investigated the effect of magnetic field on the carrier transport phenomenon in metal-oxide-semiconductor field-effect transistor (MOSFET) with double gates by examining the behavior of the semiconductor under the Lorentz force and a constant magnetic field. Various behaviors within the channel have been simulated including the potential distribution, conduction and valence bands, total current density, total charge density and the magnetic field. The results obtained indicate that this modulation affects the electrical characteristics of the device such as on-state current (I_{ON}), subthreshold leakage current (I_{OF}), threshold voltage (V_{Th}), and the Hall voltage (V_H) is induced by the magnetic field. The change in threshold voltage caused by the magnetic field has been observed to affect the switching characteristics of the device, such as speed and power loss, as well as the threshold voltage V_{Th} and (I_{ON}/I_{OF}) ratio. Note that it is reduced by 10-3 V. 102 for magnetic fields of ± 6 and ± 5.5 tesla respectively.

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1. INTRODUCTION

With the continuous advance of semiconductor technology miniaturization, nanoscale integrated circuits have become extremely sensitive to external magnetic fields [1]. It is well known that miniaturizing conventional metal-oxide-semiconductor field-effect transistor (MOSFETs) at the nanoscale [2] results in a higher magnetic sensitivity with respect to the magnetic field due to the smaller active channel area [3], [4]. It allows a variety of complex short-channel effects (SCE) such as hot carrier effect, threshold voltage, substrate carrier effect, Hall voltage, will occur within linear region with large fluctuations in drain voltage [5], [6]. The effect of the parasitic effect on the external electrical properties of field effect transistors has been reported in the field of MOSFETs [7], [8] microelectronics, and some studies have also studied materials that conduct current [9]. Investigation of the existence, magnetic field in carrier transport phenomenon, and thus the active region of semiconductor device, especially magnetic field in complementary metal oxide semiconductor (CMOS) transistor technology [10].

Experiments in some case studies have shown that magnetic fields cause a current deflection in the drain current voltage, which alters the conductivity of the active region resulting in asymmetric magnetic tunneling and non-uniform spatial conduction in MOSFETs [11], [12]. Wick made the first measurement of the Hall-effect of silicon on a fairly impure sample [13]. Other studies by Shockley and Pearson and Putley and Mitchell [14], [15] use the Hall effect of low-impurity single-crystal silicon. Magnetic reciprocating current of an N-type metal-oxide-semiconductor (N-MOS) transistor exposed to external magnetic fields

B=7T and 14T [16]. Therefore, the Lorentz force acts on the current wires in the current channel [17]. However, due to its limited application in such a high-level field [18], [19], this topic has not been studied.

Hall-effect device simulation is relatively new, having begun in the 1980s [20] to help analyze and understand Hall-effect behavior in complex devices such as integrated circuits [21]. The aim of this paper is to analyze advanced nanoscale CMOS integrated circuits and their sensitivity to external magnetic fields. Their performance can be seriously affected, so it may be due to unforeseen failures. For vehicles and machines controlled by these circuits, the system may lose control.

To solve this problem, it is necessary to control the effect of external magnetic field on the operation of these circuits. This control includes the quantification, analysis, and effects of these noises on the circuit performance. For this purpose, a double gate MOSFET transistor is considered and modeled by the finite element method, which takes into account all the effects of carrier transport inside the semiconductor under an external magnetic field.

2. METHOD

Figure 1 shows the structure of the device investigated in the simulation of the proposed structure in this work. The applied magnetic field $B=(0, B_y, 0)$ is assumed to be perpendicular to the current flowing between the drain and the source of the two contacts oriented along the y-axis. The current density through the silicon channel is along the z-axis. To detect the Hall voltage V_h , two open Hall 1 and Hall 2 rectangular contacts are provided and fabricated on a MOSFET with a double gates structure arranged perpendicular to the Y direction.

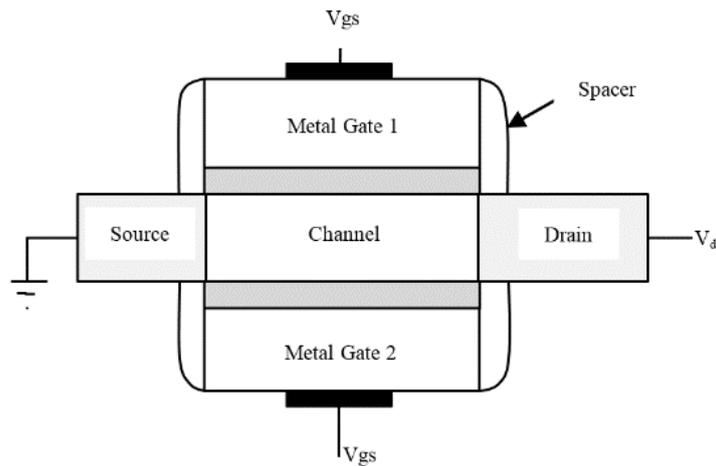


Figure 1. The schematic structure of the MOSFET with double gates [22]

Channel length $L=20$ nm, width $W=28$ nm. The drain-source voltage is represented by V_d , the gate-source voltage is represented by V_g , and the threshold voltage is represented by V_t . Table 1 illustrates the physical parameters of the MOSFET used in this simulation structure [23].

Table 1. Physical parameters of the MOSFET with double gates used in the simulation structure

Parameter	Volume
Impurity doping in the channel (N_a)	10^{14} cm^{-3}
Impurity doping in drain and source (N_d)	10^{18} cm^{-3}
Thickness of silicon film (t_{Si})	10 nm
Thickness of oxide (t_{ox})	2 nm

When a constant magnetic field B is applied perpendicular to the direction of the drain current, the Lorentz equation was used to describe the Hall-effect \mathcal{M} of the MOSFET with double gate [24] as:

$$\mathcal{M} = \frac{d^2r}{dt^2} + \frac{m dr}{\tau dt} = [E + (V_d \cdot B)](-e) \tag{1}$$

where m is the effective mass of the cyclotron, r is the position, τ represent the average (recalculated) electron lifetime. V_d is the motion of the electron through the Hall effect. An electric field is applied in the direction given by the biased contacts of the transistor. Then, the Hall field \tilde{E}_H generated by the Hall-effect [25] is given as (2).

$$\tilde{E}_H = B_t \frac{(p\mu_p^2 - n\mu_n^2)}{(e(p\mu_p^2 + n\mu_n^2))} \left(\frac{I_d}{w.T} \right) \quad (2)$$

At low drain voltage VD , in the linear region of operation of a MOSFET, $VD < VG - VT$. The area density of carriers in the channel is approximately constant over the channel. This charge density can be calculated as (3) [25]:

$$Q_{ch} = C_{ox}(V_g - V_T) \quad (3)$$

where C_{ox} represents the capacitance of the gate oxide on the circuit. The current of the drain I_d can be calculated as (4) [25].

$$I_d = 2\mu_{ch}C_{ox} \frac{W}{L} V_d \left(V_G - V_T - \frac{V_d}{2} \right) \quad (4)$$

At the channel drain boundary, the charge density will be reduced to zero, and the current practically remains constant. The MOSFET Hall voltage V_H can be calculates as [25]:

$$V_H = G_H I_D B_T \frac{r_H}{Q_{Ch}} \quad (5)$$

where G_H represent the factor of the geometric correction and r_H represent the Hall factor.

3. RESULTS AND DISCUSSION

Figure 2 shows the presence of (B=+6 and -6 tesla) with the absence of magnetic field (B=0 tesla). From Figure 2, we can see that in the relaxation state ($V_g=0$), the Hall voltages for the three magnetic field values are almost identical. When the transistor is biased, the Hall voltage gradually increases or decreases asymmetrically according to the direction of the applied magnetic field with respect to the zero magnetic field (B=0 tesla). Until saturation, the movement of electrons on the walls of the holes stops.

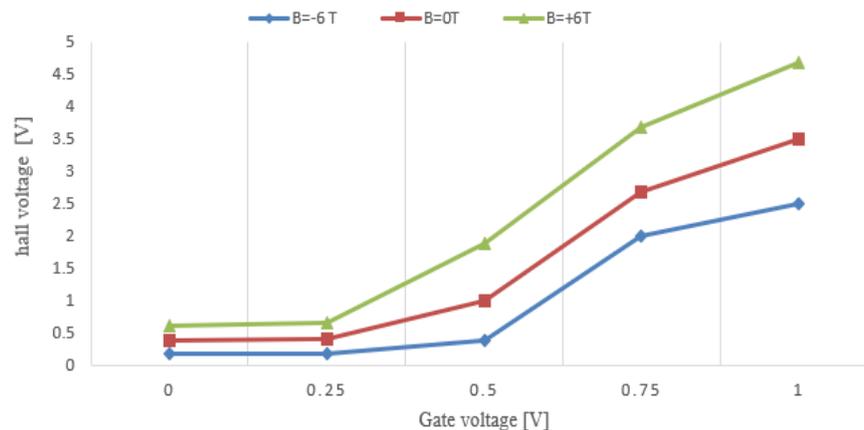


Figure 2. Simulated of the double gate MOSFET Hall voltage (V_h) for (B=+6, -6 tesla, B=0 tesla), $V_d=0.05$ V

Figure 3 shows the Hall voltage V_H as a function of the drain current I_D flowing through the drain and source contacts. It consists of a gate voltage V_G and a magnetic field B applied to the gate contact (G). B=+6, B=-6 tesla, B=0 tesla. At rest ($V_g=0$), we can see that the Hall voltage is more or less for all three magnetic field values. As the gate voltage increases, the Hall voltage gradually increases or decreases asymmetrically with respect to the zero magnetic field (B=0 tesla) according to the direction of the applied

magnetic field, and the Hall voltage increases or decreases immediately once the threshold voltage V_T is reached, the voltage rises or falls rapidly. If the value of the bias voltage V_G is high, the Hall voltage will follow the same change until it settles in the saturation region.

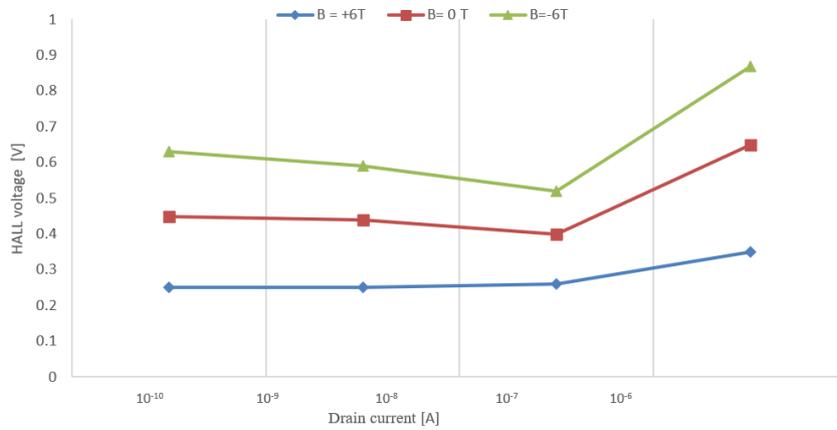


Figure 3. Simulated MOSFET Hall voltage V_H versus drain current at $B=+6$, -6 tesla, and $B=0$ tesla

If the carriers are biased towards the Hall 2 recombination surface, their current will decrease with decreasing transistor channel concentration. If the carriers are biased towards the Hall 1 recombination plane, the carrier concentration in the transistor channel will increase and the drain current will also increase. This explains the difference in Hall voltage between the two surfaces of the Hall 1 and Hall 2 contacts. Therefore, the magnetic transistor is sensitive to the signal of the applied magnetic field.

Figure 4 shows the central potential in the x direction for three magnetic field values. Given that the device is in the on state, the gate voltage varies from 0 to 1 V and the drain voltage is 0.05 V, so the current in the channel increases with the gate voltage. The Hall-effect causes a drain-source current with magnetic induction B perpendicular to the direction of this current, along the two contact Hall planes.

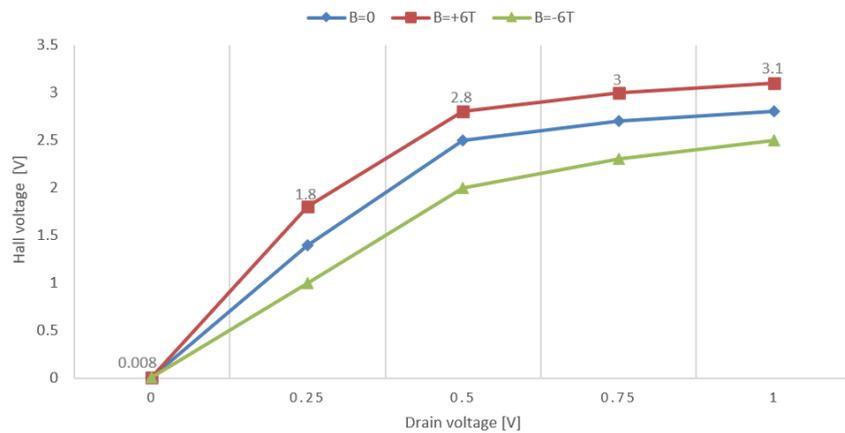


Figure 4. Simulated MOSFET Hall voltage V_H variation with respect to drain voltage (V_D) for $B=+6$, -6 tesla and $B=0$ tesla when $V_G=0.05$ V

The drain current I_D versus drain voltage V_D curves for constant flux density, ($B=0$ tesla, 6 and -6 tesla) are shown in Figure 5. In the linear region of the I_D versus V_D curve, the drain current I_D remains constant in both directions of the applied magnetic field, whereas in the saturation region we find that the I_D increases or decreases depending on the direction of the applied magnetic field. Due to the Hall effect, electrons accumulate on the contact surface between Hall 1 and Hall 2. So, the magnitude of the charge amplitude in the inverse layer per unit area is effectively reduced, reducing the permittivity of the channel shown in Figure 5, thereby reducing the drain current I_D . If a constant magnetic field B is applied in the

opposite direction (negative y direction), the effect will be exactly the opposite. In this case, the permeability increases and the current I_D of the drain increases. The Hall voltage against the drains voltage is shown in Figure 6. If the carriers have been deflected in the direction of Hall 2 recombined surface, then the concentration in the channel of the transistor will decrease and the current will also decrease.

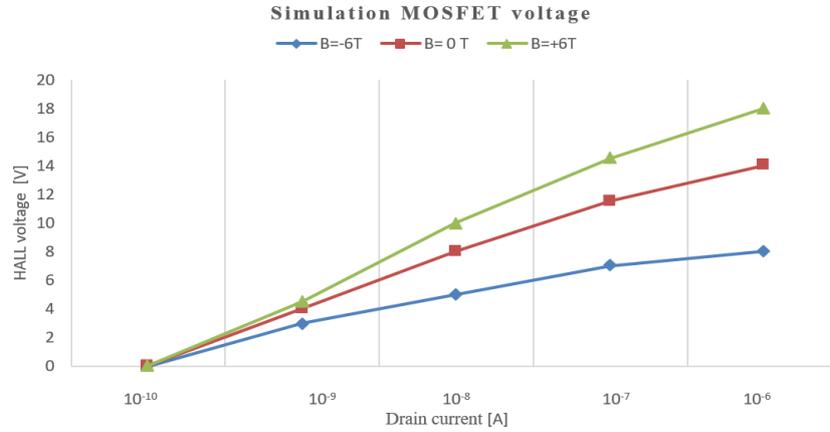


Figure 5. Simulated MOSFET Hall voltage variation with respect to drain current for different drain voltages, at B=+6, -6 tesla and B=0 tesla and $V_G=0.05$ V

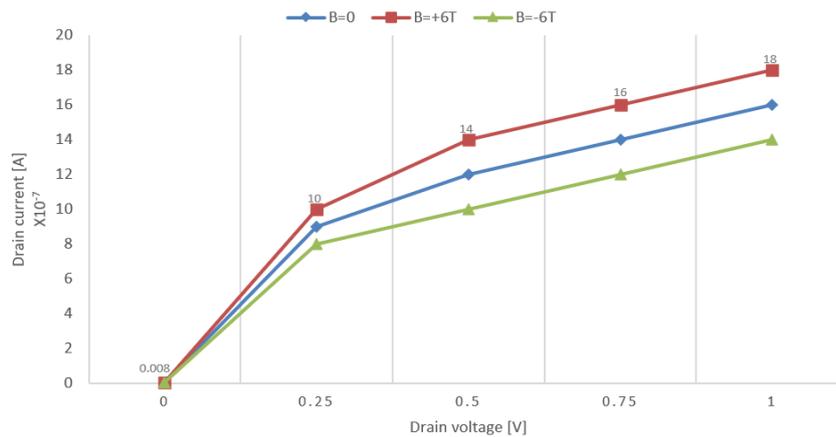


Figure 6. Simulated MOSFET drain current I_D versus drain voltage V_D in case of (B=+6, -6 tesla and B=0 tesla) when $V_G=0.5$ V

Figure 7 shows the Hall voltage against the drain current of the MOSFET surface. If the carriers are deflected in the direction of the recombination surface of the Hall 1, then the concentration in the transistor channel will increase, and the current of the drain will increase. This declares the difference in the value of the Hall voltage on the both surfaces of Hall 1 and Hall 2 connections. So, we can conclude that this magneto-transistor was extremely sensitive to the applied magnetic field sign.

Figure 8 shows the discontinuous ratio of drain current with respect to the magnetic field B direction which applied at various drain voltages $V_d=0.1$ V, $V_d=0.5$ V and $V_d=1$ V. Note that at high drain voltages, there is a large difference in sensitivity corresponding to the saturation region of the I_D versus V_D curve shown in Figure 6. At B=0 tesla, the difference in the threshold voltage $V_t=0.440$ V region is slightly smaller, but observed at the minimum drain voltage V_d , the difference is almost negligible.

The sensitivity of the device was evaluated for both channels and the results are shown in Figure 9. The different gate voltages $V_g=0.1$ V, $V_g=0.5$ V, and $V_g=1$ V obtained in Figure 8 show the proportional sensitivity between the Hall voltage difference and the direction of the applied magnetic field. There is a large difference in the sensitivity of the different gate voltages, but a large difference is observed at gate voltages around the threshold voltage $V_t=0.440$ V for B=0 tesla.

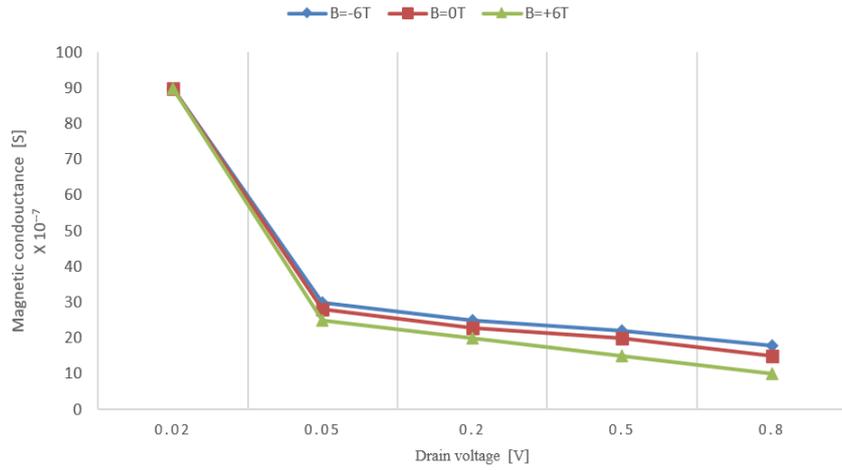


Figure 7. Valence band energy along with the channel length along x-direction at (B=+6, -6, and B=0 tesla) tesla at different gate to source voltages V_G values and at $V_D=0.05$ V

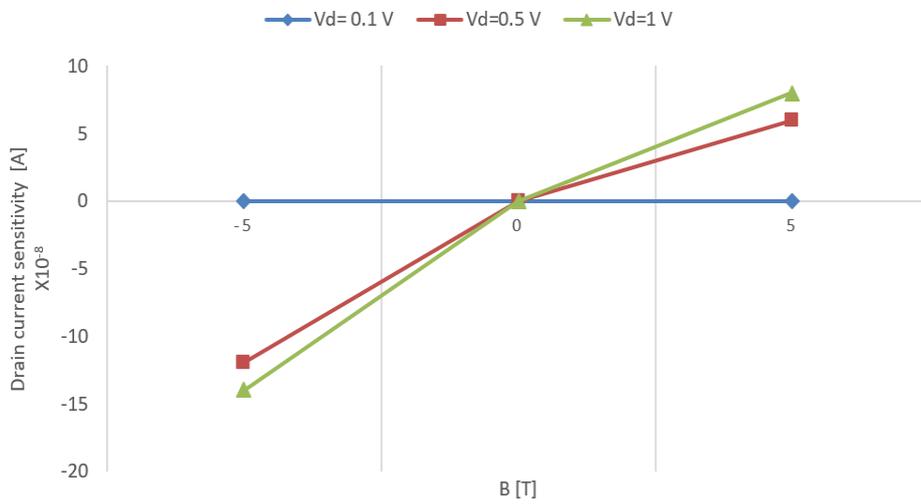


Figure 8. Simulated MOSFET drain current I_D imbalance ($\Delta I_D = I_{D1} - I_{D2}$) versus the applied magnetics field

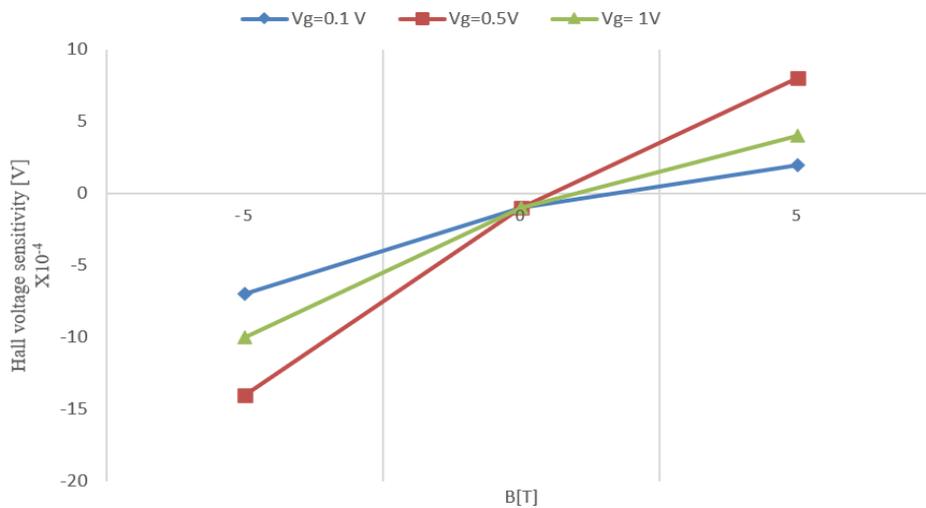


Figure 9. Simulated MOSFET Hall voltage difference ($\Delta V_H = V_{H1} - V_{H2}$) versus the applied magnetics field

4. CONCLUSION

This paper presents a numerical simulation of the effect of magnetically induced Hall magnetic fields on the electrical characteristics of an n-channel double gates MOSFET transistor. Several theories suggest that for small transistors, the Hall voltage V_H peaks in both magnetic field directions in the threshold region of short-channel FETs compared to long-channel FETs. This heaped because the drain current (I_D) changes at different drain voltages (V_D) and the direction of the applied magnetic field is perpendicular to the direction of the drain current caused by the inversion charge of the layer, which directly reflects the permeability behavior. It is expressed that they are there. From the results obtained, it can be seen that for short channel transistors, the drain current I_D and magnetic trans conductance (g_{mm}) are also reduced, depending on the strength of the magnetic field rather than the direction of the magnetic field. Adverse effects observed include a decrease in the (I_{ON}/I_{OF}) ratio as a function of the applied magnetic field (B). This is one of the requirements of today's CMOS technology. From this point of view, we examined the various solutions developed to remedy the controlled parasites and set out to quantify and reduce (or eliminate) them.

REFERENCES

- [1] H.-C. Chow, P. Chatterjee, and W.-S. Feng, "A simple drain current model for MOS transistors with the lorentz force effect," *Sensors*, vol. 17, no. 6, May 2017, doi: 10.3390/s17061199.
- [2] P. Chatterjee, H.-C. Chow, and W.-S. Feng, "Drain current modulation of a single drain MOSFET by lorentz force for magnetic sensing application," *Sensors*, vol. 16, no. 9, Aug. 2016, doi: 10.3390/s16091389.
- [3] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*. Hoboken, NJ, USA: John Wiley & Sons, Inc., 2006.
- [4] W. M. E. A. W. Jusoh and S. H. Ruslan, "Design and analysis of current mirror OTA in 45 nm and 90 nm CMOS technology for bio-medical application," *Bulletin of Electrical Engineering and Informatics*, vol. 9, no. 1, pp. 221–228, Feb. 2020, doi: 10.11591/eei.v9i1.1860.
- [5] M. Kessi, A. Benfdila, and A. Lakhlef, "Investigation on cylindrical gate-all-around (GAA) tunnel FETS scaling," in *2017 IEEE 30th International Conference on Microelectronics (MIEL)*, Oct. 2017, pp. 199–202, doi: 10.1109/MIEL.2017.8190102.
- [6] M. Kessi, A. Benfdila, A. Lakhelef, L. Belhimer, and M. Djouder, "Investigation on body potential in cylindrical gate-all-around MOSFET," in *2019 IEEE 31st International Conference on Microelectronics (MIEL)*, Sep. 2019, pp. 213–216, doi: 10.1109/MIEL.2019.8889640.
- [7] B. Arezki, M. Kessi, and A. Lakhlef, "FinFET versus GAAFET performances and perspectives," *European Material Research Society (EMRS), Spring Meeting*, Nice, France, 2019.
- [8] J. Höfflin, C. Sander, P. Gieschke, A. Greiner, and J. G. Korvink, "Subthreshold CMOS transistors are largely immune to magnetic field effects when operated above 11 T," *Concepts in Magnetic Resonance Part B: Magnetic Resonance Engineering*, vol. 45, no. 2, pp. 97–105, Apr. 2015, doi: 10.1002/cmr.b.21284.
- [9] D.-V. Nguyen *et al.*, "Modeling the effect of strong magnetic field on n-type MOSFET in strong inversion," in *2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Dec. 2018, pp. 637–640, doi: 10.1109/ICECS.2018.8617922.
- [10] A. Acharyya, D. Chatterjee, A. Mondal, and N. Banerjee, "Experimental study on the effect of magnetic field on current-voltage characteristics of n-channel enhancement-type MOSFET," *Journal of Electron Devices*, vol. 13, pp. 945–948, 2012.
- [11] A. E. P. De los, E. A. Gutierrez-D, J. Molina-R, and F. Guarin, "Non-homogeneous space mechanical strain induces asymmetrical magneto-tunneling conductance in MOSFETs," in *2014 44th European Solid State Device Research Conference (ESSDERC)*, Sep. 2014, pp. 90–93, doi: 10.1109/ESSDERC.2014.6948765.
- [12] E. A. Gutierrez-D. *et al.*, "Atomistic magnetoconductance effects in strained FETs," in *28th Symposium on Microelectronics Technology and Devices (SBMicro 2013)*, Sep. 2013, pp. 1–5, doi: 10.1109/SBMicro.2013.6676181.
- [13] L. Hebrard *et al.*, "On The influence of strong magnetic field on MOS transistors," in *2016 IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Dec. 2016, pp. 564–567, doi: 10.1109/ICECS.2016.7841264.
- [14] H. P. Baltes, L. Andor, A. Nathan, and H. G. Schmidt-Weinmar, "Two-dimensional numerical analysis of a silicon magnetic field sensor," *IEEE Transactions on Electron Devices*, vol. 31, no. 7, pp. 996–999, 1984.
- [15] M.-A. Paun, J.-M. Sallèse, and M. Kayal, "Comparative study on the performance of five different hall effect devices," *Sensors*, vol. 13, no. 2, pp. 2093–2112, Feb. 2013, doi: 10.3390/s130202093.
- [16] R. Sarpeshkar, T. Delbruck, and C. A. Mead, "White noise in MOS transistors and resistors," *IEEE Circuits and Devices Magazine*, vol. 9, no. 6, pp. 23–29, Nov. 1993, doi: 10.1109/101.261888.
- [17] C. Schutte and P. Rademeyer, "Subthreshold 1/f noise measurements in MOS transistors aimed at optimizing focal plane array signal processing," *Analog Integrated Circuits and Signal Processing*, vol. 2, no. 3, pp. 171–177, Sep. 1992, doi: 10.1007/BF00276630.
- [18] S. Cristoloveanu, M. Bawedin, and I. Ionica, "A review of electrical characterization techniques for ultrathin FDSOI materials and devices," *Solid-State Electronics*, vol. 117, pp. 10–36, Mar. 2016, doi: 10.1016/j.sse.2015.11.007.
- [19] A. H. Mohammed, G. T. Hasan, and K. J. Ali, "Numerical analysis of the photovoltaic system inspection with active cooling," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 11, no. 4, pp. 2779–2789, Aug. 2021, doi: 10.11591/ijece.v11i4.pp2779-2789.
- [20] F. Traub, J. Hansen, W. Ackermann, and T. Weiland, "Automated construction of physical equivalent circuits for inductive components," in *2013 International Symposium on Electromagnetic Compatibility*, 2013, pp. 67–72.
- [21] F. N. Abdul-kadir and F. H. Taha, "Characterization of silicon tunnel field effect transistor based on charge plasma," *Indonesian Journal of Electrical Engineering and Computer Science (IJECS)*, vol. 25, no. 1, pp. 138–143, Jan. 2022, doi: 10.11591/ijeecs.v25.i1.pp138-143.
- [22] P. Hillenbrand, M. Beltle, S. Tenbohlen, and S. Monch, "Sensitivity analysis of behavioral MOSFET models in transient EMC simulation," in *2017 International Symposium on Electromagnetic Compatibility-EMC EUROPE*, Sep. 2017, pp. 1–6, doi: 10.1109/EMCEurope.2017.8094762.
- [23] M. Kessi and A. Benfdila, "Magnetic sensitivity modeling of dual gate MOS transistor," *Indonesian Journal of Electrical Engineering and Computer Science (IJECS)*, vol. 24, no. 2, pp. 1238–1248, 2021, doi: 10.11591/ijeecs.v24.i2.pp1238-1248.

- [24] M. Hebali *et al.*, "A high electrical performance of DG-MOSFET transistors in 4H-SiC and 6H-SiC 130 nm technology by BSIM3v3 model," *Journal of Electrical Engineering*, vol. 70, no. 2, pp. 145–151, Apr. 2019, doi: 10.2478/jee-2019-0021.
- [25] I. Sabiri, H. Bouyghf, A. Raihani, and B. Ouacha, "Optimal design of CMOS current mode instrumentation amplifier using bio-inspired method for biomedical applications," *Indonesian Journal of Electrical Engineering and Computer Science (IJECS)*, vol. 25, no. 1, pp. 120–129, Jan. 2022, doi: 10.11591/ijeecs.v25.i1.pp120-129.

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