International Journal of Electrical and Computer Engineering (IJECE)
Vol. 13, No. 4, August 2023, pp. 3778~3787
ISSN: 2088-8708, DOI: 10.11591/ijece.v13i4.pp3778-3787

Design of 5.1 GHz ultra-low power and wide tuning range hybrid oscillator

Arunkumar Pundalik Chavan, Ravish Aradhya
Department of Electronics and Communication, RV College of Engineering, Bengaluru, India

Article Info

Article history:

Received Jul 31, 2022
Revised Sep 25, 2022
Accepted Oct 1, 2022

Keywords:

Output noise
Phase noise
Ring oscillator
Standard deviation
Tuning range

ABSTRACT

The objective of the proposed work is to demonstrate the use of a hybrid approach for the design of a voltage-controlled oscillator (VCO) which can lead to higher performance. The performance is improved in terms of the tuning range, frequency of oscillation, voltage swing, and power consumption. The proposed hybrid VCO is designed using an active load common source amplifier and current starved inverter that are cascaded alternatively to achieve low power consumption. The proposed VCO achieves a measured phase noise of -74 dBc/Hz and a figure of merit (FOM) of -152.6 dBc/Hz at a 1 MHz offset when running at 5.1 GHz frequency. The hybrid current starved-current starved VCO (CS-CS VCO) consumes a power of 289 µW using a 1.8 V supply and attains a wide tuning range of 96.98%. Hybrid VCO is designed using 0.09 µm complementary metal–oxide–semiconductor (CMOS) technology. To justify the robustness, reliability, and scalability of the circuit different corner analysis is performed through 500 runs of Monte-Carlo simulation.

Corresponding Author:

Arunkumar Pundalik Chavan
Department of Electronics and Communication Engineering, RV College of Engineering
Bengaluru, India
Email: arunkumarpc@rvce.edu.in

1. INTRODUCTION

Oscillators represents the basic building block of the electronic system used for generating a frequency of oscillation, frequency synthesis, frequency translation, and clock generation. The current trend is to replace bulky comparators employed in sigma-delta modulators with voltage-controlled oscillator-based (VCO) quantizers. The ideal VCO is used to generate high operating frequencies while varying control voltage. VCO is categorized into two types: i) inductor/capacitor (LC) oscillator-based and ii) ring oscillator (RO) based [1]. LC oscillator based VCO is constructed using a passive LC component as a resonator and active element to compensate for the loss of the resonator. The frequency of the LC oscillator is given by (1).

$$\omega_c = \frac{1}{\sqrt{LC}} \quad (1)$$

RO is constructed by a connecting chain of inverting amplifiers in a ring structure which is coupled with a positive feedback loop [2] as shown in Figure 1. Basic operation of RO relies on the propagation delay of a chain single inverter. If one of the output nodes of RO is excited then the pulse propagates through each inverting amplifier and eventually reverses the initial excited state.

For N-stage RO having propagation delay as t_d for single stage the frequency of the oscillation is given by (2) and the delay is given by (3).

$$f_{osc} = \frac{1}{2Nt_d} \quad (2)$$

$$t_d = \frac{V_{osc}C_L}{I_{ctrl}} \quad (3)$$

By substituting (3) in (2) frequency of oscillation [3] is obtained and given as (4),

$$f_{osc} = \frac{I_{ctrl}}{2NV_{osc}C_L} \quad (4)$$

where I_{ctrl} the current in the inverter N is the number of stages, V_{osc} is the voltage applied and is C_L is the load capacitance of the inverter. From [4] it is observed that oscillation frequency is inversely proportional to, oscillating amplitude, load capacitance, and many delay elements. Voltage-controlled oscillator-based analog to digital converter (ADC) has gained more interest in the latest trends because of its ease in implementation. The main drawback of VCO-based ADC is power dissipation, frequency of oscillation, and voltage swing. Askari and Saneei [4] describe a differential VCO design that achieves a wide tuning range and high frequency. The drawback of this design is high phase noise and large power consumption.

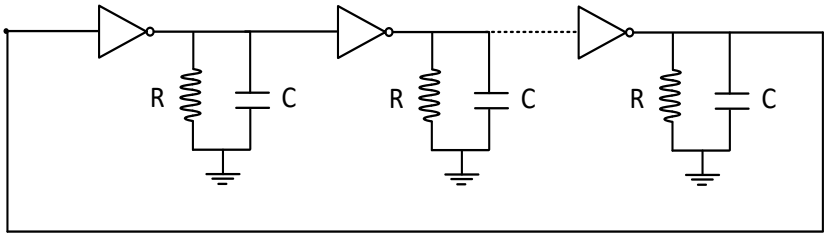

Figure 1. Basic N-stage RO structure

Straayer and Perrott [5] stated that existing LC oscillators have drawbacks such as large chip low tuning range, and high power dissipation. To overcome the drawbacks a complementary metal–oxide–semiconductor (CMOS) VCO is designed in [6] but it offers a low oscillation frequency. To boost the tuning range of frequency a new methodology is implemented [7]. It is observed that large output swing, power consumption is high. Elissati *et al*. [8] introduce a high-frequency VCO at a cost of a high power, figure of merit (FOM), and low tuning range. A novel ring oscillator topology is designed by Li *et al*. [9] measures high frequency of oscillation and high tuning range but consumes high power. Maiti *et al*. [10] developed a hybrid power efficient ring VCO giving penalty of lower frequency of oscillation and low tuning range. In [11] authors developed a ring oscillator based on the current source this design consumes less power but lacks in frequency tuning. In [12] author developed a design of current starved VCO that dissipates large power.

Taking into account limitations an attempt is made in this paper to design a novel ultra-low power, wide tuning range, and moderate phase noise hybrid current starved-current starved VCO (CS-CS VCO). The novelty of the paper lies in cascading of a common source with an active load inverter and current starved inverter that are cascaded alternatively to reduce the power dissipations and increase the frequency of oscillation and FOM. The article is organized as follows: The design of hybrid CS-CS VCO design and mathematical model is described in section 2 and section 3 respectively. Section 4 gives a detailed report of process voltage and temperature (PVT) analysis. A detailed comparative analysis is carried out in section 5. Finally, section 6 concludes the article.

2. PROPOSED HYBRID CS-CS VCO

The hybrid VCO is designed using two different types of delay elements: common source active load-based inverter and current starved inverter which are placed alternatively. Hybrid VCO is tested for five stages. In the proposed design stage 1, 3, and 5 are common source active load inverter and stage 2 and 4 current starved inverter is used as shown in Figure 2. To achieve a high frequency of oscillation and low power dissipation the aspect ratio of each MOSFET is calculated. Table 1 shows the device dimension to design hybrid VCO. Figure 3 shows the output transient response of the proposed VCO circuit.

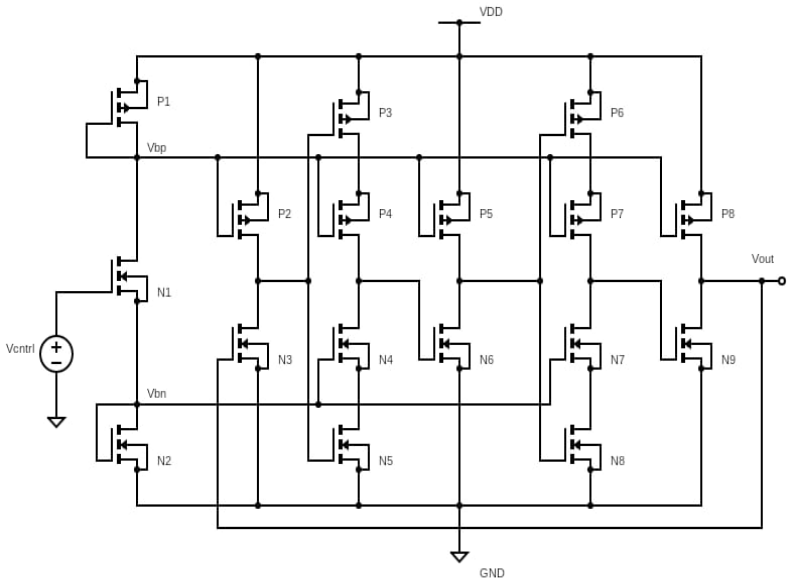

Figure 2. Proposed hybrid CS-CS VCO circuit

Table 1. Device dimension

Device Aspect Ratio (W/L)		
	NMOS	PMOS
N1	W=1 µm, L=100 nm	P1
N2	W=500 nm, L=100 nm	W=220 nm, L=100 nm
N3,N5,N6,N8,N9	W=120 nm, L=100 nm	P2-P8
N4,N7	W=500 nm, L=100 nm	W=120 nm, L=100 nm

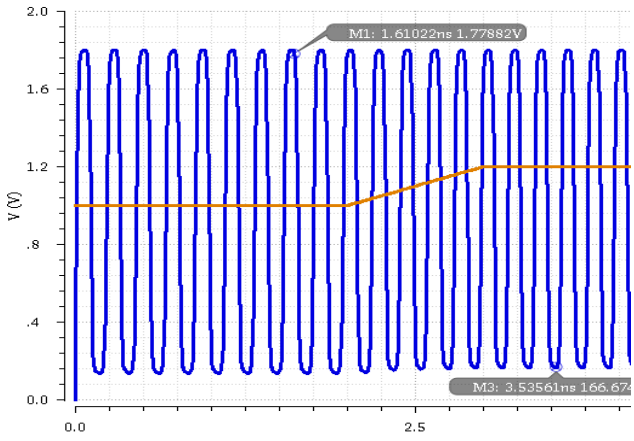

Figure 3. VCO transient analysis with control voltage

3. MATHEMATICAL MODEL FOR FREQUENCY ESTIMATION

The output oscillation frequency of CS-CS VCO is measured as a reciprocal of the total delay time of both inverters that are varied by control voltage in biasing circuit. The internal capacitance model of common source with active load and current starved inverter is shown in Figures 4(a) and (b) respectively. Figures 5(a) and (b) represents the ideal input and output of VCO respectively. The frequency of oscillation for hybrid CS-CS VCO is given in (5). where xd_{CSamp} and xd_{csps} is the delay of common source amplifier with active load and current starved respectively.

$$f_{osc} = \frac{1}{N_1 xd_{csamp} + N_2 xd_{csps}} \quad (5)$$

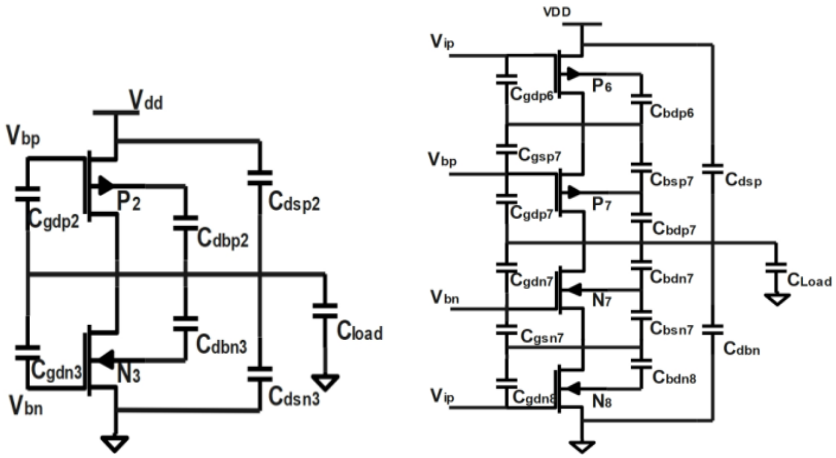

Figure 4. Capacitance model of inverter (a) common source with active load and (b) current starved inverter

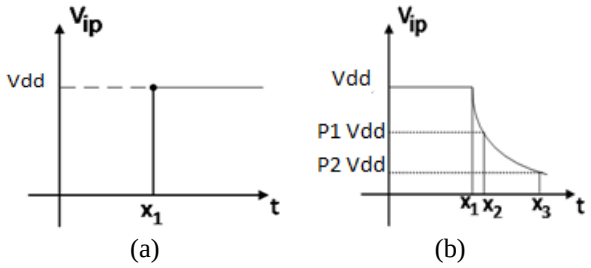

Figure 5. Ideal input and output [13] (a) ideal input pulse and (b) ideal output pulse

3.1. Calculation of delay in CS with active load

From the Figure 4(a), effective load capacitance is given in (6). Where cin_{csps} is the input capacitance of current starved inverter given in (7). Total delay of common source with active loading is given in (8).

$$c_{load} = c_{gdn1} + c_{gdp1} + c_{dbp1} + cin_{csps} \quad (6)$$

$$cin_{csps} = c_x\{(wl)_{n7} + (wl)_{n8} + (wl)_{p6} + (wl)_{p7}\} \quad (7)$$

$$xd_{CSamp} = x_{phl1} + x_{plh1} \quad (8)$$

x_{phl1} and x_{plh1} is the delay for high to low and low to high transition respectively. During high to low transition $x_2 - x_1$ and $x_3 - x_2$ is expressed in (9) and (10). By adding (9) and (10) high to low and low to high transition delay expressed in (12) and (13) respectively. The (12) and (13) in (8) we get total delay of common source with active load inverter.

$$x_2 - x_1 = \frac{c_{load}(1-p_1)v_{dd}}{\frac{1}{2}\mu_n c_{ox}\left(\frac{W}{l}\right)(v_{in}-v_{th})^2} \quad (9)$$

$$x_3 - x_2 = \frac{c_{load}}{\frac{1}{2}\mu_n c_{ox}\left(\frac{W}{l}\right)(v_{dd}-v_{th})^2} \ln\left[\frac{2p_1-p_2}{p_2}\right] \quad (10)$$

$$x_{phl1} = (x_2 - x_1) + (x_3 - x_2) \quad (11)$$

$$x_{phl1} = \frac{c_{load}(1-p_1)v_{dd}}{\frac{1}{2}\mu_n c_{ox}\left(\frac{W}{l}\right)(v_{in}-v_{th})^2} + \frac{c_{load}}{\frac{1}{2}\mu_n c_{ox}\left(\frac{W}{l}\right)(v_{dd}-v_{th})^2} \ln\left[\frac{2p_1-p_2}{p_2}\right] \quad (12)$$

$$x_{plh1} = \frac{c_{load}(1-p_1)v_{dd}}{\frac{1}{2}\mu_p c_{ox}\left(\frac{W}{l}\right)(v_{in}-v_{th})^2} + \frac{c_{load}}{\frac{1}{2}\mu_p c_{ox}\left(\frac{W}{l}\right)(v_{dd}-v_{th})^2} \ln\left[\frac{2p_1-p_2}{p_2}\right] \quad (13)$$

3.2. Calculation of delay in current starved inverter

From the circuit the gate voltage of transistor n7 and p7 is provided by bias circuit, in which node voltages are connected by p2 and n3. Total load capacitance of Figure 4(b) is represented in (14). Where c_2 is the load capacitance at the output node and cin_{cs}.

$$c_{l2} = c_{gdp6} + c_{gdp7} + c_{gdn7} + c_{gsn7} + c_{gdn8} + c_{bdp6} + c_{bsp7} + c_{bdp7} + c_{bdn7} + c_{bdn8} + c_{dsp1} + c_{dbn1} + c_2 + cin_{cs} \quad (14)$$

$$cin_{(cs)} = c_x\{(wl)_{n3} + (wl)_{p2}\} \quad (15)$$

$$xd_{CSPS} = x_{phl2} + x_{plh2} \quad (16)$$

$$x_2 - x_1 = \frac{c_{l2}(1-p_1)v_{dd}}{\frac{1}{2}\mu_n c_{ox}\left(\frac{W}{l}\right)_n(v_{gs4}-v_{th})^2} \quad (17)$$

$$x_3 - x_2 = \frac{c_{l2}}{\frac{1}{2}\mu_n c_{ox}\left(\frac{W}{l}\right)_n(v_{dd}-v_{th})}\ln\left[\frac{2p_1-p_2}{p2}\right] \quad (18)$$

$$x_{phl2} = (x_2 - x_1) + (x_3 - x_2) \quad (19)$$

$$x_{phl2} = \frac{c_{l2}(1-p_1)v_{dd}}{\mu_n c_{ox}\left(\frac{W}{l}\right)_{n7}(v_{gs4}-v_{th})^2} + \frac{c_{l2}}{\mu_n c_{ox}\left(\frac{W}{l}\right)_{n8}(v_{ss}-v_{th})}\ln\left[\frac{2y_1-y_2}{y_2}\right] \quad (20)$$

$$x_{plh2} = \frac{c_{l2}(1-k_1)v_{ss}}{\mu_p c_{ox}\left(\frac{W}{l}\right)_{p7}(v_{gs4}-v_{th})^2} + \frac{c_{l2}}{\mu_p c_{ox}\left(\frac{W}{l}\right)_{p8}(v_{dd}-v_{th})}\ln\left[\frac{2p_1-p_2}{p_2}\right] \quad (21)$$

By substituting (20) and (21) in (16) the total delay of current starved inverter. Oscillation frequency of proposed hybrid VCO is calculated by substituting final expression of (16) and (8) in (5). From the (5) it can be stated that frequency of oscillation is inversely proportional to time delay of individual inverter.

4. MEASUREMENT RESULT

The performance metric for hybrid-based VCO is computed for simulation to analyze the percentage of alteration in metric. The proposed hybrid-based VCO is designed on a cadence platform using a 90 nm CMOS technology process with a supply voltage of 1.8 V. The proposed hybrid VCO is tested for different process corners, voltage, and temperature.

4.1. High frequency oscillation and gain of VCO

The proposed hybrid VCO produces an oscillation frequency of 5.1 GHz. Figure 6 gives the variation of frequency with a variation of Vctrl voltage. Table 2 presents a device parameter used to analyze the frequency of oscillation. Figure 7 shows the oscillation frequency histogram plot measured for 500 runs of Monte Carlo simulation. From the plot, it is observed that the variation of frequency is ranging from 4.49 to 5.46 GHz with a standard deviation of 189 MHz.

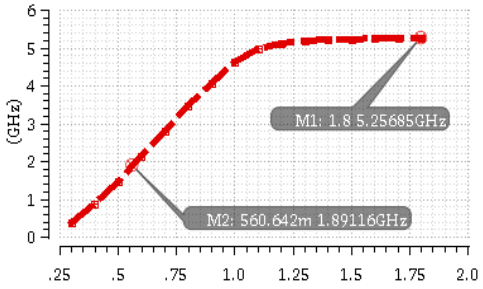

Figure 6. Frequency plot with variation of Vctrl

Table 2. Device parameter

Parameter	Value	Parameter	Value
Technology	90nm	µnCox	0.62*10-4
Supply Voltage	1.8V	Number of stages (N)	5
µpCox	0.87*10-4	Vthn	0.212 V
µnCox	0.62*10-4	Vthp	0.226 V

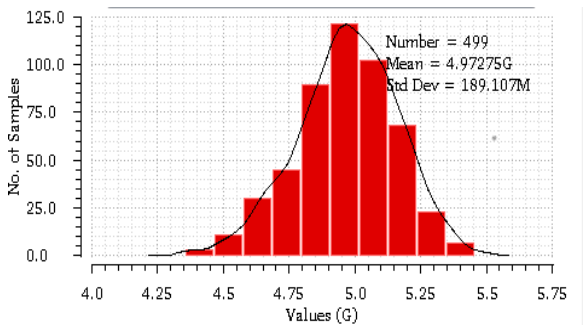

Figure 7. Histogram of oscillation frequency

The gain of the VCO is also called tuning sensitivity, it is denoted as KVCO. Tuning sensitivity is the ratio of varying in the frequency of oscillation with respect to varying in control voltage, it is expressed in (22). In Figure 8 the slope is a tuning sensitivity of a hybrid VCO, the value of KVCO is found 6.60 GHz/V. Control voltage is varied from 1 to 1.8 V tuning sensitivity also changes from 4.5 to 6.60 GHz/V.

$$K_{vco} = \frac{\Delta f_{osc}}{\Delta V_{ctrl}} \quad (22)$$

4.2. Frequency of oscillation as a function of temperature

Figure 9 represents the variation of frequency with change in temperature of hybrid VCO. Temperature is varied from -27 °C to 97 °C that reflects in decreasing of frequency from 6.3 to 4.3 GHz. Average power of the circuit decreases as increase in temperature. The average power decrease from 440 µW to 330 µW from -27 °C to 87 °C for Vctrl=1.2 V.

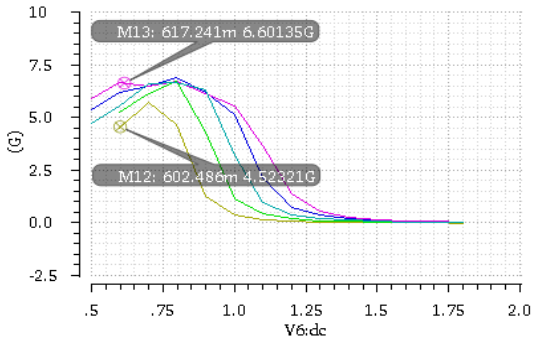

Figure 8. VCO tuning sensitivity versus Vctrl for different voltage

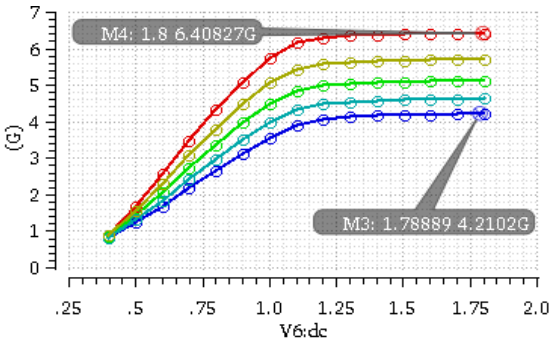

Figure 9. Variation of frequency with temperature

4.3. Best case/worst case analysis

The hybrid VCO is analyzed for the entire process corner from best case to the worst case. From the Table 3, it is observed as best fast-fast (FF) corner to the worst slow-slow (SS) corner have an alteration of 49.27% and 43.43% in average power and frequency of oscillation. The Histogram plot for average power and phase noise are plotted in Figures 10 and 11 that is obtained through 500 runs of Monte Carlo runs of NN corner (27 °C). Power, oscillating frequency and phase noise is found to be unaffected from zero skew to 5% skew simulation.

Table 3. Power, frequency of oscillation and phase noise @1Mhz offset frequency

Process Corner		No Skew		5% Process Skew					
		Power (mW)	F_{osc} (GHz)	Power (µW)		F_{osc} (Hz)		Phase Noise (dBc/Hz)	
				X	Σ	X	Σ	X	Σ
Pre Layout	NN	0.308	4.64	309.4	23.584	4.96G	187.335M	-69.64	0.678
	SS	0.192	3.055	193.56	16.034	3.44G	141.77M	-73.91	0.576
	SF	0.234	3.66	236.39	21.432	3.81G	222.92M	-68.30	0.984
	FS	0.320	4.859	319.185	19.328	4.82G	179.05M	-69.56	0.420
	FF	0.442	6.20	442.1	30.47	6.4G	230.766M	-66.90	0.789

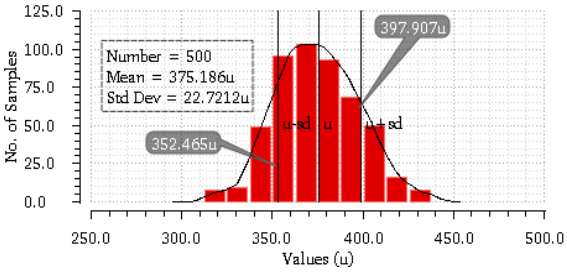

Figure 10. Histogram of average power

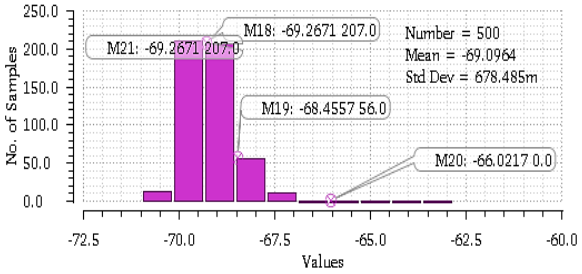

Figure 11. Histogram of phase noise

The output noise plot between Vn versus V/sqrtHz is shown in Figure 12. The output noise value is varied between different values of Vdd. from the plot its observed that for all supply voltages the noise saturates after about 2 KHz. Hence, it is known as white noise or Johnson noise and it is one of the most difficult noises to filter out. At 5.2 GHz the output noise is found to be 25 nV/sqrtHz. which is very small compared to output amplitude so output noise does not impact much. For the proposed design the output swing ranges between 70 mV to 1.78 V.

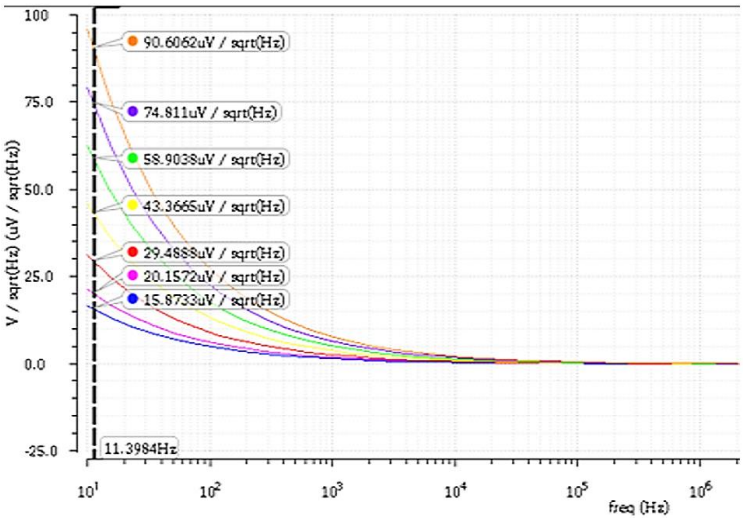

Figure 12. Plot of output noise

4.4. Effect of Vctrl sweep

Performance metric gets affected as we vary control voltage for different supply voltage. We observed that power dissipation for Vctrl=0.6 V is low because of phase control transition in the pull up network of common source amplifier with active load and current starved inverter. From Figure 13, it is observed that output frequency is directly proportional to Vctrl voltage. For Vctrl=0.4 V the frequency is found to be 890 MHz and for Vctrl=1.8 V the frequency is found to be 5.25 GHz. Figure also proves the frequency will vary with varying supply voltage.

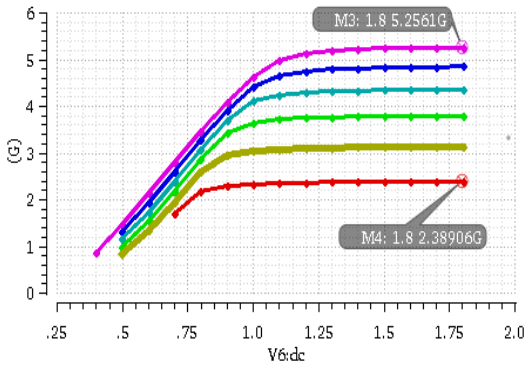

Figure 13. Vctrl versus frequency with variation of supply voltage

4.5. Performance metric as a function with number of stages

Hybrid VCO is tested for different number of stages varied from 5 to 11 to observe the result deviation and it is summarized in Table 4. From the table it is observed that as there is increase in number of stages from 5 to 11 the maximum frequency of oscillation decreases from 6.2 to 2.68 GHz, frequency tuning range gradually decreases as we increase the stages of VCO. Proposed 5 stage hybrid VCO achieves a tunning range of 96.98%.

Table 4. Performance metrics of hybrid VCO v/s of number of stages

No. of stages	Simulation	Frequency Range	Tuning Range %	Max VCO Gain (GHz/V)	Performance Metric @ V_{cntrl}=1.2 V, V_{dd}=1.8V	
					Average Power	Maximum Frequency
5	Pre-Layout	179.7 MHz-5.93 GHz	96.98	6.58 GHz/V @0.85 V	308 µW	6.2 GHz
7	Pre-Layout	507.6 MHz-4.5 GHz	88.73	4.62 GHz/V @0.8 V	346 µW	4.12 GHz
9	Pre-Layout	386.7 MHz-3.693 GHz	89.54	3.51 GHz/V @0.8 V	311 µW	3.09 GHz
11	Pre-Layout	561 MHz-2.168 GHz	74.15	2.83 GHz/V @0.8 V	343 µW	2.68 GHz

4.6. Eye diagram

The eye diagram is plotted to calculate the jitter and the maximum and minimum output swing of VCO. The eye height and eye width determine the sensitivity of output noise margin and timing jitter. From Figure 14 the eye height is found to be 1.62 V and the eye width is 0.331 V. The jitter range was found to be 7 to 27 ps. For the proposed VCO we can observe that logic 'low' and logic 'High' does not seem to overlap. From the eye diagram, it is observed that the eye-opening point is twice the clock period (2*79) ps and subsequently oscillating frequency of approximately 6.2 GHz.

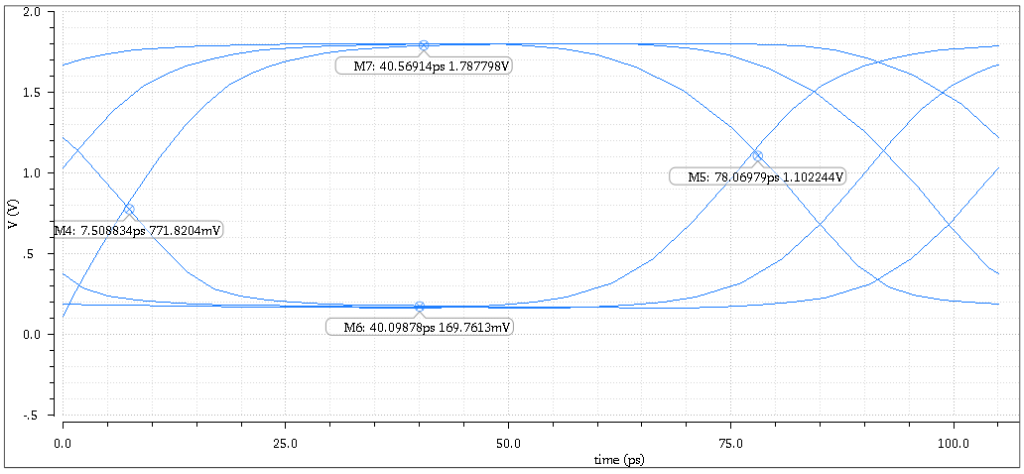

Figure 14. Simulated eye diagram plot for output

5. PERFORMANCE COMPARISON

The proposed VCO design is compared with different existing models presented in literature and results are tabulated in Table 5. Finally, it is observed that the proposed work has extensively improved in terms of average power and oscillating frequency. The hybrid VCO dissipates 97.5%, 90.37%, 90.37%, 75%, 62.5%, 99.2%, 6.4%, 63.3%, 95.8%, 68.88%, 95.1%, 63.6%, 98.6% and 77.5% lesser power compared to [13]–[27]. The proposed design not only increases the tuning range but also the high frequency of oscillation. The trade-off of the design is the effect of phase noise is detected to be less compared to the previous work.

Table 5. Performance summary with previously published VCO

Parameter	Process (nm)	Supply (V)	Average power (mW)	Phase noise (dBc/Hz)	Oscillation frequency (GHz)	Tuning range (%)
[14]	90	1.2	12	-109	15	14
[15]	90	1.3	3	-116	20.8	4.2
[16]	90	0.6	3	-114	19	8.2
[17]	90	0.5	1.16	-87	2.24	90
[18]	90	0.6	0.771	-89	0.48	94
[19]	90	0.7	37	-96	1	63.2
[20]	90	2.5	-	-	2.54	--
[21]	90	1	0.31	-105	0.45	--
[11]	90	1.1	0.79	-113	1	24
[13]	90	1.2	0.047	-115	2.46	95.4
[22]	90	1	7	-88	8	65
[23]	90	1.2	0.9	-94	2.4	70
[24]	90	1	18	-80	10	70
[25]	90	1.2	0.77	-87	2.3	67
[26]	90	1.2	22	-85	11.8	67
[27]	90	1	1.29	-102	5.9	80
Proposed work	90	1.8	0.289	-73.08	5.1	96.98

6. CONCLUSION

In this proposed work, a novel ultra-low-power hybrid CS-CS based VCO is proposed using 0.09 µm technology with 1.8V supply. This design is extensively better in terms of output frequency, low power and tuning range compared to other VCO circuits. The complete VCO is tested for five different corners through 500 runs of Monte Carlo in both 'zero skew' and 5% process skew. The design results with power dissipation of 289 µW.

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BIOGRAPHIES OF AUTHORS

Arunkumar Pundalik Chavan received the B.Eng. degree in electronics and communication engineering from BV Boomraddi College, India, in 2010 and the M.Tech. Degree in electric VLSI design and Embedded System from RV College of Engineering, India, in 2011. Currently, he is an Assistant Professor at the Department of Electronics and Communication Engineering, RV College of Engineering. His research interests include low power VLSI, analog VLSI design, and digital VLSI design. He can be contacted at email: arunkumarpc@rvce.edu.in, chavanarunkumar@gmail.com.

Ravish Aradhya born on March, 27th, 1969 in Karnataka, India, obtained his BE degree in Electronics from RV College of Engineering in 1991, ME degree in Electronics from University Visvesvaraya college of Engineering, Bangalore, in 1995, and Ph.D. degree from Visvesvaraya Technological University, Belagavi, India in 2014. He is currently serving RV College of Engineering, Bangalore 560 059, as professor in Electronics and Communication Engineering Department the past 23 years. With a vast 26 years of teaching experience, he has thirteen text books written/adapted/reviewed for leading publishers like McGraw-Hill and Pearson Education, guided many undergraduate and post graduate projects. He can be contacted at email: ravisharadhya@rvce.edu.in.