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Design and optimization of high electron mobility transistor with high-k dielectric material integration

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ABSTRACT

We have developed and simulated a high electron mobility transistor (HEMT) operating in the 5 nm regime. This HEMT uses hafnium oxide (HfO_2), a high-k dielectric material, to create an undoped region (UR) beneath the gate. While the gate and undoped regions share equal thickness, the channel length differs. This innovative undoped under the gate dielectric HEMT design mitigates the maximum electric field (V) within the channel area, leading to a significant increase in drain current. The utilization of a high-k dielectric in the HEMT structure results in a saturated Ion current that is 60% higher compared to conventional structures. Specifically, we use an AlGaN/GaN/SiC-based HEMT with an intrinsic section below the gate, using HfO2 as the high-k dielectric substantial, for applications requiring high power and high-frequency power amplifiers. Compare this advanced HEMT design to conventional HEMTs and you will see improved conductivity, a greater drain current (I_d), a 54% increase in transconductance (Gm), and a lower on-resistance (R_{on}). Additionally, advancements in the electric field in the Y direction are seen. This HEMT structure exhibits superior performance compared to alternative materials analyzed. The integration of AlGaN/GaN materials in HEMTs opens up extensive opportunities in the realms of radio frequency very large-scale integration (VLSI) and power electronics.

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1. INTRODUCTION

As innovation progresses every year, there is a critical interest for very large-scale integration (VLSI) gadgets, particularly as device dimensions shrink to nanometer scale, making short channel effects more pronounced. Because channel lengths in submicron technology are less than 5 nm, decreasing gate lengths and the accompanying rise of undesired situations like drain induced barrier lowering (DIBL) require novel techniques to manage nanodevices. In nanoscale technology, architectures such as the double gate (DG), triple gate (TG), and gate all around (GAA) offer better scalability than conventional devices to reduce these short channel effects [1], [2].

When compared to high electron mobility transistors (HEMTs), traditional metal oxide semiconductor field effect transistors (MOSFETs) are usually thought of as moderately slower devices. As a result, Gallium

nitride (GaN) HEMT devices show excellent thermal conductivity and stability along with a greater bandgap, higher critical electric field, and increased electron drift velocity [3], [4]. III-V bandgap semiconductors like gallium and aluminum nitride, as well as low-k dielectric materials like silicon dioxide (SiO_2) and high-k dielectric materials like hafnium oxide (HfO_2), are used in optoelectronic devices, especially high-power ones [5]. The heterostructure of Gallium nitride HEMT enables an undoped channel, leading to higher breakdown voltages owing to the utilization of higher bandgap semiconductors like Gallium nitride, as well as low-k dielectric materials like silicon dioxide and high-k dielectric materials like hafnium oxide [6], [7].

One particular kind of heterostructure field effect transistor (H-FET) is the high electron mobility transistor (HEMT), renowned for its exceptional performance at RF and microwave frequencies, coupled with a lower noise figure [8]. Operating on the principle of a two-dimensional electron gas within its heterostructure, HEMTs experience fewer electron collisions, contributing to their efficacy. Because HEMTs have a high on-current (Ion) at lower gate voltages (VGS), they are a good choice for a variety of radio frequency design applications, such as radar communications, broadcast radio receivers, and cellular mobile telecommunications [9], [10].

Due to their exceptional material properties, such as their high electron saturation velocity, high breakdown electric field, and efficient underlap implementation of gate induced drain lowering (GIDL) mitigation, Gallium nitride-based high electron mobility transistors (GaN-HEMTs) are widely used. Unfortunately, the underlap approach shortens the gate's effective length, which deteriorates the gate manageability of silicon dioxide (SiO_2) and silicon (S_i) based HEMT devices and clearly lowers the on-current (Ion) [11].

Gallium nitride-based HEMTs operate effectively without doping due to their high carrier concentration, which minimizes dopant scattering and ensures a more uniform distribution of dopants. However, the significant concern with GaN-based HEMTs is the self-heating effect resulting from increased channel temperature. Continuous efforts are underway to reduce thermal resistance and mitigate this consequence in the expedient, particularly in nanodevices. GaN-based HEMTs are lethargy to utilizing different dielectric materials in order to solve the thermal resistance and self-heating consequence. The most preferred dielectric materials among them include silicon (S_i), silicon dioxide (SiO_2), silicon carbide (6H-SiC), silicon nitride (SiN), and high-k dielectric material like helium oxide (HfO_2). Specifically, Silicon Carbide (6H-SiC) efficiently reduces leakage current in the device by forming a high-quality interface with GaN-HEMTs [12], [13].

The outline of the paper structure is as follows: The model of an intrinsic 5 nm regime gate HEMT is covered in detail in the second section. This includes mesh view, potential distribution and electric field analysis. Subsequently, the Results are shown in the third part along with performance comparisons of different materials. Lastly, the final section discusses the conclusion.

2. DEVICE STRUCTURE AND SIMULATION PARAMETERS

Figure 1 depicts the planned high electron mobility transistor (HEMT) operating within the 5 nm gate regime, featuring an undoped region referred to as U-HEMT. This innovative device incorporates high-k dielectric material, specifically hafnium oxide (HfO_2), with dimensions restrained in millimicrons using the Silvaco TCAD ATLAS simulator [14], [15]. Noteworthy is the inclusion of an undoped region with HfO_2, setting it apart from conventional devices. The gate length is given as L_g=0.005 μm, and the work function of the metal gate is 4.87 eV. Other dimensions include gate-source spacing (L_{gs}=0.015 μm), length (L_d=0.032 μm), gate-drain spacing (L_{ds}=0.015 μm), and undoped HfO_2 region length (L_u=0.08 μm). The undoped region beneath the gate effectively reduces the electric field within the channel region, leading to a significant increase in drain current [16]. Figure 2 illustrates the mesh view of the undoped HEMT, showcasing non-uniform grid spacing along both axes. Additionally, Figures 3 and 4 depict potential distributions and the electric field of the new structure, respectively. The device's speed and performance parameters are intricately tied to the gate length, with channel doping influencing drain current levels. Utilizing the Silvaco ATLAS Simulator, simulation of the undoped HEMT within the 5nm gate regime, employing HfO_2 as the high-k dielectric material, is conducted to extract all pertinent electrical parameters. It is noteworthy that in this suggested configuration, silicon (S_i) replaced by silicon carbide (6H-SiC) of serves as the substrate [17], [18].

Using the ATLAS simulator, the direct current (DC) and radio frequency (RF) properties of the Undoped HEMT with HfO_2 are investigated for several material combinations. A fixed gate length of 0.005 μm is used [19], [20]. Table 1 displays the dimensions of the undoped HEMT device, with particular emphasis on the crucial parameter of Gate length (5 nm). The high-k, 5 nm regime gate HEMT employs diverse materials and simulation methods, as outlined in Tables 2 and 3.

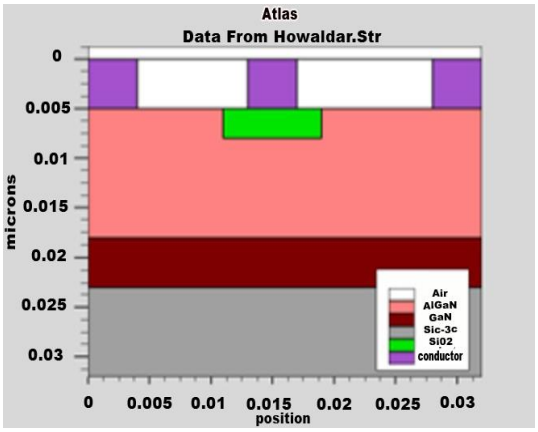

Figure 1. Proposed structure

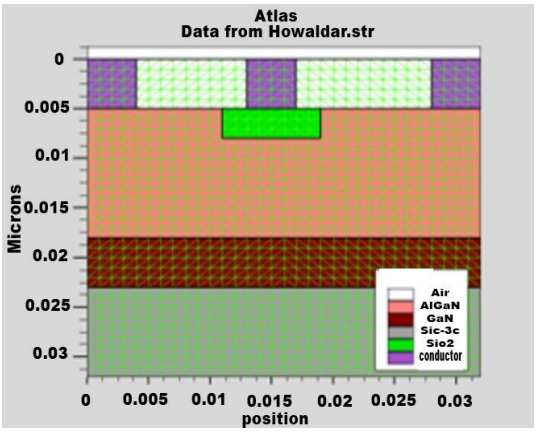

Figure 2. View of the planned structure in mesh

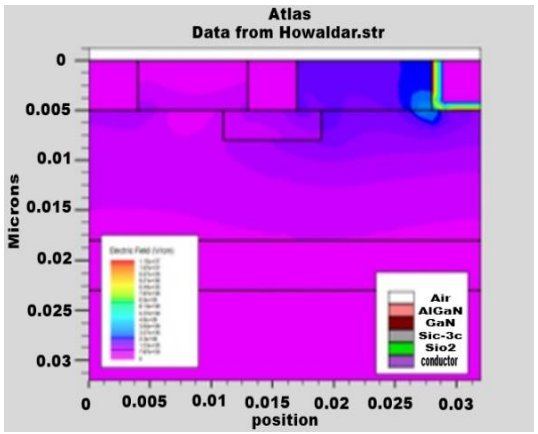

Figure 3. Electric field distribution of purported structure

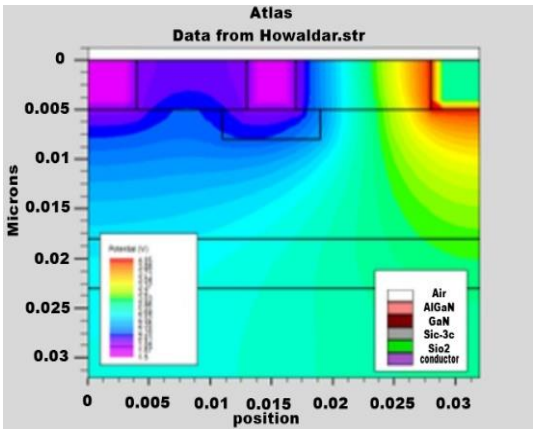

Figure 4. Potential scattering of proposed structure

Table 1. Utilized parameters for the suggested structure

Parameter	Notation	Values
Device length	LD	0.036 µm
Channel length	L_g	0.006 µm
Gate space to source	L_{gs}	0.016 µm
Drain space to gate	L_{gd}	0.014 µm
Undoped region length	L_s	0.006 µm
Source length	L_s	0.006 um
Drain length	L_d	0.004 um
work function=4.82eV		

Table 2. Used processes for simulation of proposed device

Technique Pattern	Description
Gummel	Used as solution technique
Newton trap	SHJ models and SIS models
Maxtrap	Method statement and trap is enabled
Gummel	Structural information is preserved after each iteration

Table 3. Models used for the simulation

Material model	Description
conmob	Concentration Dependent model
srh	carrier lifetimes model
auger	high current densities model

3. SIMULATION RESULTS AND DISCUSSION

When the gate voltage (VG) falls below the threshold voltage (Vt), minority carriers flow from the source and the off-state of the device is indicated, resulting in a subthreshold current [21]. Conversely, when the gate voltage (VG) surpasses the threshold voltage (Vt), the device transitions to the ON state, prompting the flow of drain current (Id) versus drain voltage (Vd) for various material combinations, as illustrated in Figure 5 [22], [23].

Figure 6 illustrates the drain current of the intrinsic area utilizing a 5 nm gate and high-k dielectric factual, specifically hafnium oxide (HfO_2), within the HEMT, with the gate length fixed at 5 nm. It is noted that the leakage current (Ioff) remains constant [24], [25]. Notably, Figure 6 demonstrates that the AlGaN/GaN/SiC combination yields a higher ON current compared to other material combinations [26].

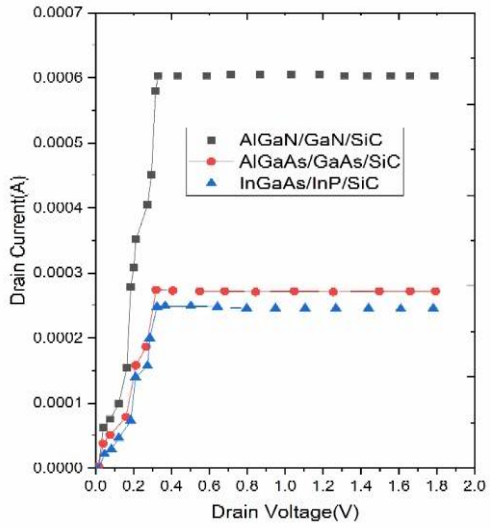

Figure 5. Id vs Vd for different dielectric materials

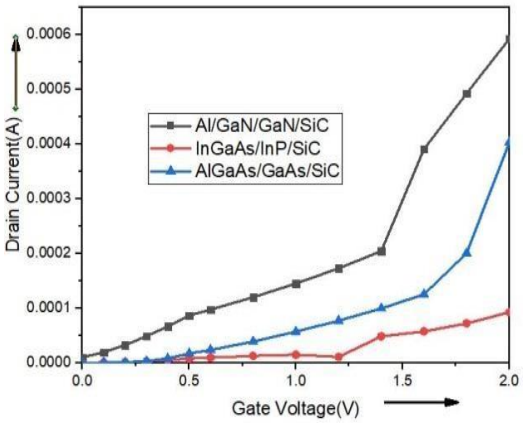

Figure 6. Id vs Vgs for different dielectric materials

3.1. Variation of drain current and drain conductance

Figure 7 illustrates the drain conductance (G_d) across different drain voltages. It is evident that the AlGaN/GaN/SiC combination exhibits enhanced drain conductance compared to other material combinations [27].

$$Drain\ Conductance\ (G_d) = \frac{\delta I_{ds}}{\delta V_{ds}}$$

3.2. Variation of transconductance

High transconductance is necessary to get the right amplifier gain; Figure 8 [28] shows how this varies with gate voltages (V_{gs}).

$$Transconductance\ (G_m) = \frac{\delta I_{ds}}{\delta V_{gs}}$$

Figure 9 presents plotting the simulated drain voltage (V_d) against on-resistance (Ron). For all materials, it is found that the equivalent on-resistance reduces as drain conductance rises [29]. The electric field dissemination of the suggested intrinsic HEMT device using HfO2 beneath 5 nm regime gate is shown in Figure 10. It is evident that the electric field concentration in the undoped HEMT has been enhanced compared to conventional devices [30]. Table 4 lists the suggested HEMT's performance specifications. The data obtained clearly show that the AlGaN/GaN/SiC HEMT performs better than the other two material HEMT constructions.

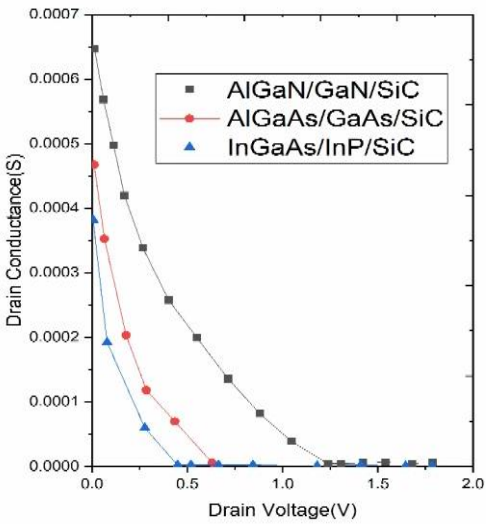

Figure 7. Gd vs Vds for different dielectric materials

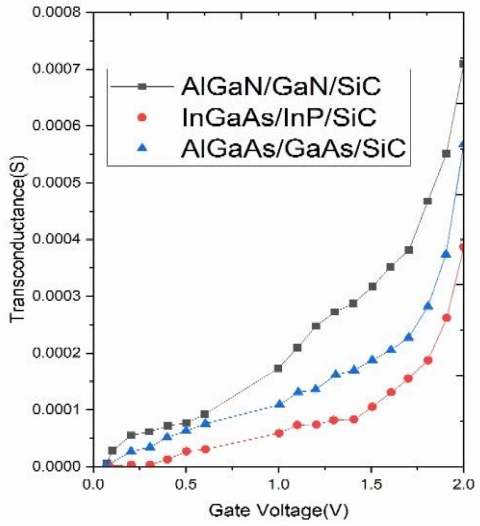

Figure 8. Drain conductance vs gate voltage for different materials

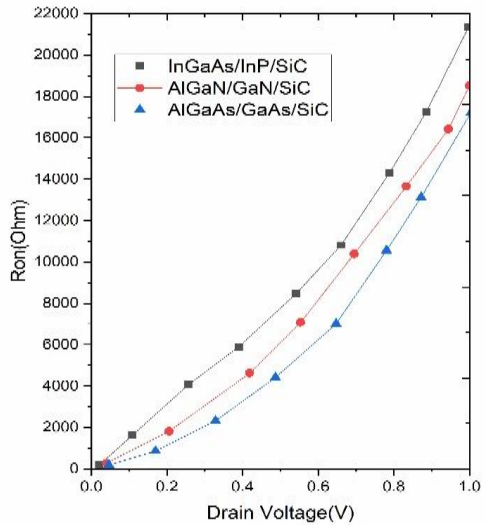

Figure 9. Ron vs Vds for different dielectric materials

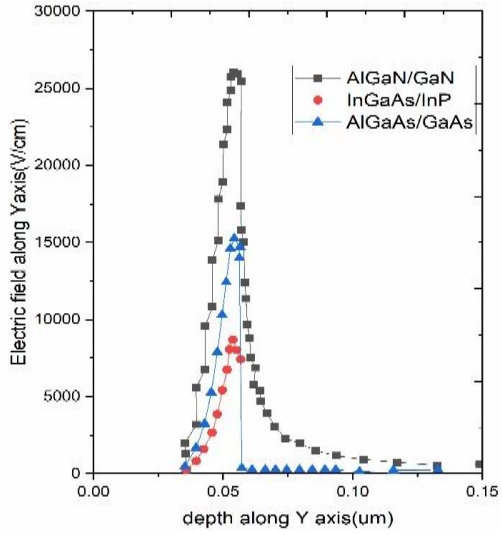

Figure 10. Electric field for different dielectric materials

Table 4. Performance metrics for obtained results

Parameter	AlGaN/GaN/ SiC	AlGaAs/ GaAs/SiC	InGaAs/InP/SiC
Ion(A)	5.041	1.8	2.12
Ioff(A)	1.01	2.8	9.17
Ion/Ioff	4.19	0.59	.24
Gd(S)	6.18	4.51	4.01
Ron(ohms)	1.17	2.1	2.12
Vth(V)	0.8	0.36	0.6
Gm(S)	8.02	6.12	4.16

4. CONCLUSION

Using the Silvaco TCAD ATLAS simulator, the research presents the design and simulation of an advanced high electron mobility transistor (HEMT) operating in the 5nm gate regime. This new HEMT structure has an undoped area below the gate and uses hafnium oxide (HfO_2) as a high-k dielectric material. The substrate is silicon carbide (SiC) and the channel is AlGaN. With HfO_2 serving as the high-k dielectric material below the gate, the GaN-based advanced HEMT exhibits a number of noteworthy performance improvements, such as higher on-current (Ion), a higher Ion/Ioff ratio, higher transconductance, lower ON resistance, and improved drain conductance. Consequently, the suggested HEMT device employing HfO_2 as the high-k dielectric material beneath the gate emerges as the preferred choice for high-power and high-frequency applications.

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