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Single-phase transformerless inverter topologies at different levels for a photovoltaic system, with proportional resonant controller

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ABSTRACT

In this paper, we have studied the topologies of single-phase transformerless inverters with different levels using a proportional-integral-resonant (PIR) AC controller, and the multi-level cascade inverter topology with sinusoidal pulse with modulation (SPWM) control in an open and closed loop. To ensure that these photovoltaic inverters can inject a defined amount of reactive power into the grid according to international regulations. Therefore, precise monitoring of the mains voltage vector by a phase-locked loop (PLL) system is applied to ensure the proper functioning of this system. For inverter topologies with less than three levels, the simulation results show that the highly efficient and reliable inverter concept (HERIC) topology performance is better than that of H5 and H6. On the other hand, the performance of the topology H6 ameliorate is superior to those of H4, H5, and HERIC in currents of leakage. On the other hand, for the control of cascaded multi-level closed-loop inverters, we notice that there is an improvement in the spectra and the elimination of all frequency harmonics, close to that of the fundamental, and a reduction in the rate of harmonic current distortion.

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1. INTRODUCTION

Recently, the use of high-power inverters has increased at various levels due to the inability to supply electricity. In addition, the photovoltaic (PV) module and grid are separated to prevent electric leakage. Therefore, it considers the importance of the efficiency and price of the PV system at the conversion stage [1], [2]. However, an inverter with a transformer provides multiple power stages that reduce efficiency and complicate the system [3], [4]. As a result, the inductance of the output filter and the power supply impedance form an oscillator circuit [5], [6]. Leakage current increases all harmonics and power loss supplied to the grid [7], [8]. To reduce leakage current, we proposed a full-bridge inverter with bipolar sinusoidal control (SPWM) [9], [10]. Therefore, multi-level converters are various types of arrays that are provided for high-power applications due to the overall efficiency of high-level output signals and output waveforms and produce the desired AC output in multi-level inverters [11], [12]. The integral part (I) is added to the proportional resonance controller (PR) to allow tracking of alternating current (AC) and direct

current (DC) components. It also allows the cancellation of DC disturbances caused by voltage source inverters, non-idealities, and non-linear loads [13], [14].

Therefore, close monitoring of the line voltage vector by the phase-locked loop (PLL) system is required to ensure that the control strategy works properly [15]–[17]. In this article, we analyze the study of grid-connected, transformerless single-phase inverters and compare them in terms of total harmonic distortion (THD). Finally, an improved H6 topology is proposed. On the other hand, the second purpose of this work is to study and improve the control of 5-level single-phase cascade inverters for photovoltaic applications. After reviewing the multi-level cascade inverter topology, select the optimal topology (5 levels) [18], [19]. The following is a simulation of this topology using pulse width modulation (PWM)-based control in an open-controlled control loop with various controls, especially the resonant proportional controller PR [20], [21].

2. A BLOCK DIAGRAMS OF PHOTOVOLTAIC SYSTEM INVERTTER AND PR CONTROLLER

2.1. Block diagrams of system

Figure 1 indicates the diagram of our system. Since the output signal of the PV panel is very low, it is practically impossible to keep a large number of panels because it is not economical. An additional increase stage is important to elevate the voltage level. For low-power applications, an inverter full-bridge single phase is proposed, though its efficiency is very low.

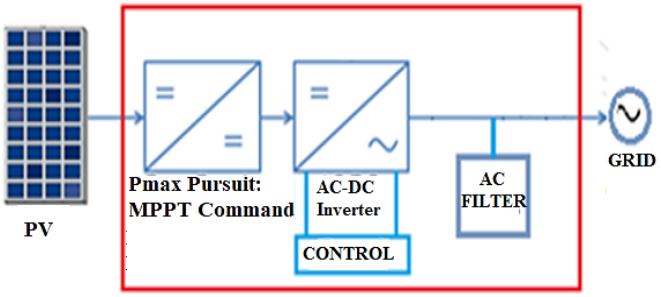


Figure 1. Block diagrams of photovoltaic system inverter

2.2. PR control

The PR current controller GPR(s) is represented by:

$$GPR(s) = KP + KI\frac{S}{S^2+\omega 0^2} \quad (1)$$

Whenever *KP* and *KI* are the proportional and integral gain terms respectively. The proportional-integral-resonant (PIR) controllers have so far been typically employed in synchronous-frame-based AC current control with unbalanced voltage transients [22], [23]. The current controller, which is more suited to operate with sinusoidal references, is the PR controller.

2.3. Transport delay based PLL block

For different multi-level inverters, several approaches can be used in this case. To generate a quadrature signal, you must use a transport delay block. The latter can introduce a 90-degree phase shift with respect to the fundamental frequency of the input signal as shown in Figure 2 [24], [25].

2.4. Multi-level structure: case of the single-phase inverter cascade with five levels

The five-level cascade inverter consists of a series of two single-phase inverters in 3-level bridges (H-bridge). This inverter is made up of eight switches. Each switch constitutes a transistor-controlled complementary. Figure 3 indicates the structure of a five-level single-phase inverter, it consists of eight switches and two voltage sources (similar to two 80 V photovoltaic batteries). The load is linear of the inductive type (similar to an AC motor), in order to visualize the output signals at the terminals of the load. The control circuit comprises a sinusoidal generator supplying the reference signal Vref of frequency 50 Hz, and four triangular generators supplying carrier signals of frequency 5 kHz, with comparators, which generate the control signals.

Table 1 shows the output voltage for each of the five-level cascade inverter configurations. The control circuit of this inverter comprises a sinusoidal generator supplying the reference signal Vref of frequency 50 Hz and four triangular generators supplying carrier signals of frequency 20,000 Hz, with comparators, which generate the control signals.

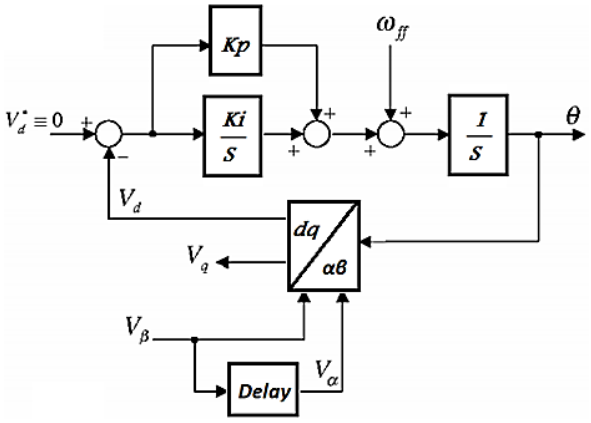


Figure 2. A transport delay PLL block

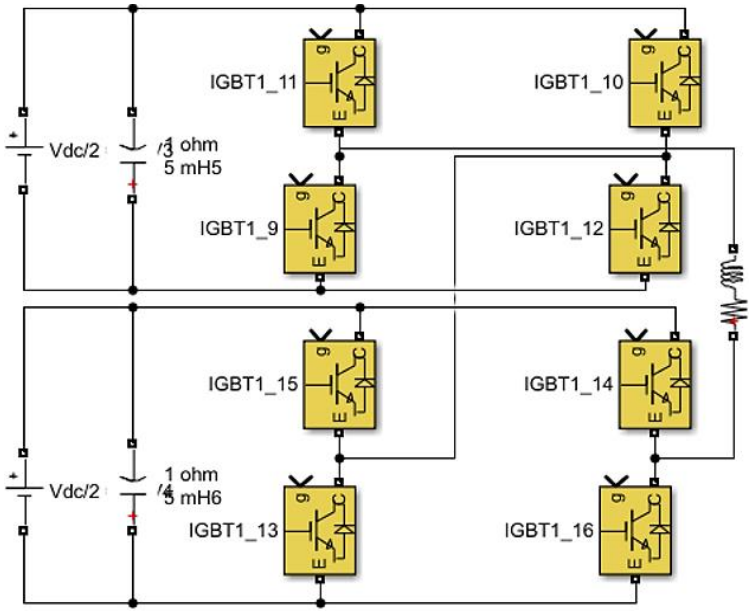


Figure 3. Structure of the five-level cascade inverter

Table 1. Output voltage for each of the five-level cascade inverter configurations

Switches	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	V_s output voltage
State of Each Switches	1	0	0	1	1	0	0	1	$2V_{dc}$
	1	0	0	1	0	1	0	1	V_{dc}
	0	1	0	1	0	1	0	1	0
	0	1	0	1	0	1	1	0	$-V_{dc}$
	0	1	1	0	0	1	1	0	$-2V_{dc}$

3. SIMULATION RESULTS

3.1. Simulation and output result of H4 topology

The H4 topology in the Figure 4 consists of four active switches (S1-S4) with antiparallel body diodes (D1-D4). The diode completes the current path during the freewheeling period. By applying different

unipolar, and hybrid modulations, the system creates three voltage levels throughout the filter. Bipolar modulation, on the other hand, can be used to generate two voltage levels with high core loss as presented in the Figure 5(a). According to Figure 5(a) it can be seen that the output signal of the current and the voltage at the terminal of the load are purely sinusoidal and equal to the value of the reference voltage. Therefore, the harmonics are eliminated; bipolar sinusoidal pulse width modulation eliminates losses. The resulting current is almost sinusoidal with a current harmonic distortion factor of 2.39% as shown in Figure 5(b).

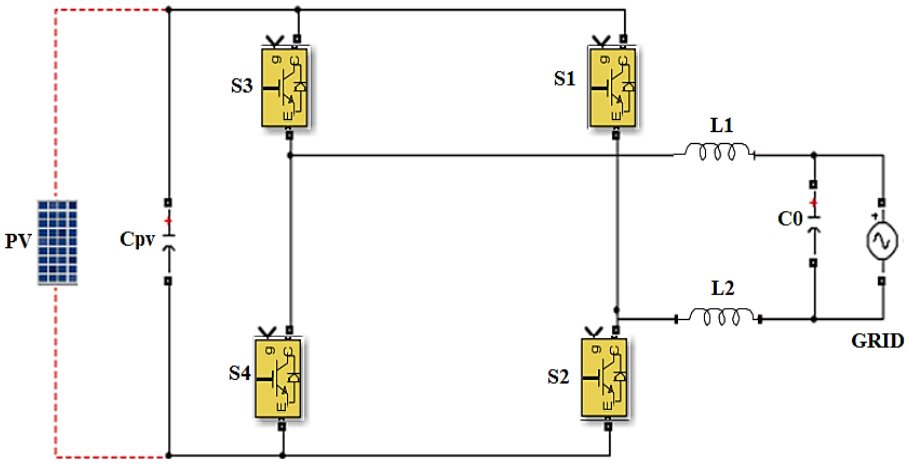
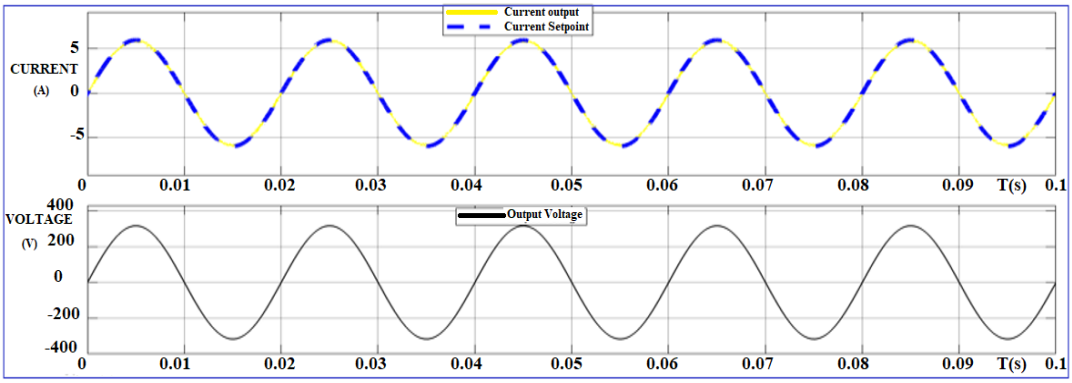
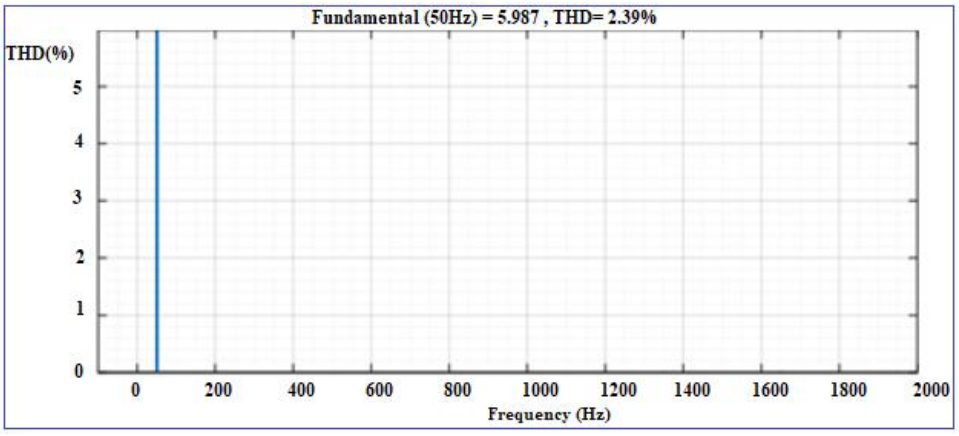


Figure 4. H4 topology



(a)



(b)

Figure 5. Set point, (a) output current and output voltage and (b) THD value of the output current at the load

3.2. Simulation and output result of H5 topology

The H5 topology in Figure 6 consists of five active switches (S1 through S5). Switch S5 is inserted between the positive DC bus and topology H4. This is called the DC side isolation topology. The S5 allows shutdown in zero voltage conditions and provides isolation between the grid, and PV array to minimize power loss. Figure 7(a) shows the output signal waveform for this topology. The latter allows the generation of sinusoidal unipolar voltage and reduces output current ripple. The power loss is small, but the THD is not completely eliminated, at 3.35% as shown in Figure 7(b). The S5 switch provides this reduction, which is twice the frequency of other switches.

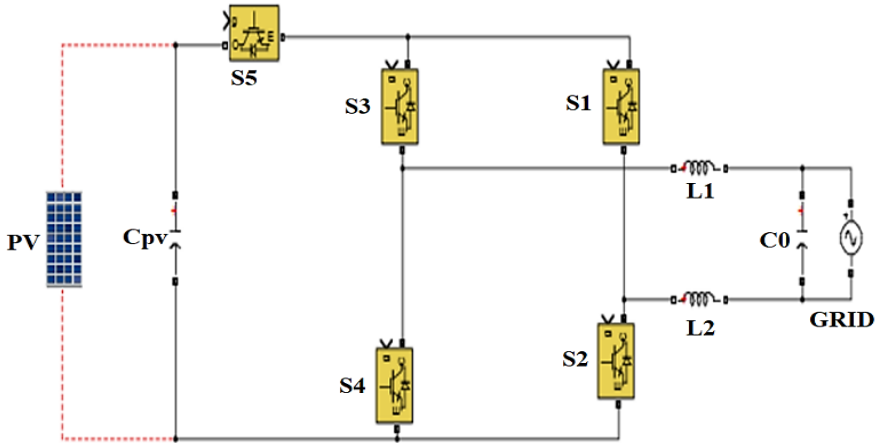
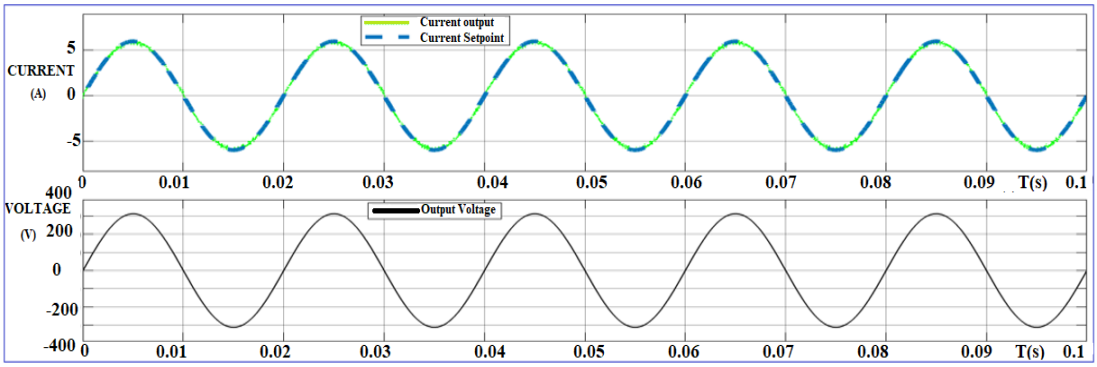
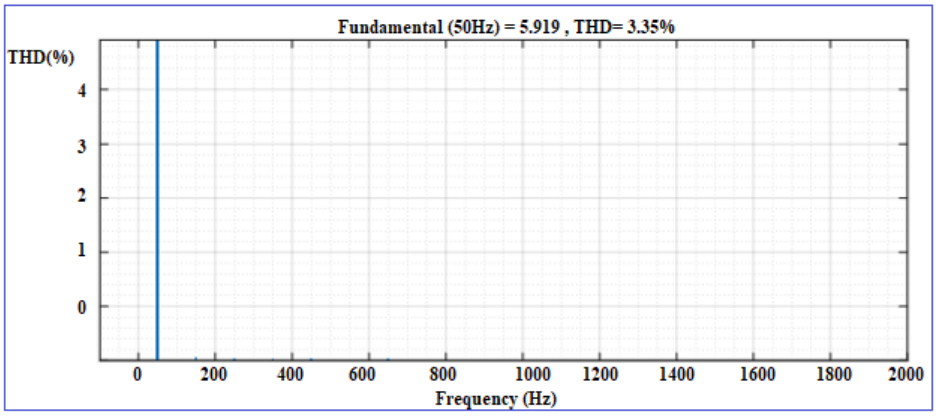


Figure 6. H5 topology



(a)



(b)

Figure 7. H5 topology (a) set point, output current and output voltage and (b) THD value of the output current at the terminals of the load

3.3. Simulation and output result of HERIC topology

HERIC Inverter topology is obtained by linking two interrupts directly to the output of the H4 topology as shown in Figure 8. These two additional switches are activated when the power is off. In this case, all other switches will open before the PV module disconnects from the grid. As shown in Figure 9(a), the addition of two active switches 5 and 6 to the output of the traditional topology H4 provides a very efficient and reliable inverter topology (HERIC). The output voltage is a sine wave, eliminating leakage current in Figure 9(b). Since only two switches are conducting, the conduction loss is low and the THD is reduced by 1.92% compared to the previous topology.

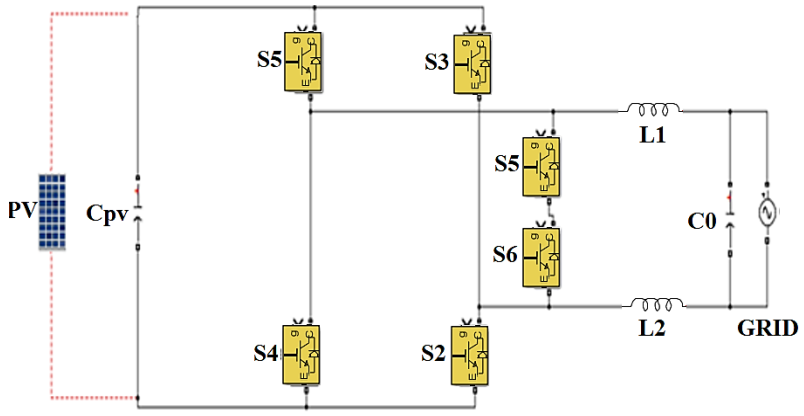
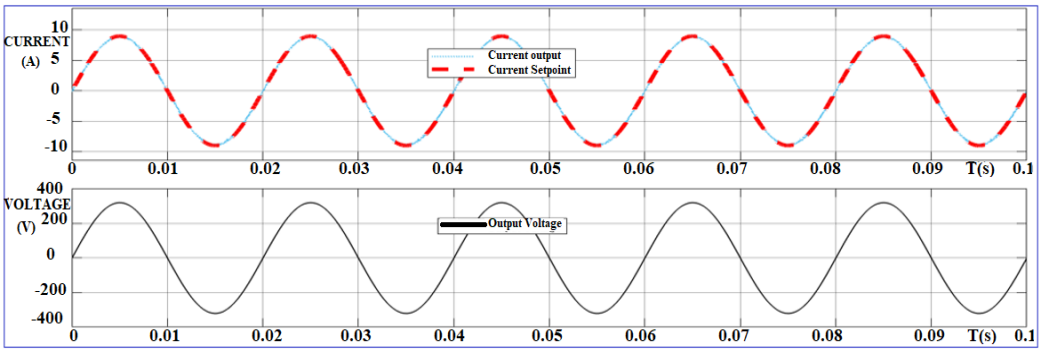
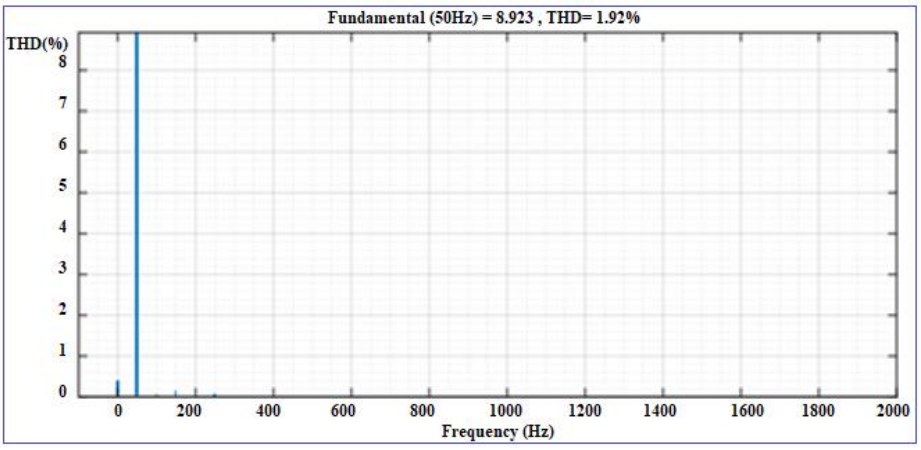


Figure 8. HERIC topology



(a)



(b)

Figure 9. HERIC topology, (a) setpoint, output current and output voltage and (b) THD value of the output current at the terminals of the load

3.4. Simulation and output result of H6 ameliorated topology

The H6 topology was achieved by inserting an active switch into the negative bus of the DC link in the H5 topology, as shown in Figure 10. It consists of six independently controlled active switches (S1 to S6). In the negative half cycle, switch S6 is active, and in HF Switch 3 and 4 are active. Switches 1, 2, and 5 are disabled. Therefore, current leakage and electromagnetic interference are low. Figure 11(a) shows the model of H6 ameliorated inverter. Figure 11(b) shows simulated waveforms of proposed H6 topologies at the unity power factor. These topologies make it possible to reduce the current variation at the output and eliminate the inductance losses after the generation of a unipolar output voltage at three levels. Hence, current leakage is completely eliminated. Despite the results obtained with the existing H6 inverter topology, leakage current is not completely eliminated. To solve this problem by adding a memory branch that allows improvement of this existing topology, the latter allows for the complete elimination of leak currents. In addition, the harmonic distortion of this topology is very low (THD=0.15%) and has excellent reactive power capacity as shown in Figure 11(c).

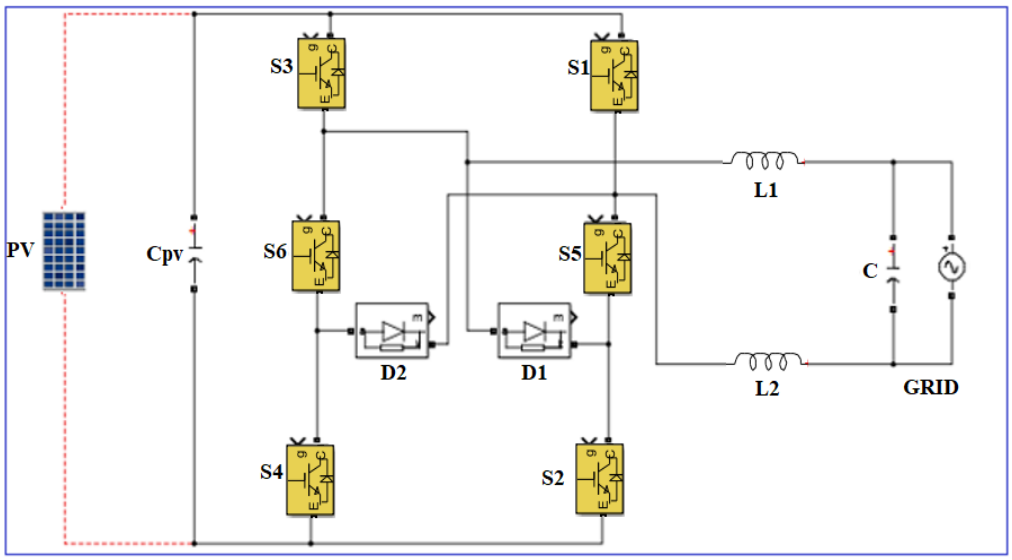


Figure 10. H6 topology

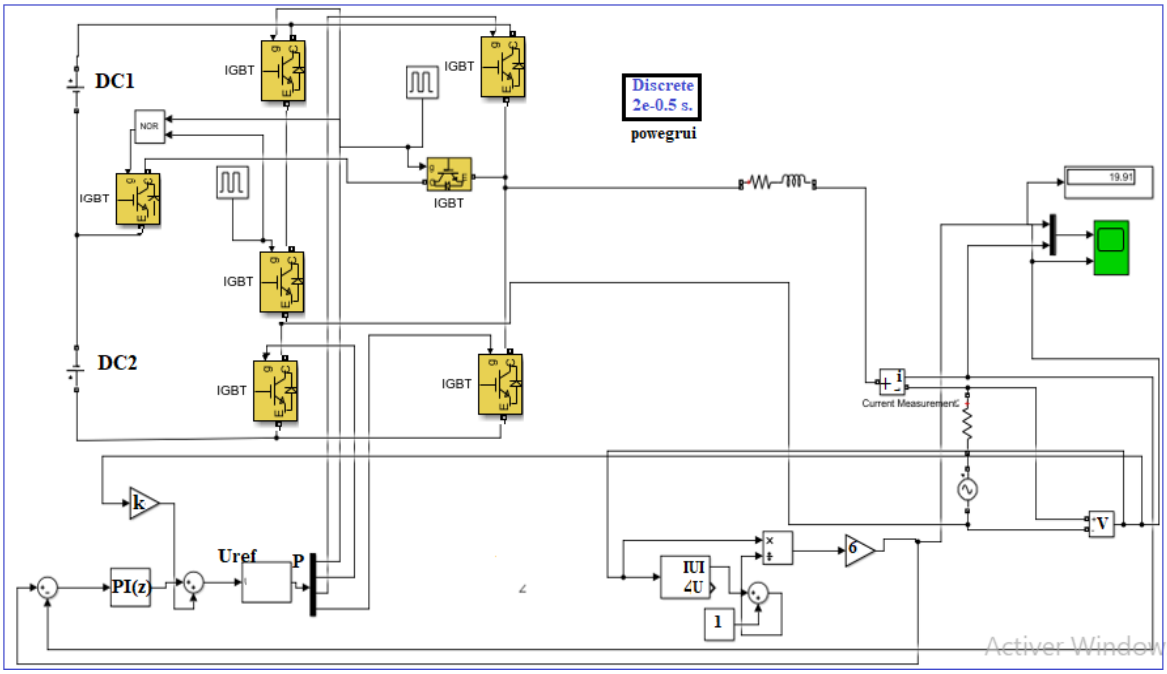
An analysis of the different topologies showed that the H4 and H5 topology has only four and five power devices. With the proposed PWM modulation, it could be seen that the form of the current signal and the grid voltage of these topologies is purely sinusoidal. The analysis of Figures 5, 7, 9, and 11 demonstrated that the inverter voltage output and current output that is in sinusoidal form. On the other hand, the waveform has less distortion; the above values as shown in Table 2 showed that the output obtained is purely sinusoidal. The amplitude of the current is near to a set point, and the waveform is sinusoidal. The results of the PWM technique showed that the ripples in the output are reduced to a great amount in the less inverter transformer. The comparison of the THD of these four technologies is given in Table 2. This THD is calculated based on simulated results.

Spectral analysis showed that the overall THD of the enhanced H6 topology was THDi=0.15% and THDv=0.15% lower than the other different typologies as shown in Table 2. Therefore, the improved H6 topology has the best current consumption characteristics. In this topology, the conduction loss is lower because only two switches are in the positive voltage grid conduction state compared to the H4, H5, HERIC, and H6 families.

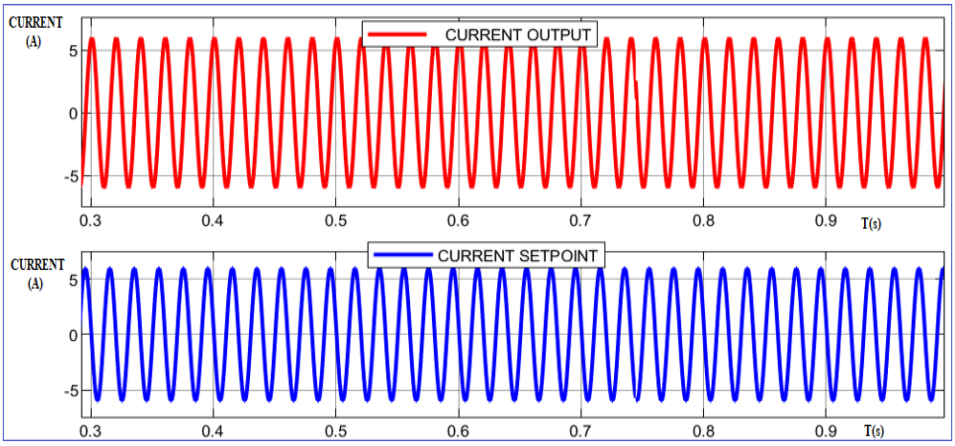
3.5. Simulation and output of the of the cascade inverter at five levels

3.5.1. Open loop control (OL)

Figure 12(a) shows the output current and voltage output signals, the current signals consist of five levels (+8, +4, 0, -4, -8A) and for the output voltage is the superposition of the two input sources. It is cut to the carrier frequency, has five levels +80, +40, 0, -40 and -80 V. After filtering; Figure 12(b); current and voltage, output signals the form of current and voltage becomes quasi-sinusoidal with a THDi=4.74% as shown in Figure 13(a)-(b).



(a)



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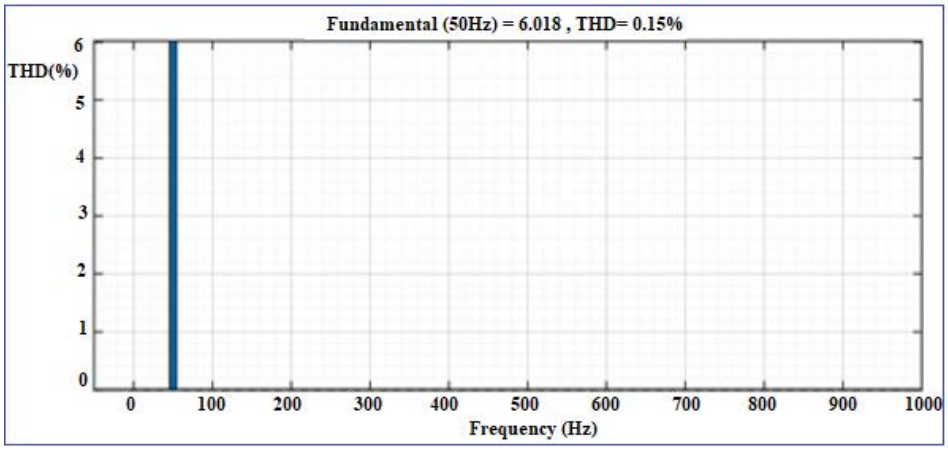
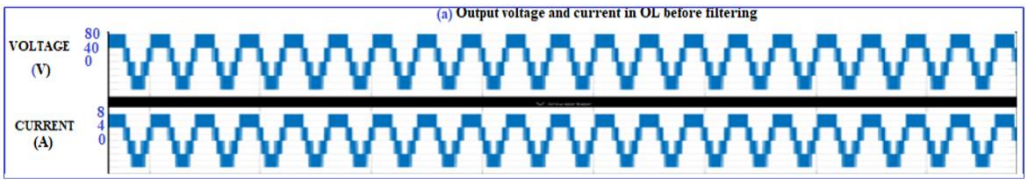


(c)

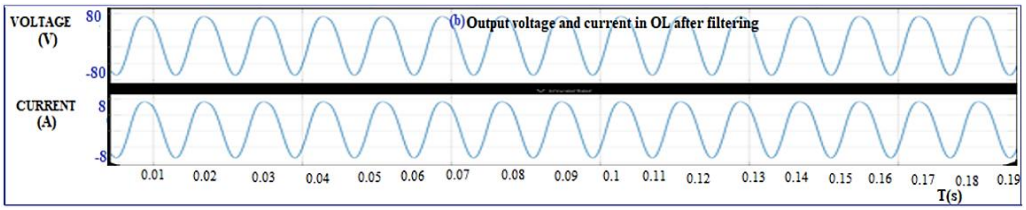
Figure 11. H6 ameliorated topology (a) model of H6 ameliorated inverter, (b) setpoint and output current, and (c) THD value of the current output at the terminals of the load

Table 2. Comparison of total harmonic distortion of these four typologies

Topology	$THD_{Current}$	$THD_{Voltage}$
H4	2.39%	0.16%
H5	3.33%	0.16%
HERIC	1.92%	0.16%
H6 Ameliorate	0.15%	0.15%

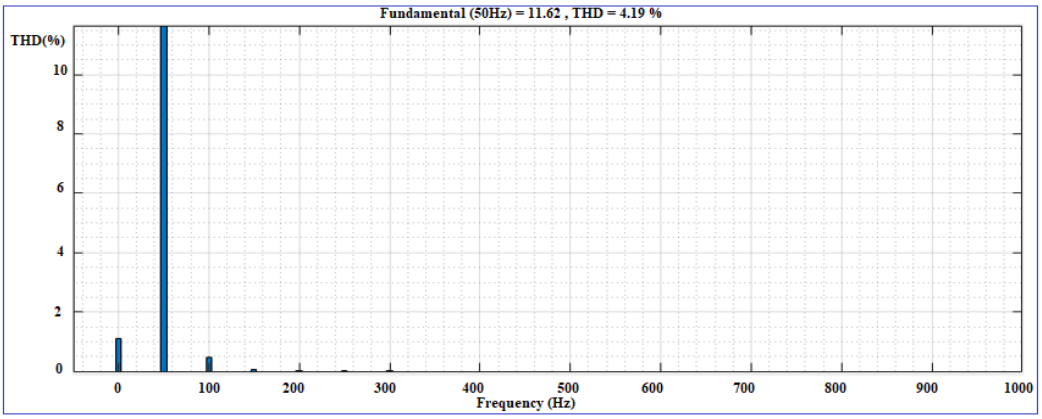


(a)

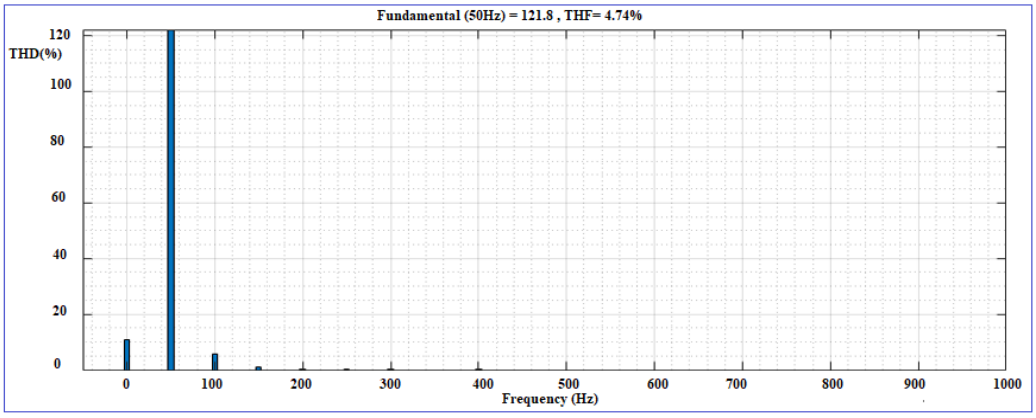


(b)

Figure 12. Output voltage and current in OL (a) before filtering and (b) after filtering



(a)



(b)

Figure 13. THD value of current and voltage at the output of the 5NV cascade inverter in OL after filtering (a) current and (b) voltage

3.5.2. Closed loop control (CL)

Figure 14 shows the simulation diagram of the closed-loop five-level single-phase inverter. In this part, we have controlled the inverter in a closed loop according to the Figures 15(a) and 15(b), (see in appendix). Note that the output signals of the inverter shown in Figure 16 (see in appendix) in the form of current and voltage are perfectly sinusoidal for closed-loop control. Figure 15 shows the frequency spectra of the output voltage and current of the 5NV closed-loop cascade inverter. After having ordered this closed-loop inverter, note that there is an improvement in the current, and voltage spectra at the load terminal, and also the elimination of all the harmonics of frequency close to that of the fundamental (50 Hz), which allows the reduction of harmonic distortion rate with a THDi=0.30% and THDv=0.45%. From the Figure 17 (see in appendix) and after comparison of the output currents of the inverter and at the load terminal, we see that it has a precise monitoring of the current and mains voltage vector by the PLL system, which ensures proper operation of the control system.

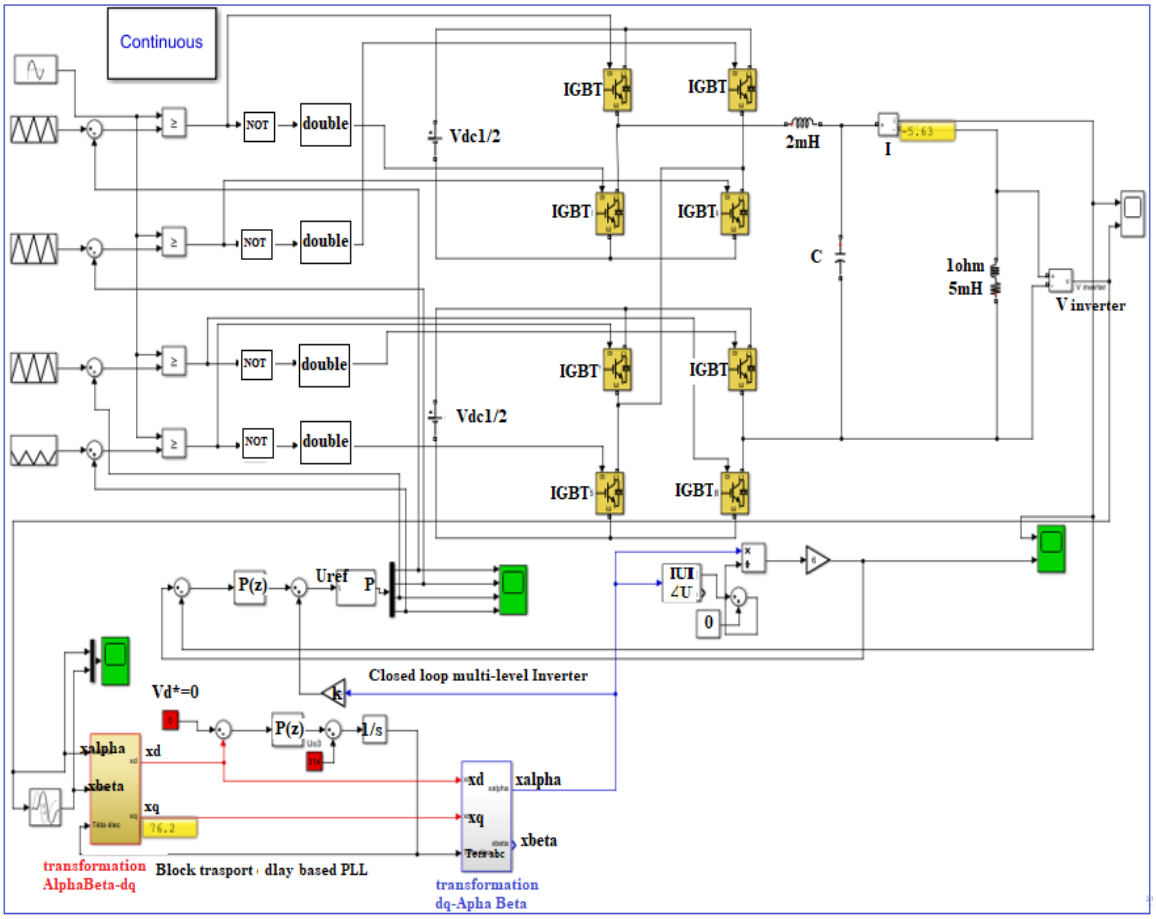


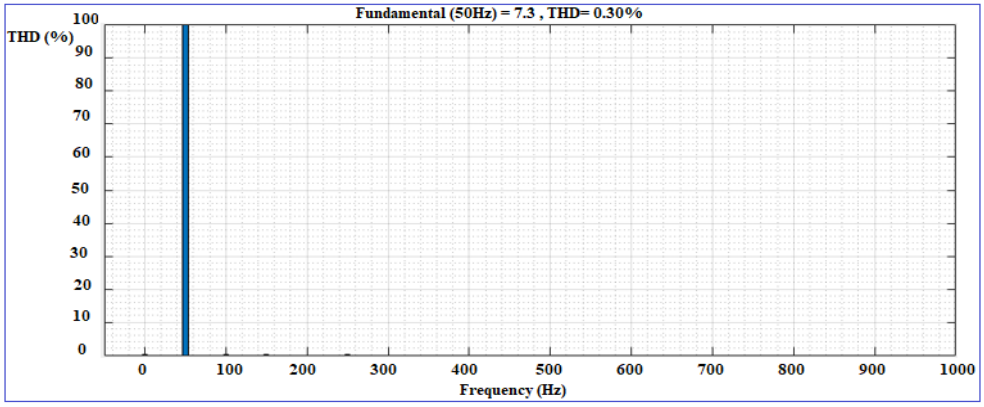
Figure 14. Control diagram of the single-phase inverter five levels

4. CONCLUSION

This article is devoted to the research, improvement, and design of PV inverters at different levels while ensuring optimal operation of PV sources using a PR AC controller. A regulation loop is also introduced to respond to grid connection problems with a low PLL algorithm to ensure better synchronization between the photovoltaic source and the grid. The H5, HERIC, and H6 topologies without transformers provide galvanic isolation but do not eliminate the current leakage. The total THD of the topologies H4, H5, and HERIC is 2.39%, 3.33%, and 1.92% respectively. The H6 topology exhibits the best current leakage characteristic with a THD lower than the other typologies equal to 0.15%, which is within the specified limit. The current leakage is reduced, and meets the safety standard. After having described the cascade inverter topology at five levels, we applied to the latter an advanced PWM control in a closed regulation loop at the end of studying the influence of this control before, and after the application of filtering on the loads

connected to the inverter, the output of the inverter, and the effect of harmonics on the output current, and voltage. After ordering this closed-loop inverter, we noticed an improvement in the voltage and current spectra at the load terminal. Also, the elimination of all the harmonics of frequency close to that of the fundamental (50 Hz) and a reduction of the rate of harmonic distortion from THDi=34 .99% to THDi=0.30% for the current and of THDv=34.99% to THDv=0.45% for the voltage. Thus, although these results demonstrate the superiority of the PR controller for applications requiring sinusoidal references, when using the PR controller, the harmonics 3, 5, and 7 in the current grid indicate that harmonics are eliminated, and conform to standard regulations.

APPENDIX



(a)

(b)

Figure 15. Current and voltage spectrum at the output of the 5NV cascade inverter in CL (a) current and (b) voltage

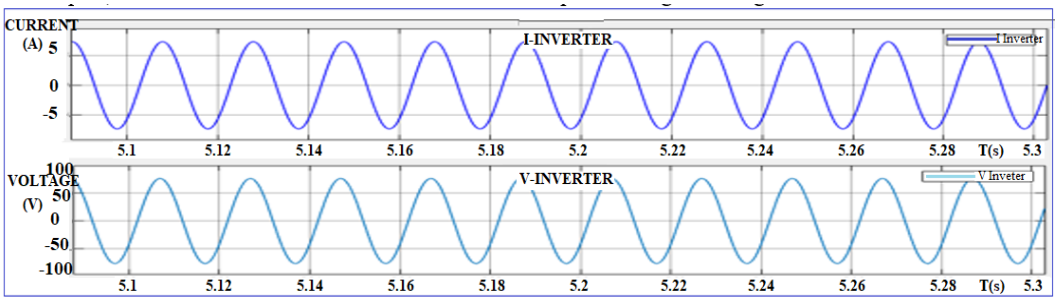


Figure 16. Output voltage and current in CL

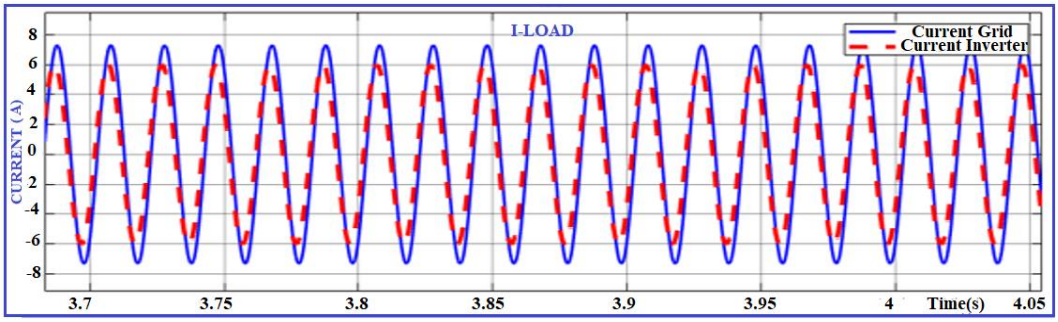


Figure 17. Output current at the grid terminal

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