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Adiabatic technique based low power synchronous counter design

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ABSTRACT

The performance of integrated circuits is evaluated by their design architecture, which ensures high reliability and optimizes energy. The majority of the system-level architectures consist of sequential circuits. Counters are fundamental blocks in numerous very large-scale integration (VLSI) applications. The T-flip-flop is an important block in synchronous counters, and its high-power consumption impacts the overall effectiveness of the system. This paper calculates the power dissipation (PD), power delay product (PDP), and latency of the presented T flip-flop. To create a 2-bit synchronous counter based on the novel T flip-flops, a performance matrix such as PD, latency, and PDP is analyzed. The analysis is carried out at 100 and 10 MHz frequencies with varying temperatures and operating voltages. It is observed that the presented counter design has a lesser power requirement and PDP compared to the existing counter architectures. The proposed T-flip-flop design at the 45 nm technology node shows an improvement of 30%, 76%, and 85% in latency, PD, and PDP respectively to the 180 nm node at 10 MHz frequency. Similarly, the proposed counter at the 45 nm technology node shows 96% and 97% improvement in power dissipation, delay, and PDP respectively compared to the 180 nm at 10 MHz frequency.

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1. INTRODUCTION

Sequential circuits play an important role in many very large-scale integration (VLSI) circuits and computer processors. As a result, designing low-power sequential circuits is an important aspect of VLSI design, especially for high-performance applications. A counter is a device that counts the occurrences of a specific event or activity and, on occasion, displays that information, often in relation to a clock signal. Digital electronics utilize counters for counting purposes; they can keep track of particular circuit events. A novel complementary metal oxide semiconductor (CMOS) logic for low power, which is based on the adiabatic switching principle, is called adiabatic logic. It comes from the word "thermodynamics," which means no energy dissipation [1]. Wang and Lau [2] proposed less power-switched output adiabatic logic. This circuit uses a single N-channel metal oxide semiconductor (NMOS) for precharge rather than two diodes as in previous circuits. Unlike CMOS circuits, the counter is designed using an adiabatic technique, which means that less power is dissipated when switching takes place. In many VLSI applications, such as

timers, frequency dividers, analog-to-digital converters (ADCs) or digital-to-analog converters (DACs), memory, and so on, low-power circuits are used [3]. Soundar *et al.* [4] presented the design of energy-efficient logic circuit using the adiabatic technique. In comparison to CMOS logic, this logic uses a charge recovery mechanism to produce relatively low power consumption. Traditional static CMOS logic can directly drive and be driven by the new technology. The power dissipation of the integrated circuit becomes a very serious issue when the size of the integrated circuit increases and more components are manufactured per unit die area with technological advancement. Counter architecture has a power overhead because of the high power consumption due to the clock signal delivery and the undesired flip-flop activity produced by the clocks [5]. Current and Mow [6] introduced parallel counter design using four-valued threshold logic.

Internet of things (IoT) devices have stringent constraints on power dissipation. Adiabatic logic has been used as a novel computing platform for the development of energy-efficient internet of things devices [7]. Umarani [8] presented a high-performance asynchronous counter based on gate diffusion input (GDI) T-flip-flops with a low area and power consumption. The GDI technique is used here, which enables the construction of many complex logic functions using only two transistors. As a result, the memory device is vital in digital systems, where flip-flops are the basic building blocks of digital circuits with low power and delay. Majeed *et al.* [9] presented a synchronous counter design using a novel level-sensitive T-flip-flop based on quantum-dot cellular automata (QCA) technology. Xin *et al.* [10] explained a complementary pass-transistor adiabatic logic (CPAL) flip-flops with adiabatic two-phase CPAL operating in near-threshold and super-threshold regions. The two-phase CPAL adiabatic technique is used to design the D and T flip-flops. The power dissipation of medium-voltage adiabatic flip-flops is significantly reduced when they run at a reasonable speed. Akhila and Kumar [11] presented a design of sub-threshold adiabatic logic-based Johnson's ring counter using static CMOS and SAL D flip-flop. Katreepalli and Haniotakis [12] presented a power-efficient 6-bit binary up-down counter design using a T flip-flop. Kumar and Kumar [13] presented a low-power 4-bit synchronous counter configuration using efficient charge recovery logic (ECRL) and positive feedback adiabatic logic (PFAL) and 2PASCL adiabatic logic based on D flip–flop. Krishnaveni *et al.* [14] suggested a high-speed conditional data mapping flip-flop (CDMFF) parallel counter based on state look ahead logic.

Low-power design is considered very powerful for any digital circuitry's excellent performance for sequential circuits. Different types of counters are designed for different types of logic. The counter can be used in various logic designs and applications [15]. When compared to a conventional ring counter, a synchronous counter requires half the number of flip-flops. Kumar *et al*. [16] presented a design and analysis of fully static true single-phase-dual edge triggered-flip flop for internet of things applications. In terms of latency, power, figure of merit, and area, the presented flip-flop proved to be more power efficient than typical single and double-edge-triggered flip-flops. The performance characteristics of two types of dual edge triggered flip-flops are compared and the optimal flip is determined. When compared with a typical dual edge-triggered flip-flop in full static mode, clock overlaps problems in dual edge-triggered TSPC flip-flops are decreasing.

Kahleifeh and Thapliyal [17] presented a less-energy and CPA-resistant adiabatic CMOS/MTJ logic for IoT devices. Spin transfer torque magnetic tunnel junctions (STT-MTJs) and adiabatic logic are used to minimize both leakage power and dynamic power. CMOS integrated circuits are also vulnerable to power analysis assaults due to side-channel leakage. Adiabatic logic is used to create secure circuits with consistent power usage, hence preventing power analysis attacks. When compared to CMOS circuits, a hybrid adiabatic-MTJ design was developed, which uses two-phase adiabatic logic to give a low-energy and secure solution.

Kumar and Kumar [18] introduced adiabatic logic and parallel computing designs in the full adder, for ultralow-power applications. The use of adiabatic logic makes these devices energy-efficient for low-power applications, and they work satisfactorily at low voltages. Monteiro and Takahashi [19] presented a low-power two-phase clocking adiabatic PUF circuit. The IoT has made it possible for battery-operated devices to send private information, but it also has high power consumption and security risks. Physical unclonable functions (PUFs) based on adiabatic present a viable approach for safe and low-power IoT device applications to overcome these issues. Padmini [20] presented a leakage resilient adder using dual rail, single clock adiabatic logic against differential power analysis (DPA) attacks. Single clock positive feedback adiabatic logic (SCPFAL) is introduced, which reduces energy dissipation and also produces uniform power and current traces. It is verified by implementing the fundamental gates and a 1-bit and 4-bit dual rail SCPFAL adder with previous methods.

Ramachandran *et al.* [21] presented the proposed design of all-optical shift registers by D flip-flop. All-optical shift registers are designed with interconnected D flip-flops and are operated by conventional clock pulses. PISO, designed as a 2-bit shift register using a D flip-flop, is developed using a Mach-Zehnder interferometer-semiconductor optical amplifier based on all-optical logic gates. Daram *et al.* [22] presented a low-power design of a carry look-ahead adder by using adiabatic logic. The carry look-ahead adder, also known as the fast adder, also plays an important role in reducing circuit delay. Because delay is a significant

factor in low-power VLSI circuits, using an adiabatic technique reduces energy consumption in full adders. When comparing ECRL and PFAL, energy consumption is reduced in both, but slightly more in PFAL. Koyasu and Takahashi [23] presented a performance and security evaluation of the S-box using current-pass optimized symmetric pass gate adiabatic logic. Comparing the current-pass optimized symmetric pass gate adiabatic logic (CPO-SPGAL) to traditional adiabatic logic, the CPO-SPGAL achieves a flat current waveform. This paper presents the design of direct-current diode-based positive feedback adiabatic logic (DC-DB PFAL) based T flip-flop which is proposed first time and then the designing of the synchronous counter is carried out. The performance matrix such as power dissipation (PD), latency, and power delay product (PDP) is analyzed for the proposed circuits. It gives improved results for PD and PDP.

The rest of the article is organized as follows. Section 2 presents the basics of adiabatic logic. Section 3 presents the proposed T flip-flop based on the DC-DB PFAL adiabatic design technique. Section 4 discusses the design of a 2-bit synchronous counter using the proposed T flip-flop. Section 5 is devoted to result in analysis and discussion. Finally, section 6 concludes the paper.

2. ADIABATIC LOGIC

The thermodynamics process that does not exchange heat with the environment is "adiabatic." It also allows for energy reuse, which reduces the overall amount of energy drawn from the source. The adiabatic logic technique outperforms compares to the other circuit design techniques in terms of reducing energy consumption in a variety of activities [24]. In adiabatic circuits, there are three basic rules for energy utilization. The transistor should not be turned on if there is a potential difference between the drain and the source. Never turn off a transistor if current flows between the source and drain. Current should never be passed through a diode. A trapezoidal power clock signal is used to recover the signal energy instead of a static operational voltage. To charge the load capacitance in adiabatic logic, a constant current supply is used instead of a constant voltage supply. The power clock supply is used to create an energy-effective way.

3. DESIGN METHOD AND IMPLEMENTATION

In this section, the proposed T flip-flop and 2-bit synchronous counter are designed using the DC-DB PFAL adiabatic approach using the Virtuoso tool at 45 and 180 nm nodes and at different frequencies of 10 and 100 MHz. Proposed designs are analyzed in terms of delay, PD, PDP, and results are compared with the existing adiabatic and conventional approaches. DC-DB PFAL adiabatic approach is the modification of the modify positive feedback adiabatic logic (MPFAL) logic circuit. The proposed design that allows for complete charge recovery, which was previously impossible. A high-impedance path to the power clock is provided by the diode attached at the bottom of the NMOS tree and it acts as an active load. By reducing the rate of discharge of internal nodes of the logic circuit, it can control the discharging path. The positive source of DC voltage is connected between the diode and the ground to further incorporate the benefit of the level shifting technique in the presented logic circuit. The level-shifting approach minimizes the gate-to-source voltage at the output transistors and thus reduces the leakage and gate current, which in turn, reduces the energy consumption.

3.1. Proposed flip–flop

This section addresses the design of the proposed T flip-flop. This is designed using the basic concept of D flip-flop and Ex-OR gate [24] using the direct current diode based positive feedback adiabatic logic (DC-DB PFAL). The schematic of the proposed circuit is shown in Figure 1.

DC-DB PFAL adiabatic logic approach is proved to be one of the best approaches to reduce the energy dissipation in adiabatic logic circuits. If the *T* input is high, the *T* flip-flop changes state ("toggles"). The flip-flop holds the previous value if the *T* input is low. The output (Q_{next}) of the *T* flip-flop is characterized by (1).

$$Q_{next} = T \wedge \mathrm{Q} \tag{1}$$

Simulation results are illustrated in Tables 1 and 2. At 100 MHz frequency, the proposed T flip-flop shows a power dissipation of 0.05 and 8.80 mW, delay of 9.06 and 8.16 ns, and PDP of 0.0004 and 0.07 fJ respectively at 45 and 180 nm technology node. Similarly, the proposed circuits at 10 MHz frequency show a power dissipation of 0.03 and 0.043 mW, delay of 7.28 and 31.09 ns, and power delay product of 0.0002 and 0.0013 fJ, respectively at 45 and 180 nm technology nodes. The simulations are carried out at different voltage nodes. The detailed analysis of the results is discussed in section 4.

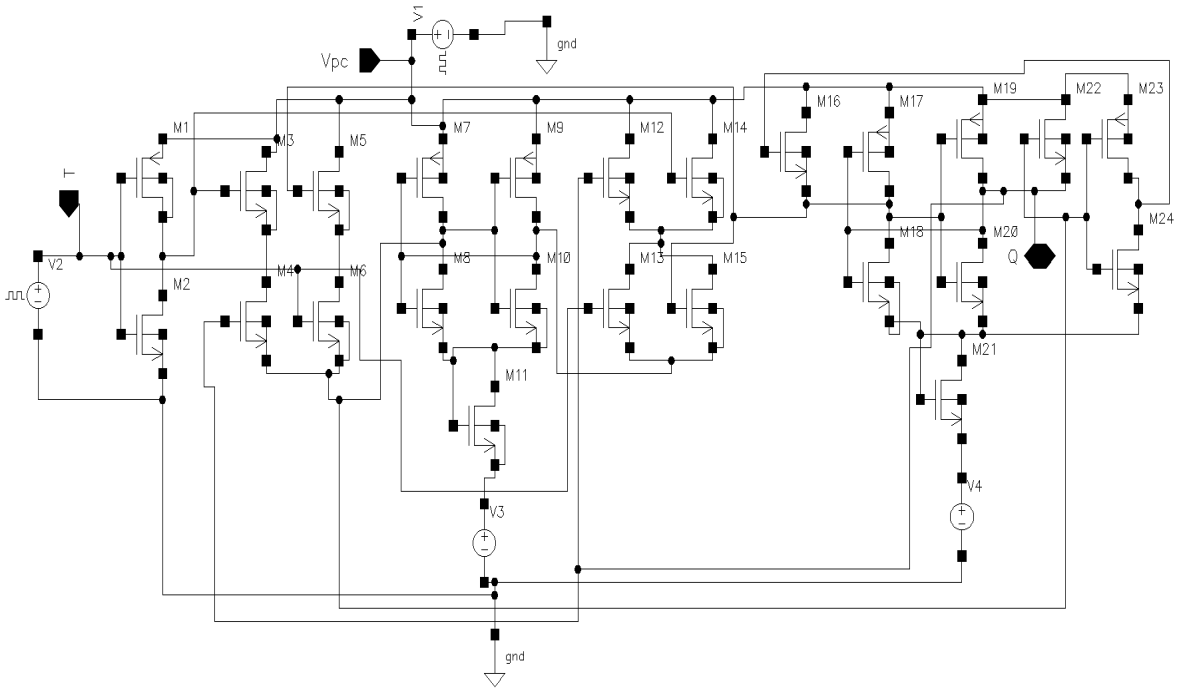

Figure 1. T flip-flop

Table 1. PD, delay, and PDP comparison of T flip-flop based on the DC-DB PFAL adiabatic logic at different voltages and at 10 MHz frequency

Si. No.	Voltage (V)	PD (mW)	Delay (ns)	PDP (fJ)	Tech. (nm)
1	0.7	0.031	7.28	0.0002	45
2	1	138	4.08	0.563	
3	1.2	172	3.74	0.643	
4	1.5	219	3.81	0.834	
5	1.8	263	3.83	1.007	
1	0.7	0.043	31.09	0.0013	180
2	1	10.21	31.24	0.318	
3	1.2	23.81	31.53	0.750	
4	1.5	75.37	31.14	2.347	
5	1.8	289.3	28.66	8.291	

Table 2. PD, delay, and PDP comparison of T flip-flop based on the DC-DB PFAL adiabatic logic at different voltages and at 100 MHz frequency

S. No.	Voltage (V)	PD (mW)	Delay (ns)	PDP (fJ)	Tech.
1	0.7	0.05	9.06	0.0004	45
2	1	210	9.04	1.89	
3	1.2	225	9.02	2.02	
4	1.5	284	9.01	2.55	
5	1.8	341	9.01	3.07	
1	0.7	8.80	8.16	0.07	180
2	1	14.6	8.14	0.118	
3	1.2	104	8.13	0.845	
4	1.5	308	8.13	2.504	
5	1.8	380	8.12	3.085	

3.2. Proposed counter design

Counters are designed using T flip-flops. Counters count the number of clock pulses or inputs, and the amount of bits in the counter is determined by the number of flip-flops utilized in its design. Counter block diagram is shown in Figure 2. Designing a 2-bit counter requires two flip-flops.

This work proposes an energy-efficient design of a 2-bit synchronous counter with fewer hardware overhead, as shown in Figure 3. The presented design shows substantial gain in terms of PD. This basic proposed design can be extended to a wide-bit counter design, giving a more substantial power consumption gain.

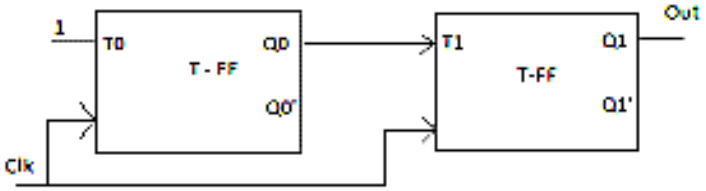

Figure 2. Counter block diagram

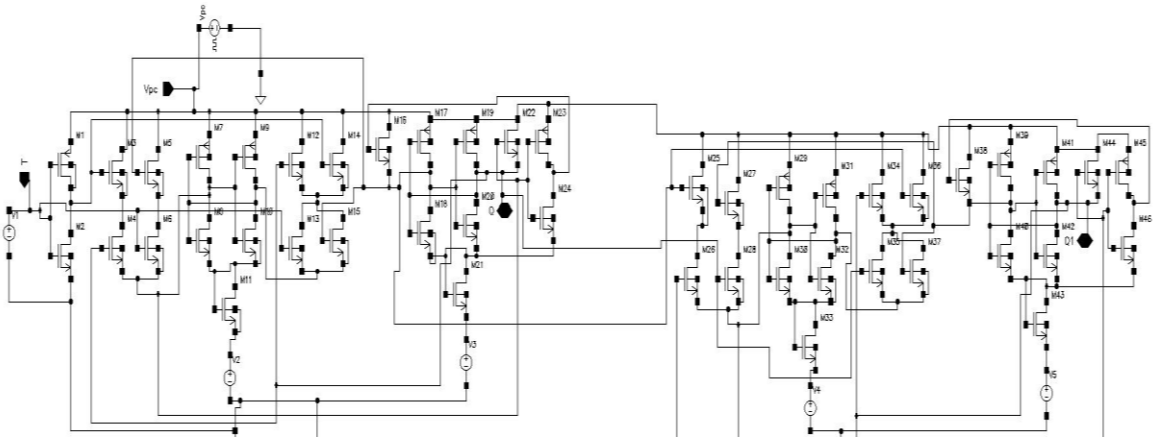

Figure 3. A 2-bit synchronous counter design using T flip–flop

4. RESULT ANALYSIS AND DISCUSSION

The simulation results of the T flip-flop and 2-bit synchronous binary counter design using the DC-DB PFAL adiabatic approach have been discussed in this section. Virtuoso performs these simulations at 180 and 45 nm technology nodes. The comparative analysis of delay, PD, and PDP at different frequencies, voltages, and temperatures of presented circuits is illustrated in Tables 1 to 4. It is observed that the PD of DC-DB PFAL-based proposed T flip-flop and counter is less significant as compared to the different adiabatic approaches available in the literature.

Table 3. PD, delay, and PDP comparison of T flip-flop-based 2-bit synchronous counter design using DC-DB PFAL adiabatic logic at different voltages and at 10 MHz frequency

Si. No.	Voltage (V)	PD (mW)	Delay (ns)	PDP (fJ)	Tech. (nm)
1	0.7	0.034	81.65	0.002	45
2	1	13.67	80.5	1.100	
3	1.2	27.01	81.0	2.187	
4	1.5	228.0	80.7	18.39	
5	1.8	316.3	80.3	25.39	
1	0.7	3.018	35.10	0.105	180
2	1	3.762	33.28	0.125	
3	1.2	7.225	32.58	0.235	
4	1.5	30.44	31.82	0.968	
5	1.8	352.5	28.01	9.873	

Table 4. PD, Delay, and PDP comparison of T flip-flop-based 2-bit synchronous counter design using DC-DB PFAL adiabatic logic at different voltages and at 100 MHz frequency

Si. No.	Voltage (V)	PD (mW)	Delay (ns)	PDP (fJ)	Tech. (nm)
1	0.7	1.791	9.38	0.016	45
2	1	19.32	9.33	0.180	
3	1.2	219	9.07	1.986	
4	1.5	228	8.90	2.029	
5	1.8	361.7	8.51	3.078	
1	0.7	8.92	8.10	0.072	180
2	1	9.18	8.13	0.074	
3	1.2	63.9	8.09	0.516	
4	1.5	308.6	8.07	2.490	
5	1.8	392	8.06	3.159	

4.1. Comparative assessment of proposed circuits for variable voltage

The assessment of the proposed DC-DB PFAL-based T flip-flop is carried out for the estimation of PD, delay, and PDP at variable voltages and at two different technology nodes (45 and 180 nm) for two different frequencies as given in Tables 1 and 2. In the tables, the parameters of the proposed T flip-flop are compared at 45 and 180 nm technology nodes for the assigned operating voltage ranging from 0.7 to 1.8 V. At the 45 nm technology node, the power dissipation of the presented T flip-flop has found an improvement of 30% at 10 MHz and 99% at 100 MHz operating frequency when compared with the values at 180 nm node. Here, all the improved values are estimated at the operating voltage of 0.7 V. Similarly, in Tables 3 and 4 for the proposed counter circuit, the improvement in power dissipation is observed to be 96% at 10 MHz frequency and 79% at 100 MHz frequency. Another vital element of the analysis is the latency of the flip-flop and synchronous counter observed between in (input) and out (output) signals. For the proposed T flip-flop, the improvement in the delay of the circuit is obtained as 76% at 10 MHz and 11% at 100 MHz frequency. Also, for the proposed counter, the propagation delay is better at the 180 nm node which is observed as 56 % and 14% respectively at 10 MHz frequency and 100 MHz frequency. Further, the PDP is calculated for the proposed circuits. The proposed T flip-flop excels by 85% at 10 MHz and 99% at 100 MHz

when compared to PDP. Meanwhile, the proposed counter outperforms with an improvement of 97% at 10 MHz and 77% at 100 MHz frequency. It is evident from the above discussion that the proposed circuits perform well at the 45 nm technology nodes for power dissipation and PDP.

4.2. Comparative assessment of proposed circuits for variable temperature

The analysis is carried out for the proposed circuits by varying the temperature over the range of 25 ºC to 35 ºC. The performance metrics such as PD, delay, and PDP are estimated at two different technology nodes of 45 and 180 nm and for two different operating frequencies of 10 and 100 MHz as shown in Tables 5 to 8. Here, the operating voltage is fixed at 0.7 V and the results are compared for both technology nodes. The improvement in each parameter for the proposed circuits is evaluated at 25 ºC. Tables 5 and 6 present the analysis of the proposed T flip-flop. It is observed in Tables 5 and 6 that the improvement in PD for T flip-flop at 45 nm is 24% at 10 MHz and 97% at 100 MHz frequency. At 10 MHz, the propagation delay has improved values at the 45 nm technology node while at 100 MHz the delay obtained is better at the 180 nm node. While estimating PDP, the values are again improved by 84% at 10 MHz and 96% at 100 MHz at the 45 nm node.

Table 5. PD, delay, and PDP comparison of T flip-flop based on the DC-DB PFAL adiabatic logic at 0.7V voltage, at different temperatures and at 10 MHz frequency

Si. No.	Temperature (°C)	PD (mW)	Delay (ns)	PDP (fJ)	Tech. (nm)
1	25	0.579	7.29	0.004	45
2	27	0.03	7.28	0.0002	
3	30	0.809	7.27	0.005	
4	32	1.384	7.26	0.010	
5	35	2.278	7.24	0.016	
1	25	0.76	33	0.025	180
2	27	0.04	31	0.001	
3	30	1.102	33	0.036	
4	32	1.905	33	0.062	
5	35	3.150	33	0.103	

Table 6. PD, delay, and PDP comparison of T flip-flop based on the DC-DB PFAL adiabatic logic at 0.7V voltage, at different temperatures and at 100 MHz frequency

Si. No.	Temperature (°C)	PD (mW)	Delay (ns)	PDP (fJ)	Tech. (nm)
1	25	0.24	9.06	0.0021	45
2	27	0.05	9.06	0.0004	
3	30	0.50	9.06	0.004	
4	32	0.79	9.06	0.007	
5	35	1.23	9.06	0.011	
1	25	8.42	8.16	0.068	180
2	27	8.80	8.14	0.071	
3	30	9.37	7.98	0.074	
4	32	9.76	7.98	0.077	
5	35	10.3	8.16	0.084	

Table 7. PD, delay, and PDP comparison of T flip-flop-based 2-bit synchronous counter design using DC-DB PFAL adiabatic logic at 0.7 V voltage, at different temperatures and at 10 MHz frequency

Si. No.	Temperature (°C)	PD (mW)	Delay (ns)	PDP (fJ)	Tech. (nm)
1	25	0.34	81.6	0.027	45
2	27	0.034	81.65	0.0027	
3	30	0.48	81.1	0.038	
4	32	0.83	81.54	0.067	
5	35	1.38	81.7	0.112	
1	25	3.38	36.2	0.112	180
2	27	3.01	35.1	0.105	
3	30	2.46	36.0	0.088	
4	32	2.09	35.7	0.074	
5	35	1.52	35.6	0.054	

Table 8. PD, delay, and PDP comparison of T flip-flop-based 2-bit synchronous counter design using DC-DB PFAL adiabatic logic at 0.7 V voltage, at different temperatures and at 100 MHz frequency

Si. No.	Temperature (°C)	PD (mW)	Delay (ns)	PDP (fJ)	Tech. (nm)
1	25	1.41	9.45	0.013	45
2	27	1.79	9.38	0.016	
3	30	2.37	9.45	0.022	
4	32	2.76	9.45	0.026	
5	35	3.38	9.45	0.031	
1	25	8.81	8.13	0.071	180
2	27	9.18	8.13	0.074	
3	30	9.76	8.13	0.079	
4	32	10.1	8.13	0.082	
5	35	10.7	8.13	0.086	

On the other hand, the performance metrics such as PD, PDP, and latency for the proposed counter are obtained in Tables 7 and 8. The performance of the proposed counter is superior at the 45 nm technology node than at the 180 nm node at both frequencies. The PD is improved by 89% at 10 MHz and 84% at 100 MHz frequency and the PDP is improved by 76% at 10 MHz and 82% at 100 MHz frequency. On the contrary, the delay is found better at 180 nm than at the 45 nm nodes. However, there is always a tradeoff between power and delay which can be seen from the above discussion. Ultimately, the PDP values suggest that the proposed circuits perform better at 45 nm nodes than at 180 nm nodes. Finally, the comparative analysis of delay, PD, and PDP at various frequencies and temperatures and at two different technology nodes is carried out. A comparative analysis of the proposed counter design with the reported

literature is carried out and it is found that the presented 2-bit synchronous counter design is superior in terms of PD to the reported counter [15], as illustrated in Table 9.

Table 9. Analysis of different types of the counters available in the literature and the proposed circuits

Types of counters	Frequency (MHz)	Transistor Count	PD (mW)	Delay (ns)	PDP (fJ)	Ref.	Technology (nm)
Proposed GDI counter	-	48	0.1193	-	-	[8]	130
DFAL Johnson counter	100	-	9	35.82	0.322	[25]	-
CMOS Johnson counter	100	-	56.1	8.82	0.4952	[25]	-
TG Johnson counter	100	-	0. 22	334.75	0.0736	[25]	-
CPL Johnson counter	100	-	2096	6.44	13.49	[25]	-
2PSAL Johnson counter	100	-	5330	4.961	26.48	[25]	`-
SAR ADC based on the proposed up-down counter	-	-	5570	4.281	23.85	[12]	45
CMOS 4-bit Synchronous counter	180	-	0.757	-	-	[13]	-
ECRL 4-bit Synchronous counter	84	-	0.146	-	-	[13]	-
PFAL 4-bit Synchronous counter	132	-	0.173	-	-	[13]	-
2PASCAL°4-bit Synchronous counter	132	-	0.233	-	-	[13]	-
Using D flip-flop 2-bit parallel counter	-	-	1.023	-	-	[14]	-
Using CDMFF2-bit parallel counter	-	-	0.136	-	-	[15]	-
Proposed counter	10 MHz	48	0.034	81.65	0.002		45

5. CONCLUSION

This paper implements the proposed high-performance 2-bit synchronous counter using energy and area-efficient proposed T flip-flop. The offered counter structure has fewer numbers of transistors since the efficient DC-DB PFAL T flip-flop has only 24 transistors. The circuit is designed using both 180 and 45 nm technology nodes, and the simulation results are obtained using the virtuoso tool. The performance comparison has been made for the existing and the presented counters in terms of transistor count, latency, PDP, and PD. The proposed counter circuit design using DC-DB PFAL has shown superior performance. Future research activities may include integrating the presented DC-DB PFAL 2-bit synchronous counter in complex digital systems.

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