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Design and analysis of asymmetrical low-k source side spacer halo doped nanowire metal oxide semiconductor field effect transistor

Padakanti Kiran Kumar, Bukya Balaji, Karumuri Srinivasa Rao
Department of Electronics and Communication Engineering, Koneru Lakshmaiah Educational Foundation (Deemed to be University), Vaddeswaram, India

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ABSTRACT

In this paper, we propose a low-k source side asymmetrical spacer halo-doped nanowire metal oxide semiconductor field effect transistor (MOSFET) design and analysis. High-k spacer materials are now being researched extensively for improving electrostatic control and suppressing short-channel effects in nanoscaled electronics. However, the high-k spacers' excessive increase in fringe capacitance degrades the dynamic circuit performance. Surprisingly, this approach achieves a significant reduction in gate capacitance by maximizing the use of high-k spacer material. Three different structures, symmetrical dual-k spacer, low-k drain side asymmetrical spacer, low-k source side asymmetrical spacer halo doped nanowire MOSFET architectures are simulated and among them low-k source side asymmetrical spacer halo doped nanowire MOSFET architecture giving lower gate capacitance. After doing 3D simulations in Silvaco technology computer-aided design (TCAD) we observed that the gate capacitance and intrinsic delay are 1.23×10^{-17} farads and 1.11×10^{-12} seconds respectively for low-k source side asymmetrical spacer architecture and these are less as compared to high-k spacer architecture. So, the proposed structure is highly recommended for digital applications.

Corresponding Author:

Padakanti Kiran Kumar
Department of Electronics and Communication Engineering, Koneru Lakshmaiah Educational Foundation (Deemed to be University)
Andhra Pradesh, 522502, India
Email: kiranpadakanti0430@gmail.com

1. INTRODUCTION

To improve the enhancing usage of battery-operated devices, the system-on-chip heterogenous parameters are of paramount importance [1], [2]. These parameters include efficiency in area, cost, and power. Many medical instruments, present-day intelligent systems, and cellular phones are a few typical examples. Basic analog/digital circuits like current mirror circuits, combinational logic circuits, operational amplifiers, and static random access memory cells are a few building blocks of system-on-chip designs [3], [4].

The subthreshold region of operation converges with the high gain of operation to characterize the above-stated analog/digital circuits. The increased gate control over the channel and immunity to short channel effects are of supreme importance to scaling the device in nanometer regions without disturbing the performance of the device [5]. However, multi-gate technology has shown ways of improving these characteristics [6]–[9]. The construction of MOSFETs by using nanowires with a gate-all-around configuration promises scalability to any length due to increased immunity to short-channel effects [10]–[14] as compared to others. These also have maximum controllability on the channel, ballistic currents in the ON-state, lower leakage currents, subthreshold-

slope near the ideal value, and at the same time compatible with CMOS technology [15], [16]. The degradation in performance of the device is alleviated using modified multi-gate technology that includes symmetric underlap MOSFETs at source and drain terminals [17], [18]. This type of arrangement lowers the amount of drain-induced barrier-lowering (DIBL). Exceptional RF and analog parameters are achieved by these devices. However, this includes channel resistance distribution along the device by introducing underlap regions. This results in a decrease in the ON current of the corresponding devices [17].

The other important performance parameter in the case of devices is the leakage current. To minimize the leakage current, it is better to use gate-drain/source underlap regions in the channel. This region in the channel increases the series resistance of the channel which consequently decreases the OFF-state current as well as the ON-state current [18]. In order to reduce this series resistance, the spacer material is placed on top of underlap, and it forms coupling fields between gate-drain/source through spacers [18]–[20]. This phenomenon decreases the effective length of the channel.

A superior substitute to this type of arrangement is to have only underlap region in the drain side termed asymmetric underlap MOSFET. In this case, the ON-state current is upgraded by using different spacers of different high-k materials, Nonetheless, these high-k spacers contribute to increment an increment in parasitic fringing capacitance [21]. However, spacer engineering such as asymmetrical spacers, and symmetrical dual-k spacers remarkably enhance the performance of the device [21]–[24]. Therefore, a study of using symmetric dual-k spacers, low-k drain side asymmetric spacer, and low-k source side asymmetric spacer are studied in this paper. This type of study decreases the fringing capacitance without humiliating the required ON-state current and intrinsic delay [22]. The physical insights into fringing and horizontal channel modulation by symmetrical and asymmetrical spacers and their influence on different parameters are presented.

The main aim of this paper is to understand the influence of dielectric constant values on symmetrical and asymmetrical spacers to achieve improved device performance [23]. To characterize all these requirements, firstly a symmetric dual-k spacer halo-doped nanowire MOSFET is simulated, and its performance parameters are characterized. A similar analysis is performed for the low-k drain side asymmetric spacer and low-k source side asymmetric spacer. The paper is organized into four parts for further comparative study. Section 2 presents the proposed device structure and models used in the simulation. The performance of the proposed device and comparison with different architectures is shown in section 3. Finally, the conclusion is shown in section 4.

2. DEVICE STRUCTURE AND SIMULATION PARAMETERS

The two-dimensional cross-sectional graphical representation of various spacer-engineered halo-doped nanowire MOSFET architectures are depicted in Figures 1 to 3. These device structures are specified by a considerable gate length of 10 nm. The nanowire has a diameter (dnm) of 10 nm. The thickness of the oxide is taken as 1 nm. In the above-said architectures, a lightly doped channel is employed with 1×10^{16} cm^{-3} doping concentration and an increased doping concentration of 5×10^{19} cm^{-3} is employed in the channel to introduce halo doping at the end of the source side with implantation method in the fabrication process for adopting channel engineering [25]–[27]. A fixed halo length of 1.5 nm is used in the overall channel length of 10 nm. The nanowire has a diameter (dnm) of 10 nm. The thickness of the oxide is taken as 1 nm. The underlap and extension regions are introduced in between channel-source/drain with a length of 15 nm, 5 nm and with a doping concentration of 5×10^{17} cm^{-3}, and 1×10^{20} cm^{-3} respectively to increase the tunneling width and it leads to a decrement OFF-State current. Uniform doping of 1×10^{20} cm^{-3} is used at the source and drain doping. The spacer material is placed on top of underlap region with a length of 15 nm and SiO_2, Si_3N_4, Al_2O_3, $HfSiO_4$, and HfO_2 are used as spacer materials. A metalwork function of 4.53 eV is used in the structure.

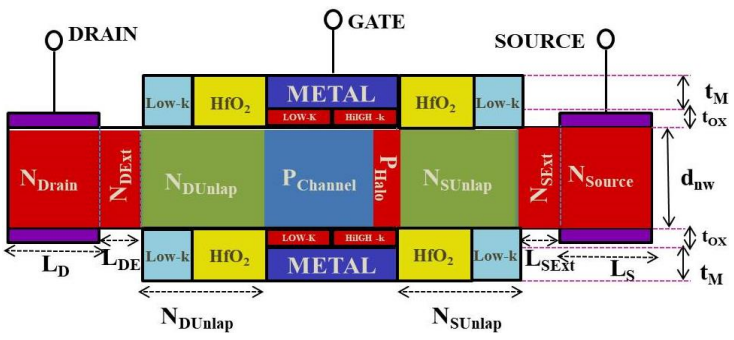

Figure 1. Two-dimensional cross-sectional graphical view of symmetrical dual-k spacer halo doped nanowire MOSFET

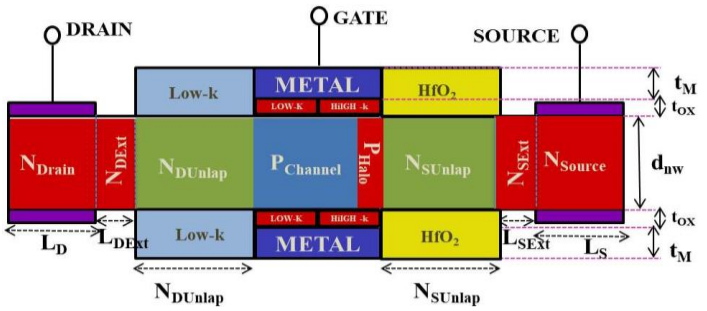

Figure 2. Two-dimensional cross-sectional graphical view of low-k drain side asymmetric spacer halo doped nanowire MOSFET

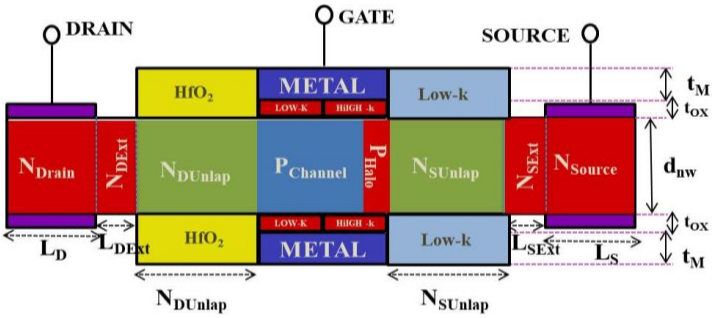

Figure 3. Two-dimensional cross-sectional graphical view of low-k source side asymmetric spacer halo doped nanowire MOSFET

Table 1 lists the numerous geometrical characteristics and their dimensions that are needed for device simulation. All simulation parameters are taken constantly for all the architectures. The proposed device is analyzed with a 3D simulation tool Atlas Silvaco technology computer-aided design (TCAD) for striving design. To have the optimum structure of the device, enhanced meshing is used to design the device. The Two-dimensional graphical representation of the proposed low-k source side asymmetrical spacer halo doped nanowire MOSFET (low-kS asym HNWFET) is depicted in Figure 3. The symmetrical dual-k spacer halo doped nanowire MOSFET (sym dual-k HNWFET) and low-k drain side asymmetrical spacer halo doped nanowire MOSFET (low-kD asym HNWFET) are shown in Figures 1 and 2. All the symmetrical and asymmetrical spacer architectures are simulated and analyzed to obtain minimum fringing capacitance without deteriorating the speed of operation of the device. The proposed device performance is compared with other spacer-engineered structures shown in Figures 1 and 2 to show the improvement. In the source/drain region, underlap-source/drain region, and extension-source/drain region uniform doping concentration is employed.

Table 1. Parameters used for device simulation

Parameter	Low-kS asym spacer halo doped NWFET values
Nanowire diameter	10 nm
Source doping	1×10^{20} cm^{-3}
Drain doping	1×10^{20} cm^{-3}
Doping of source extension	1×10^{20} cm^{-3}
Doping of drain extension	1×10^{20} cm^{-3}
Underlap doping	5×10^{17} cm^{-3}
Channel doping	1×10^{16} cm^{-3}
Halo doping	5×10^{19} cm^{-3}
Thickness of oxide	1 nm
Metal gate thickness	6 nm
Metal gate work function	4.53 eV
Length of gate	10 nm
Source/drain extension length	5 nm
Source/drain underlap length	15 nm
Length of spacer	15 nm
Halo length	1.5 nm
Source length	15 nm
Drain length	15 nm
Supply voltage	1 V

3. SIMULATION RESULTS AND DISCUSSION

The entire device simulations are carried out in the software Silvaco Atlas TCAD. To have improved numerical results, various models are used in the design process. To have proper dopants concentration accountancy, a perpendicular electric-field, parallel-electric field dependent mobility model i.e., Lombardi mobility model is used [18]. This model is the most suitable model for non-planar devices. Further, to deal with the majority and minority carrier recombination, Shockley-Read-Hall and Auger recombination models are invoked. To understand carrier statistics, Fermi-Dirac statistics are used in the simulation. For higher doped source/drain extensions, a band gap narrowing model is used. To account for the lateral band-to-band tunneling nonlocal BTBT model is invoked. The impact of carrier mobility on temperature, the concentration of dopants, and impurity scattering is used. A constant voltage of 1.0 V is used as V_{DD} to carry out all device simulations, but for RF analysis, the bias voltage at the drain to source is assumed to be half of the supply voltage i.e., $V_{DS}=V_{DD}/2$ and gate voltage is swept from 0 to V_{DD}. All the computations are carried out at an ambient temperature of 300 K.

In this paper, various structures such as sym dual-k HNWFET, low-kD asym HNWFET, and low-kS asym HNWFET are simulated for different low-k materials (SiO_2, Si_3N_4, Al_2O_3, and $HfSiO_4$). The performance parameters of each structure are compared for different low-k materials, and we obtain the most suitable low-k material for each structure. Further, the performance parameters of different structures for the most suitable low-k material are compared to obtain the best structure among them. In this process, our main motto is to reduce the fringing capacitance without degrading the intrinsic delay.

3.1. Symmetrical dual-k spacer

In the sym dual-k HNWFET, two different spacer materials i.e., HfO_2 and low-k are placed on each side of the channel. The HfO_2 spacer is placed near the channel and the low-k spacer is placed far from the channel. The optimization of this structure is done in two stages. In the first stage, we will find the best condition for the length of HfO_2 and the length of low-k then we will find the most suitable material for low-k.

3.1.1. Spacer material length variation

In the sym dual-k HNWFET, the length ratio of HfO2 and low-k varies from 1:14 to 14:1 over the total spacer length of 15nm. The spacer length of HfO_2 and low-k plays a significant role in describing the electrostatics of a gate-S/D underlap in the device. For underlap architecture, high-permittivity (k) spacer material modulates the charge transport dynamics inside the channel and the underlap region. This section demonstrates the brief electrostatics, merits, and current characteristics associated with the HfO_2 spacer length variation from 14nm to 1nm. As the HfO_2 length varies from 14 nm to 1 nm, the area of the HfO_2 spacer is decreasing. As HfO_2 has a higher dielectric constant compared to low-k spacer material, it results in a decrement in the area of a stronger fringing field region. The decrement of a stronger fringing field area results in a decrement in the gate capacitance.

Apart from that the decrement in HfO_2 spacer length increases the conduction band energy level and decreases the electric field at the drain side. As a consequence of these the ON-state Current is decreased with the reduction of HfO_2 spacer length. We can observe the impact of HfO_2 spacer length variation on conduction band energy levels and electric field in Figures 4 and 5.

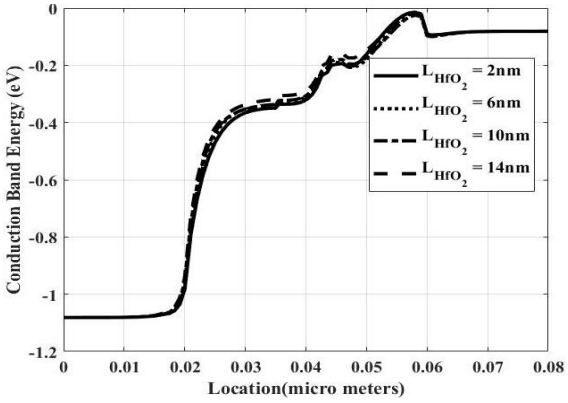

Figure 4. Conduction-band energy levels diagram of symmetrical dual-k spacer halo doped nanowire MOSFET along the channel for various HfO_2 spacer lengths with low-k as $HfSiO_4$ during ON-state

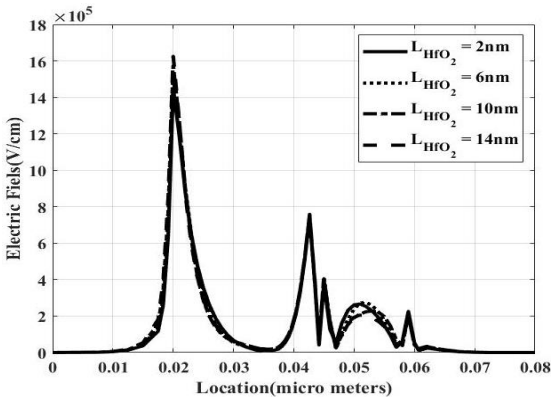

Figure 5. Electric field diagram of symmetrical dual-k spacer halo doped nanowire MOSFET along the channel for HfO_2 spacer length variations with low-k as $HfSiO_4$ during ON-state

In Figure 6, we have plotted the variation of ON-state current and gate capacitance for HfO_2 spacer lengths 2 to 14 nm. From Figure 6, it is observed that the ON-state current is decreased with the decrement of HfO_2 spacer length, but the gate capacitance is decreased up to 10nm then increased up to 6nm, and again it is decreased. So, in the sym dual-k HNWFET, we have less gate capacitance with a large ON-state current at the HfO_2 spacer length of 10 nm and a low-k spacer length of 5 nm. So, we can choose these as optimum dimensions for HfO_2 length and low-k length.

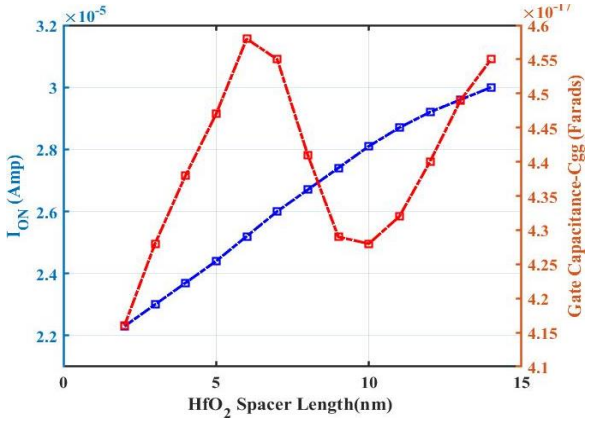

Figure 6. ON-state current and gate capacitance symmetrical dual-k spacer halo doped nanowire MOSFET with low-k as $HfSiO_4$ for HfO_2 spacer length variations

3.1.2. Low-k spacer material variation

The material engineering is performed in sym dual-k HNWFET by varying the spacer materials in the low-k spacer. Different materials with dielectric constants are taken to study the variation of gate capacitance. SiO_2, Si_3N_4, Al_2O_3, and $HfSiO_4$ are used as low-k materials with dielectric constants 3.9, 7.5, 9.3, 12 respectively. Low-k material with the lowest dielectric constant causes weak field coupling between Gate and underlap region. This leads to a reduction in fringing field strength as the dielectric constant of low-k is reduced. Reduction in fringing field strength reduces the gate capacitance. The impact of low-k spacer material variation on gate-to-source capacitance, and gate-to-drain capacitance is shown in Figure 7, and the impact on gate capacitance is shown in Figure 8. From Figure 7, it is observed that the C_{gs} and C_{gd} are decreased by decreasing the dielectric constant of a low-k material. As a result of this, the gate capacitance also decreased by decreasing the dielectric constant of the low-k spacer and it can be observed in Figure 8.

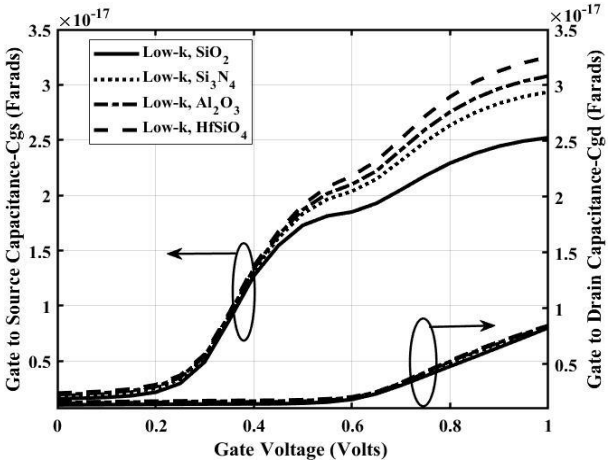

Figure 7. Gate to source and gate to drain capacitance of symmetrical dual-k spacer halo doped nanowire MOSFET by varying gate to source voltage for various low-k materials

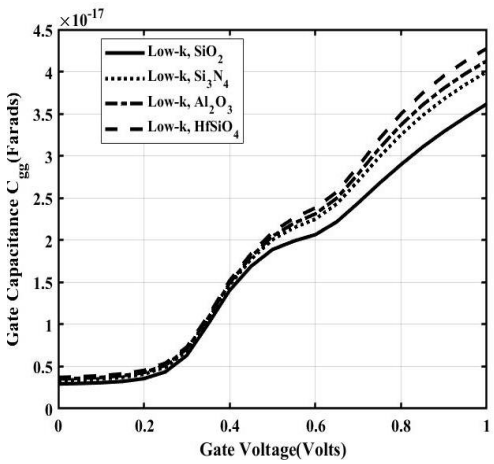

Figure 8. Gate capacitance of symmetrical dual-k spacer halo doped nanowire MOSFET by varying gate to source voltage for various low-k materials

In addition, the decrement of the low-k material dielectric constant increases the conduction band energy levels and decreases the electric field at the drain side. Therefore, the ON-state current has decreased. The impact of low-k spacer material variation on conduction band energy levels and ON/OFF-state current is plotted in Figures 9 and 10, respectively. From Figure 10, it is evident that the ON-state current is decreased by decreasing the dielectric constant of the low-k spacer and not having much impact on the OFF-state current.

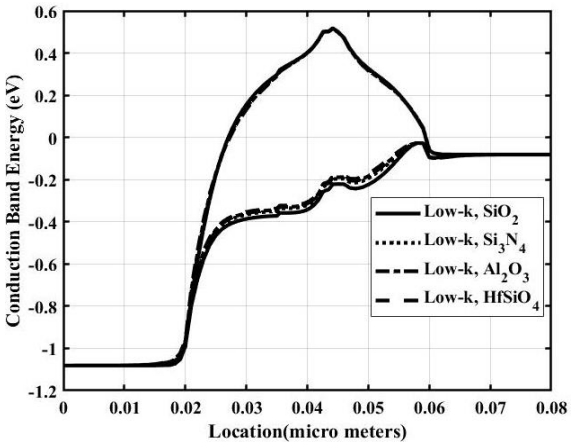

Figure 9. Conduction-band energy levels diagram of symmetrical dual-k spacer halo doped nanowire MOSFET along the channel with L_{HfO2} = 10 nm for various low-k materials during ON/OFF-state

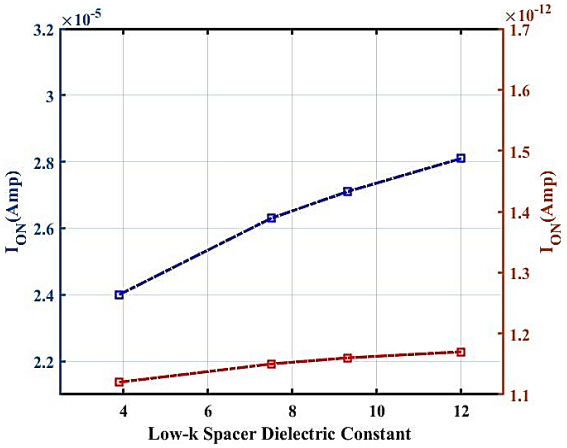

Figure 10. I_{ON} and I_{OFF} of symmetrical dual-k spacer halo doped nanowire MOSFET by varying low-k spacer dielectric constant

The performance parameters variation of sym dual-k HNWFET for various low-k materials is tabulated in Table 2. From the table, it can be understood that low-k material $HfSiO_4$ gives a high ON-state current of 2.81×10^{-5} Amps. The impact of change in low-k material on OFF-state current is negligible. Low-k material SiO_2 gives a lower gate capacitance of 3.62×10^{-17} Farads. Intrinsic delay is almost the same for different low-k materials at 1.52×10^{-12} seconds. Therefore, low-k spacer material SiO_2 is best suitable as low-k material in sym dual-k HNWFET structure because it gives the lowest gate capacitance and intrinsic delay.

Table 2. I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio, C_{gg} and intrinsic delay of sym dual-k spacer HNWFET for low-k material variation

Performance metrics	Low-k spacer			
	SiO_2	Si_3N_4	Al_2O_3	$HfSiO_4$
I_{ON} (Amp)	2.40E-05	2.63E-05	2.71E-05	2.81E-05
I_{OFF} (Amp)	1.12E-12	1.15E-12	1.16E-12	1.17E-12
I_{ON}/I_{OFF}	2.14E+07	2.29E+07	2.34E+07	2.39E+07
C_{gg} (Farad)	3.62E-17	4E-17	4.13E-17	4.28E-17
Intrinsic delay (Sec)	1.51E-12	1.52E-12	1.52E-12	1.52E-12

3.2. Low-k drain side asymmetric spacer

A similar analysis of sym dual-k HNWFET is performed for low-kD asym HNWFET structure. In low-kD asym HNWFET structure, two different spacer materials i.e., HfO_2 spacer material placed at the source side of the channel, and low-k spacer material is placed at the drain side of the channel. SiO_2, Si_3N_4, Al_2O_3, and $HfSiO_4$ are used as low-k materials with dielectric constants 3.9, 7.5, 9.3, and 12, respectively. Figure 11 shows the variation of gate-to-source/drain capacitance and Figure 12 shows the variation of gate capacitance with respect to variation in gate-to-source voltage in the case of low-kD asym HNWFET structures. In low-kD asym HNWFET structure, the use of an HfO_2 spacer source side forms strong field coupling between the gate and underlap at the source side as compared to the drain side. In general, the source side fringing fields have more weightage than overall fringing fields. Due to this, the change in low-k material dielectric constant on the drain side does not have an impact on gate capacitance and it leads to high gate capacitance.

From Figure 11, it can be observed that by varying different materials with different dielectric constants, there is a difference in the observation of the gate-to-source and gate-to-drain capacitance. For SiO_2

material, a high value of gate-to-source capacitance is observed, and a low value of gate-to-drain capacitance is observed. This analysis is different from the conventional symmetrical dual-k spacer nanowire MOSFET. Due to this, the gate capacitance is constant even though the dielectric constant of low-k material at the drain side is varied.

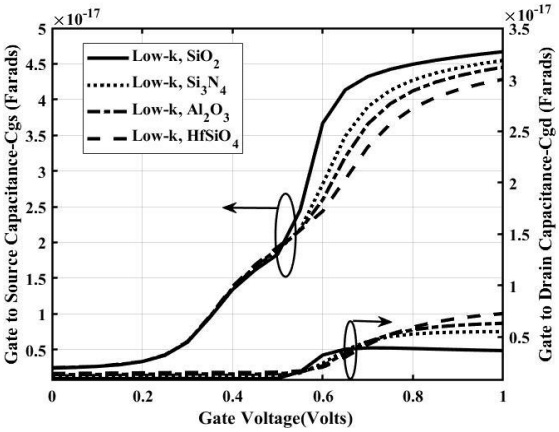

Figure 11. Gate to source and gate to drain capacitance of low-k drain side asymmetric spacer halo doped nanowire MOSFET by varying Gate to source voltage for various low-k materials

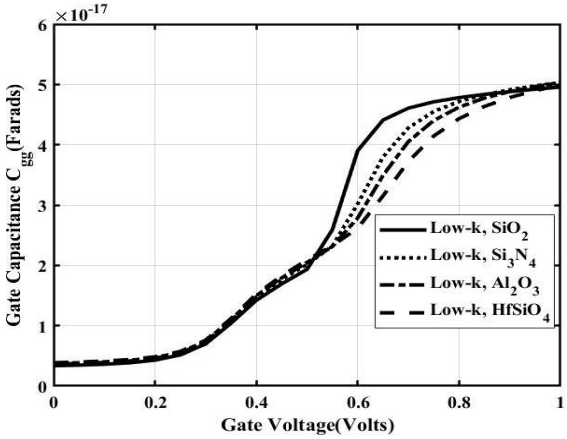

Figure 12. Gate capacitance of low-k drain side asymmetric spacer halo doped nanowire MOSFET by varying gate to source voltage for various low-k materials

Furthermore, lowering the dielectric constant of low-k materials raises conduction band energy levels and lowers the electric field at the drain. As a result, the ON-state current is reduced. A similar analysis can be applied to the conduction band energy variation as shown in Figure 13. The ON current and OFF current variations of low-kD asym HNWFET architecture are shown in Figure 14. As seen in Figure 14, reducing the dielectric constant of the low-k spacer reduces the ON-state current while having no effect on the OFF-state current.

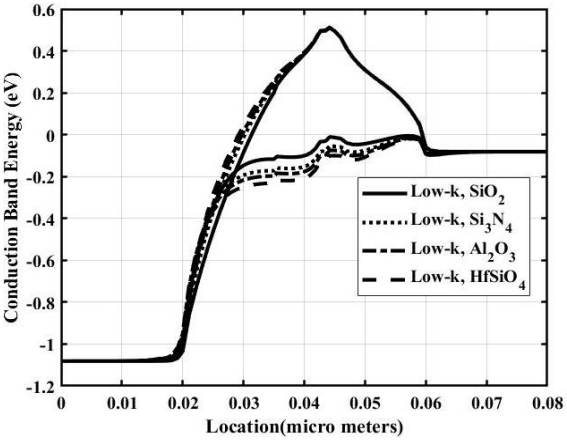

Figure 13. Conduction-band energy levels diagram of low-k drain side asymmetric spacer halo doped nanowire MOSFET along the channel for various low-k materials during ON/OFF-state

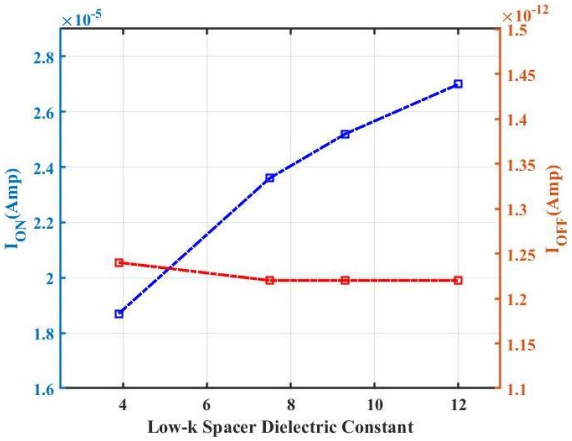

Figure 14. I_{ON} and I_{OFF} of low-k drain side asymmetric spacer halo doped nanowire MOSFET by varying low-k spacer dielectric constant

From Table 3, it is evident that low-k material $HfSiO_4$ gives a high ON-state current of 2.70×10^{-5} Amps. The impact of change in low-k material on OFF-state current is negligible. The impact of change in low-k material on gate capacitance is negligible. The minimum intrinsic delay is given by $HfSiO_4$

low-k material as 1.59×10^{-12} seconds. $HfSiO_4$ is the most suitable as low-k material in low-kD asym HNWFET structure because it gives the lowest intrinsic delay.

Table 3. I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio, C_{gg} and intrinsic delay of low-k drain side asymmetric spacer HNWFET for low-k material variation

Performance metrics	Low-k spacer			
	SiO_2	Si_3N_4	Al_2O_3	$HfSiO_4$
I_{ON} (Amp)	1.87E-05	2.36E-05	2.52E-05	2.70E-05
I_{OFF} (Amp)	1.24E-12	1.22E-12	1.22E-12	1.22E-12
I_{ON}/I_{OFF}	1.51E+07	1.93E+07	2.07E+07	2.22E+07
C_{gg} (Farad)	4.96E-17	5.03E-17	5.03E-17	5.03E-17
Intrinsic delay (Sec)	2.49E-12	1.93E-12	1.77E-12	1.59E-12

3.3. Low-k source side asymmetric spacer

In low-kS asym HNWFET structure, two different spacer materials i.e., low-k spacer placed at the source side of the channel, and HfO_2 spacer is placed at the drain side of the channel. SiO_2, Si_3N_4, Al_2O_3, and $HfSiO_4$ are used as low-k materials with dielectric constants 3.9, 7.5, 9.3, 12 respectively. Using the HfO_2 spacer drain side forms a strong field coupling between Gate and underlap at the drain side. But in overall fringing fields, the contribution of source side fringing fields is more as compared to the drain side fields. Due to this the change in low-k material dielectric constant on the source side shows large variations in the coupling field at the source side. It results in large variations in gate capacitance. The gate-to-source/drain capacitance variation with respect to gate-to-source voltage for low-k spacer material variation is plotted in Figure 15 and the impact on gate capacitance for various low-k materials is shown in Figure 16. The C_{gs} and C_{gd} capacitances are decreasing as the low-k spacer material is changed from HfSio4 to SiO_2. Because of this, the gate capacitance is lowered a lot by keeping the low-k spacer as SiO_2 and it can also be observable in Figure 16.

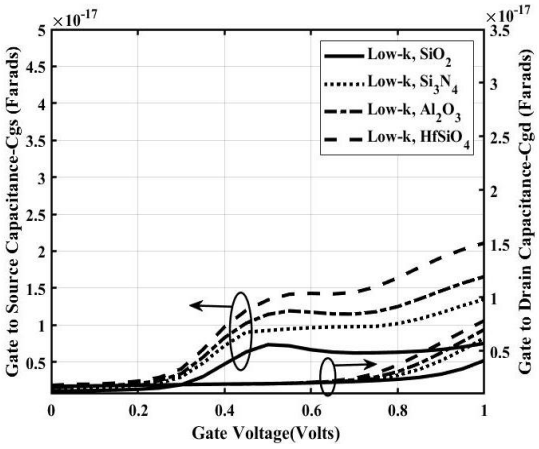

Figure 15. C_{gs} and C_{gd} of low-kS asym HNWFET by varying V_{gs} for various low-k materials

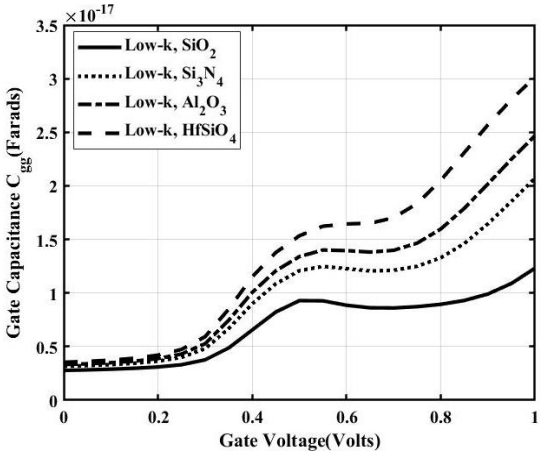

Figure 16. C_{gg} of low-kS asym HNWFET by varying Gate to source voltage for various low-k materials

Figure 17 shows the variation of conduction band energy for different materials with different dielectric constants in low-kS asym HNWFET. Similar to the above conduction, band energy levels are increasing with lowering the dielectric constant of low-k materials. Hence the ON-state current is decreasing by decreasing the dielectric constant of low-k spacer material. The variation of ON-state current and OFF-state current for different low-k spacer dielectric constants is shown in Figure 18. Decreasing the dielectric constant of the low-k spacer lowers the ON-state current while having no influence on the OFF-state current, as seen in Figure 18.

From Table 4, it is evident that low-k material $HfSiO_4$ gives a high ON-state current of 2.14×10^{-5} Amps. low-k material SiO_2 gives lower OFF-state current 6.90×10^{-13} Amps. Low-k material SiO_2 gives a lower gate capacitance of 1.23×10^{-17} Farads. The minimum intrinsic delay is given by SiO_2 low-k material as 1.11×10^{-12} seconds. SiO_2 is the most suitable as low-k material in low-kS asym HNWFET structure because it gives lower intrinsic delay and lower gate capacitance.

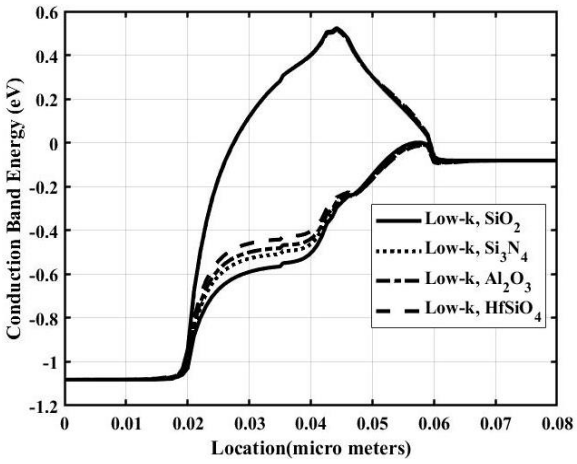

Figure 17. Conduction-band energy levels diagram of low-k source side asymmetric spacer halo doped nanowire MOSFET along the channel for various low-k materials during ON/OFF-state

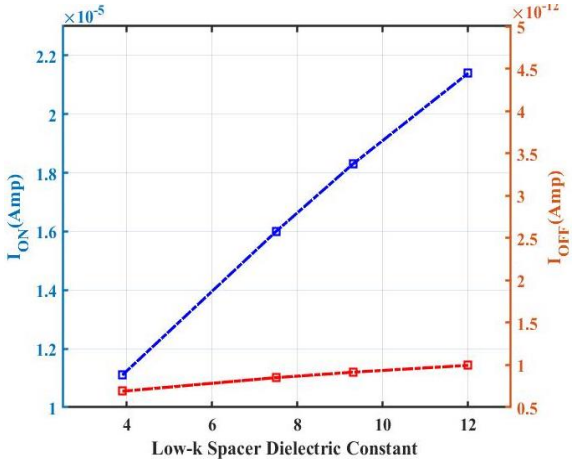

Figure 18. I_{ON} and I_{OFF} of low-k source side asymmetric spacer halo doped nanowire MOSFET by varying low-k spacer dielectric constant

Table 4. I_{ON}, I_{OFF}, I_{ON} / I_{OFF} ratio, C_{gg} and Intrinsic delay of low-k source side asymmetric spacer HNWFET for low-k material variation

Performance metrics	Low-k spacer			
	SiO_2	Si_3N_4	Al_2O_3	$HfSiO_4$
I_{ON} (Amp)	1.11E-05	1.60E-05	1.83E-05	2.14E-05
I_{OFF} (Amp)	6.90E-13	8.51E-13	9.15E-13	9.96E-13
I_{ON}/I_{OFF}	1.61E+07	1.88E+07	2.00E+07	2.15E+07
C_{gg} (Farad)	1.23E-17	2.07E-17	2.47E-17	3.02E-17
Intrinsic delay (Sec)	1.11E-12	1.29E-12	1.35E-12	1.41E-12

3.4. Performance comparison of various spacer engineered structures

The comparison of performance parameters gives the metrics of the proposed architecture with other existing architectures. The comparison of different architectures is done in terms of off-state current, on-state current, subthreshold slope, and drain-induced barrier lowering. The comparison of these parameters gives an insight into the performance of the device.

The performance metrics of different spacer-engineered structures i.e., symmetrical dual-k spacer halo doped nanowire MOSFET, low-k drain side asymmetrical spacer halo doped nanowire MOSFET and asymmetrical spacer halo doped nanowire MOSFET are compared in this section. Initially, each structure performance parameter for different low-k materials is tabulated in Tables 2 to 4 and then analyzed to find the most suitable low-k material for each structure in the earlier sections. From the data in Tables 2 to 4 it is observed that the SiO_2 is best suitable low-k material for sym dual-k HNWFET as well as for low-kS asym HNWFET and $HfSiO_4$ is the best suitable low-k material for low-kD asym HNWFET and summary of these performance parameter values are furnished in Table 5. The performance parameters gate capacitance and intrinsic delay of sym dual-k HNWFET, low-kD asym HNWFET, low-kS asym HNWFET are 3.62E-17, 5.03E-17, 1.23E-17 Farads and 1.51E-12, 1.59E-12, 1.11E-12 seconds respectively. Therefore, the low-kS asym HNWFET structure is observed to have the lowest gate capacitance and lowest intrinsic delay as compared to other structures. As a result, the low-kS asym HNWFET structure is selected as an optimistic structure to achieve the greatest performance improvement. The performance metrics of the proposed device with existing literature are compared in Table 6.

Table 5. I_{ON}, I_{OFF}, I_{ON} / I_{OFF} Ratio, C_{gg}, Intrinsic delay, DIBL and SS of various spacer engineered structures

MOSFET structure	Performance Parameter						
	I_{ON} (Amp)	I_{OFF} (Amp)	I_{ON}/I_{OFF}	C_{gg} (Farads)	Intrinsic delay (Seconds)	DIBL (mV)	SS (mV/Decade)
Sym dual-k HNWFET	2.40E-05	1.12E-12	2.14E+07	3.62E-17	1.51E-12	6.67	60.12
Low-kD asym HNWFET	2.70E-05	1.22E-12	2.22E+07	5.03E-17	1.59E-12	6.71	60.36
Low-kS asym HNWFET	1.11E-05	6.90E-13	1.61E+07	1.23E-17	1.11E-12	7.32	61.97

Table 6. I_{ON}, I_{OFF}, I_{ON} / I_{OFF} ratio, C_{gg}, Intrinsic delay, DIBL and SS comparision with existing literature

MOSFET structure	Performance Parameter						
	I_{ON} (Amp)	I_{OFF} (Amp)	I_{ON}/I_{OFF}	C_{gg} (Farads)	Intrinsic delay (Seconds)	DIBL (mV)	SS (mV/Decade)
[18]	3.12E-05	2.73E-12	1.14E+07	5.80E-17	1.86E-12	-	-
[22]	2.70E-05	3.45E-09	7.82E+03	3.08E-17	1.14E-12	-	-
Proposed low-kS asym HNWFET device	1.11E-05	6.90E-13	1.61E+07	1.23E-17	1.11E-12	7.32	61.97

4. CONCLUSION

The low-k source side asymmetric spacer halo-doped nanowire MOSFET is proposed in this paper. The simulation results demonstrate that the source side fringing fields are more compared to drain side fringing fields in the overall fields. Therefore, the asymmetrical use of low-k spacer material at the source side causes more reduction in fringing fields and it causes more reduction in gate capacitance and intrinsic delay. Among various spacer-engineered structures, the low-kS asym HNWFET structure has lower gate capacitance as 1.23×10^{-17} Farads and lower intrinsic delay as 1.11×10^{-12} seconds when low-k spacer material is SiO_2. We also observed that in the proposed structure there is a 74% reduction in gate capacitance and a 31% reduction in intrinsic delay as compared to high-k spacer structures. Further, the proposed structure is having almost ideal SS of 61.97 mV/decade and a very small DIBL of 7.32 mV. Hence, the proposed device is suitable for digital applications.

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BIOGRAPHIES OF AUTHORS

Padakanti Kiran Kumar was born in Telangana, India. He received a B.Tech. from JNTUH, M.Tech from KU, and is pursuing a Ph.D. in Koneru Lakshmaiah Education Foundation (Deemed to be University). He is presently working as an associate professor at the Department of Electronics and Communication Engineering, Balaji Institute of Technology and Science, Warangal, Telangana, India. His current research areas are FinFET and VLSI circuits. He can be contacted at kiranpadakanti0430@gmail.com.

Bukya Balaji was born in Telangana, India. He received a B.Tech. from JNTUH, M.Tech from JNTUA, and a Ph.D. degree from OPJS University. He is presently working as an associate professor at the Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation (Deemed to be University), Guntur, Andhra Pradesh, India. His current research areas are FinFET and VLSI circuits. He can be contacted at balaji@kluniversity.in.

Karumuri Srinivasa Rao was born in Andhra Pradesh, India. He received his master's degree from BITS Pilani, his Ph.D. degree from Central University. He is presently working as a professor and the head of the Microelectronics Research Group, Department of Electronics and Communication Engineering in Koneru Lakshmaiah Education Foundation (Deemed to be University), Guntur, Andhra Pradesh, India. His current research areas are MEMS-based reconfigurable antennas, MEMS actuators, bio-MEMS, RF MEMS switches, RF MEMS filters, MOSFET, FinFET, and VLSI circuits. He can be contacted at srinivasakarumuri@gmail.com.