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Ultra-wideband CMOS power amplifier for wireless body area network applications: a review

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ABSTRACT

A survey on ultra-wideband complementary metal-oxide semiconductor (CMOS) power amplifiers for wireless body area network (WBAN) applications is presented in this paper. Formidable growth in the CMOS integrated circuits technology enhances the development in biomedical manufacture. WBAN is a promising mechanism that collects essential data from wearable sensors connected to the network and transmitted it wirelessly to a central patient monitoring station. The ultra-wideband (UWB) technology exploits the frequency band from 3.1 to 10.6 GHz and provides no interference to other communication systems, low power consumption, low-radiated power, and high data rate. These features permit it to be compatible with medical applications. The demand target is to have one transceiver integrated circuit (IC) for WBAN applications, consequently, UWB is utilized to decrease the hardware complexity. The power amplifier (PA) is the common electronic device that employing in the UWB transmitter to boost the input power to the desired output power and then feed it to the antenna of the transmitter. The advance in the design and implementation of ultra-wideband CMOS power amplifiers enhances the performance of the UWB-transceivers for WBAN applications. A review of recently published CMOS PA designs is reported in this paper with comparison tables listing wideband power amplifiers' performance.

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1. INTRODUCTION

The continuous rising in the number of wireless network customers leads to fast growth in the communication systems architecture. To cover the increasing number of transmission channels effectively, new short-range wireless wideband technologies have been raised. Also, the increasing demand for low-power systems for portable and biomedical devices has directed research towards low-power technologies. Broadband wireless communication systems have become the major concern in the industry and the academic fields recently for applications in short-range and high-speed wireless systems. However, this wide bandwidth complicates the circuit-level implementation of the main RF blocks such as the power amplifiers (PAs), mixers, modulators, and demodulators in wireless transceivers.

Ultra-wideband (UWB) technique becomes among the widely recent communication techniques for short-range wireless communication interfaces that transmit data through a broad range of frequencies within

3.1-10.6 GHz with minimal radiated power and high data rates [1]. The UWB low radiated power density of −41.3 dBm/MHz saves the radiation from discovering and jamming, thus there is no need for complex security algorithms in micro transceivers. Consequently, UWB is the most appropriate technique for wireless communication systems in medical applications such as the wireless body area network (WBAN) [2]–[5]. WBAN consists of sensor nodes that are placed in several parts of the person and may be wearable or implanted under the user's skin. Each sensor node is responsible for measuring different changes in patient essential signs and sends the data to a common destination that is in charge of collecting all data from various sensor nodes [6]. Regularly there is communication among the wireless body sensors and the central node to collect all data and transmit it to a well-defined personal server located around the human body. After that a communication between the personal server and one or more access points is attained [7], [8] as shown in Figure 1. In this communication, the captured vital signs data may be forwarded to hospitals, doctors, or relatives to provide the patient with the appropriate treatment providing to establish real-time feedback to the patient and medical personnel without any disturbance. There are main requirements of the WBAN such as less response time, low power consumption, high privacy, and safety for continuous monitoring of patient status efficiently. For nearly all WBAN applications, the minimum dissipated power is the most important issue because of the limited battery lifetime [9], [10]. Thus, in order to assure power saving, UWB technology is employed. The vital signs data are transmitted to a personal server located around the body by using UWB transceivers.

Power amplifiers (PAs) are the critical component of the UWB transceiver. They include a trading-off between various performance parameters such as power added efficiency (PAE), output power, linearity, gain flatness, power dissipation, stability, input impedance matching, and output impedance matching. A high gain and good linearity are simultaneously required over a wide bandwidth, which causes the power amplifier to be the most power consumption component in a UWB transmitter. Although several works of power amplifier circuit design and implementation have been achieved [11]–[59], there is a challenge for wideband power amplifier design with low power consumption. This paper demonstrates a comprehensive review of the recent ultra-wideband complementary metal-oxide semiconductor (CMOS) power amplifier work. The rest of the paper is organized as follows: section 2 explains the different CMOS power amplifier topologies. CMOS power amplifier comparisons are tabulated in section 3, which are followed by brief conclusions in section 4.

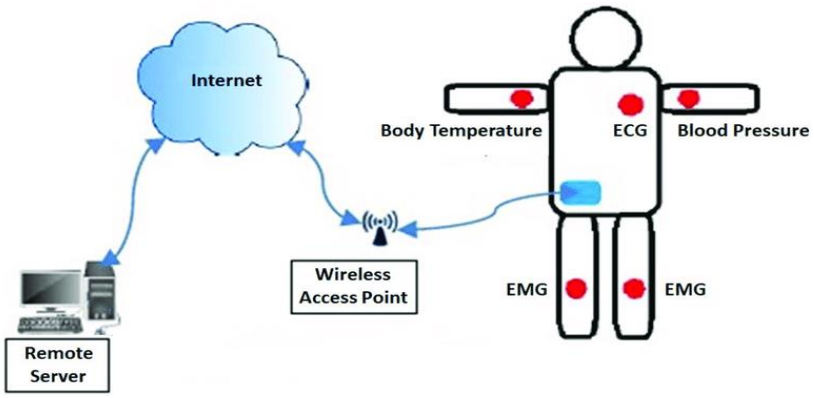


Figure 1. Basic architecture of wireless body area networks (WBAN) [7]

2. CMOS POWER AMPLIFIER TOPOLOGIES

The power amplifier (PA) is an electronic device used to amplify the power level in the transmitter, typically to drive the antenna and trade-off linearity and efficiency. It affects seriously the overall transceiver power dissipation, which decreases the power amplifier efficiency performance. Different implementation schemes of power amplifiers consist of three main configurations: cascaded power amplifier topology, cascode power amplifier topology, and shunt feedback topology. In the next subsections, different topologies for the design of CMOS power amplifiers are demonstrated by indicating the pros and cons.

2.1. Cascaded power amplifier topology

Instead of utilizing a single-stage power amplifier, multiple power stages connected in series are employed in the cascaded power amplifier topology as shown in Figure 2. In this configuration the output of the first common source power amplifier is fed to the input of the second common source power amplifier. Cascaded power amplifier topology allows the gain to increase as the number of power amplifiers increases. The advantages of cascaded power amplifier topology are the large power gain and high gain bandwidth

product. The negative side of the cascade topology is that it has high power consumption and high silicon area due to the increase in hardware components. Several previous works employ the cascaded configuration in the design and implementation of power amplifiers in order to have high gain [11], [12], [16], [17], [21], [22], [39], [45], [48],[52], [54]–[56], [59].

2.2. Cascode power amplifier topology

In this configuration, a common source stage amplifier is followed by a common gate stage to form the cascode topology [23]–[27], [34], [35], [38], [40], [49], [53] as shown in Figure 3. Mostly the cascode power amplifier topology is employed to enhance the performance of the power amplifier. There are several advantages of this configuration including high bandwidth, boost gain, less slew rate, high stability and reducing miller capacitances [23]–[27], [34], [35], [38], [40], [49], [53]. Also, better isolation between the input and output ports is attained by the cascode scheme. Moreover, a two-transistor circuit is utilized to form the cascode configuration which has an extremely low number of parts but this affects the headroom output voltage. Thus, the cascode power amplifier topology requires two transistors with a high voltage supply to compensate for the losses in the voltage headroom. As well the cascode power amplifier configuration has great output impedance which makes it difficult to match this major impedance with a 50 ohm load antenna. The cascode CMOS power amplifier scheme is utilized in prior work to produce higher power-added-efficiency PAE and boost the gain [23]–[27], [34], [35], [38], [40], [49], [53].

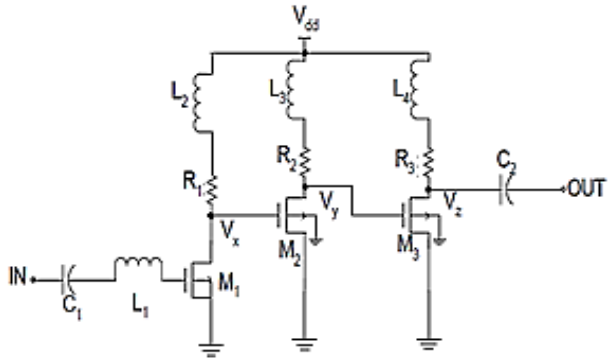


Figure 2. Cascaded CMOS power amplifier [11]

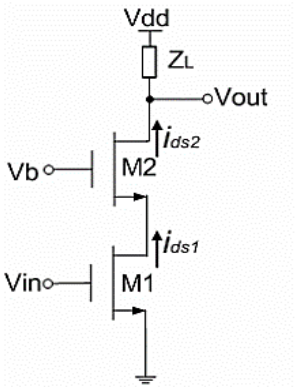


Figure 3. Cascode CMOS power amplifier [24]

In order to reduce the power consumption of the cascode amplifier, a feedback signal is established between the output from the drain of the first common source amplifier and the gate of the second common gate amplifier. Consequently, the common gate amplifier M2 is converted into a common source amplifier as shown in Figure 4. This is known as cascode current-reused topology [24], [49] The two transistors M1 and M2 in Figure 4 share the same bias current thus lowest power is consumed.

2.3. Shunt feedback power amplifier topology

A shunt feedback topology network usually comprises a resistor as shown in Figure 5. The shunt feedback topologies support the amplifier to be more stable and have high gain flattens, extended bandwidth of the amplifier, and wideband impedance matching [35]. The negative side of feedback topology is that the power gain decreases, thus the shunt feedback topology is employed with the cascaded scheme and/or the cascoded scheme to enhance the gain as illustrated in the next subsection.

2.4. Hybrid technique power amplifier

A hybrid technique power amplifier is a combination of the three main configurations of a power amplifier: cascaded topology, cascode topology, and shunt feedback topology. As shown in Figure 6, by combining more than one topology into the design of a power amplifier, many advantages can be achieved as compared with the one topology design [13]–[15], [18], [21], [28]–[33], [36], [37], [41]–[44], [48]–[50], [51], [57], [58]. To attain extra gain, several works have employed the cascode power amplifier topology followed by common-source topology [28]. Also, a broad bandwidth, great stability, and good input matching can be offered with this hybrid technique. This Hybrid power amplifier scheme (cascode and common-source topology) is shown in Figure 6(a).

Different works have utilized the cascode power amplifier topology with the shunt feedback topology in order to attain wide bandwidth, good gain flatness, high linearity, and wideband matching [13]. This hybrid power amplifier scheme (cascode and shunt feedback topology) is shown in Figure 6(b). Cascaded power amplifier topology with cascode current-reused power amplifier topology has been utilized for great wideband input/output matching, gain, and gain flatness, and low power consumption [41]. This Hybrid power amplifier scheme (cascaded and cascode current-reused topology) is shown in Figure 6(c). Several works have employed the three different configurations (cascaded topology, cascode topology and shunt feedback topology) in order to enhance the gain, bandwidth and stability [18] as shown in Figure 6(d).

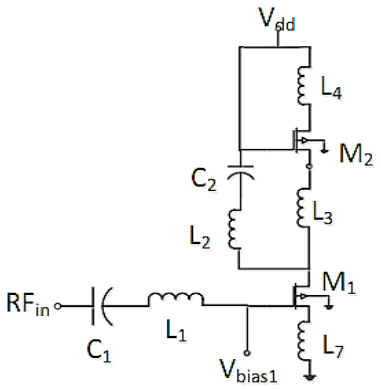


Figure 4. Cascode current-reused CMOS power amplifier [24]

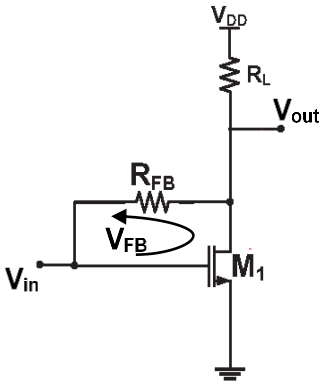
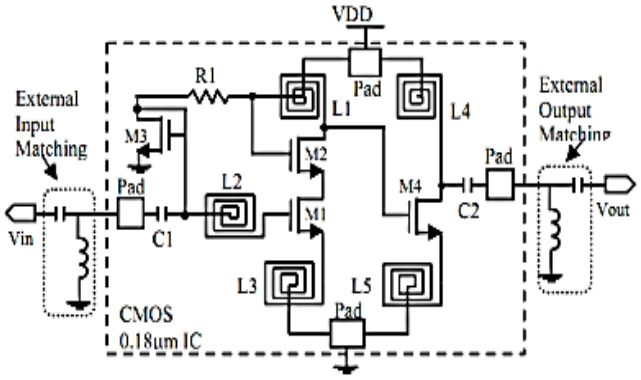
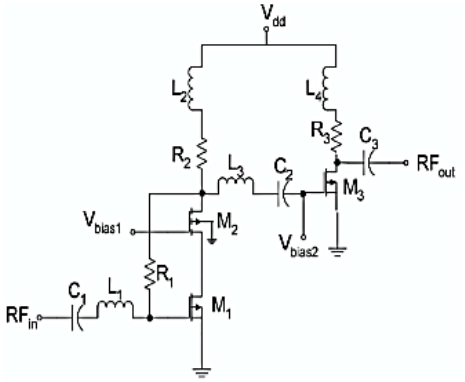


Figure 5. Resistive shunt feedback CMOS power amplifier [35]



(a)



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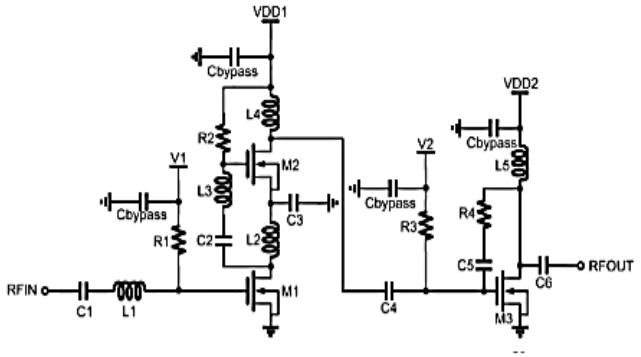
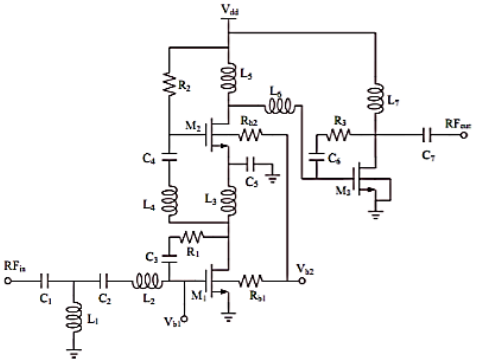


(c)



(d)

Figure 6. Hybrid technique power amplifier: (a) cascode and common-source topology PA [28], (b) cascode and shunt feedback topology PA [13], (c) cascaded and cascode current-reused topology PA [41], and (d) cascaded, shunt feedback, and cascode current-reused topology PA [18]

3. WIDEBAND CMOS POWER AMPLIFIERS

In this section, a review of several published wideband power amplifiers is demonstrated [11]–[20], [21]–[30], [31]–[40], [41]–[50], [51]–[59]. A performance comparison between different schemes of power amplifier implementation is obtained in Tables 1 to 3. The main performance parameters of prior work power amplifiers such as required power, power gain, operating frequency range, linearity, power added efficiency (PAE), compression point, power consumption, and area are listed in columns 3 to 11 in Tables 1 to 3.

3.1. Summary of the published wideband cascaded power amplifiers

There have been various works on the wideband CMOS cascaded power amplifier [11], [12], [16], [17], [21], [22], [39], [45], [48], [52], [54]–[56], [59]. A summary of the published wideband cascaded power amplifiers is presented in Table 1. As stated in section 2. A cascaded power amplifier topology has been employed to boost the power gain. However, increasing the number of stages utilized in the power amplifier design will result in a greater increase in power consumption and area. Thus, almost all prior works have employed three-stage cascaded power amplifiers [11], [17], [39], [45], [52], [54], [59] or two-stage cascaded power amplifiers [12], [16], [21], [22], [48], [55], [56].

Table 1. Summary of the published wideband cascaded power amplifiers

Reference	Process (nm)	Frequency range (GHz)	Supply voltage (V)	Output P1dB (dBm)	Gain (dB)	S11 (dB)	S22 (dB)	Power (mW)	PAE%	Area (mm^2)
[11]**	180	3.1 to 10.6	2.5	5	11.48±0.6	<-10	<-14	100	---	0.88×0.78
[17]**	180	3.1 to 10.6	---	5	11.48±0.6	<-10	<-14	100	16	0.88×0.78
[39]*	180	6 to 10.6	1.5	0	11	<-8	<-11	18	---	0.94×0.82
[45]*	180	3 to 6.2	1.8	---	11±0.6	<-14	<-12	13	---	0.86×0.81
[52]**	180	6 to 9	1.8	>3.5	10	<-10	<-35	21	---	1.1×0.8
[54]**	65	3.4 to 4.8	4	17.4	13.65 ±0.25	<-9.4	<-16.7	---	24.6	0.61×0.84
[55]*	180	3.1 to 7.5	1.2	0.5	11.4±0.8	<-11.1	<-10.5	14.5	---	0.99×0.968
[59]**	65	3 to 10	4	16±2.1	12.65±1.25	<-8.75	<-15.6	---	20.15±7.55	0.61×0.84
[12]**	180	6 to 10	1.5	5 (6-9.8GHz)	8.5	<-7	<-7	18	11.4	0.82×1.32
[16]*	180	3.1 to 10.6	1	2	10.6±0.8	<-15.8	<-9	14.3	---	0.96×0.95
[21]*	180	3.1 to 4.8	1	---	14.45±1.05	<-1.4	<-19	35.5	---	1.587×1.338
[22]*	180	3 to 7	1.8	7.21 (5GHz)	12±0.8	<-10	<-11	32	38.5 (5GHz)	0.97×0.78
[48]**	180	3.1 to 4.8	1	11	14.45±1.05	<-1.4	<-1.9	35.5	---	1.587×1.338
[56]*	180	3.1 to 10.6	2	11 (9 GHz)	12.5±1.5	<-4.5	<-8.5	36	32.5 (4GHz)	0.55

*Simulated **Measured

To increase the overall gain, prior works have employed three-stage cascaded power amplifiers. In [11], [17], three stages of cascaded common source power amplifiers have been employed working at frequency range 3.1 to 10.6 GHz to achieve a wide spectrum range with a flat gain of 11.48±0.6 dB, which lead to an increase in power consumption by 100 mW. Also, a high power added efficiency of 16% has been obtained [17]. In [52], a three-stage cascade amplifier has been employed. An input stage of a complementary amplifier has been used followed by two common source amplifiers. The power amplifier (PA) achieved a power gain of 10 dB in the range of 6 to 9 GHz with a power consumption of 21 mW from a 1.8 V power supply.

Also, different three-stage cascaded scheme has been utilized in [39], [45]. The first stage consists of a common gate (CG) amplifier with a current-reused configuration for wideband input matching and saving power consumption. A common source amplifier has been used in the second stage to enhance the gain. The third stage included a source follower transistor (output buffer) for output impedance matching. These power amplifiers [39], [45] achieve a gain of 11 dB operating in the frequency range 6 to 10.6 GHz and 3 to 6.2 GHz, with a power consumption of 18 and 13 mW at 1.5 and 1.8 V supply voltage, respectively. The same cascaded scheme has been utilized in [55] except for the last buffer stage. A common gate with a current-reuse scheme operating in the frequency band of 3.1 to 7.5 GHz has been attained to provide wideband input matching and good linearity. The achieved gain is 11.4 dB with a power consumption of 14.5 mW from a 1.2 V supply voltage. In [54], [59], a power cell contains a stage of a common source amplifier with three stacked common gates connected in series has been employed to obtain a great output power level by using a high supply voltage of 4 V. These power amplifiers [54], [59] accomplished a gain of 13.65 and 12.65 dB with PAE of 24.6%, and 20.15%, respectively.

A two-stage cascaded power amplifier has been attained [12], [16] including the common-gate stage and common source stage. The input stage has two common-gate (CG) transistors, the first CG transistor has been employed for impedance matching and the second CG transistor has been employed for isolation between the first and the second stage. The two-stage amplifiers [12], [16] provide a gain of 8.5 and 10.6 dB for the frequency ranges of 6-10 GHz and 3.1 to 10.6 GHz, respectively. Also, a high saving of power has been achieved at 18 and 14.3 mW, respectively.

Similarly, a common-gate stage followed by a common-source CS stage operating in the frequency bands of 3 to 7 GHz and 3.1 to 10.6 GHz has been attained in [22], [56], respectively. The input stage includes a CG transistor loaded by a diode-connected transistor to increase the first stage gain. The proposed PAs achieved gains of 12 and 12.5 dB, respectively. A high PAE of 38.5% and 32.5% are achieved by employing the source and load-pull simulation. In [21], [48], two-stage cascaded amplifiers formed of a common source transistor in each stage have been used. This configuration achieves a high-power gain of 14.45 dB but with a great power consumption of 35.5 mW.

3.2. Summary of the published wideband cascode power amplifiers

The wideband CMOS cascode power amplifier [23]–[27], [34], [35], [38], [40], [49], [53] review is presented in this subsection. A summary of the published wideband cascode power amplifiers is listed in Table 2. The power consumption may be reduced by utilizing the current reuse scheme. Also, increasing the linearity is accomplished by employing the self-biased circuit. In [23], [49], a one-stage cascode power amplifier in the frequency band of 3 to 5 GHz has been attained with a gain of 13.3 and 13 dB, and PAE up to 15.32%, and 15.14%, respectively. In [35], a one-stage cascode power amplifier with a shunt feedback network operating in the frequency band of 3.1 to 4.8 GHz has been attained with a high gain of 19±1 dB and power dissipation of 25 mW from 1.8 V supply voltage.

Table 2. Summary of the published wideband cascode power amplifiers

Reference	Process (nm)	Frequency range (GHz)	Supply voltage (V)	Output P1dB (dBm)	Gain (dB)	S11 (dB)	S22 (dB)	Power (mW)	PAE%	Area (mm^2)
[23]**	180	3 to 5	1.8	1.08	13.3±1	<-7.5	<-7	25.2	15.32	---
[26]*	180	3.1 to 10.6	1.8	---	18±0.2	<-10	<-8.4	---	---	---
[34]*	180	3 to 5	1.2	6.6	16±0.5	<-11	<-8.5	23.2	16.4	0.75
[24]**	180	3.1 to 4.8	1.8	8(4GHz)	10.3±0.8	<-5	<-8	24	40.5	0.97
[35]*	180	3.4 to 4.8	1.8	-4.2	19±1	<-10	<-8	25	---	1.9×1.1
[49]*	180	3 to 5	1.8	---	13	<-9	<-13	15.1	15.14	---
[49]*	180	3 to 5	1.8	---	15	<-7.5	<-7.5	14.8	24	---
[25]*	130	2 to 5.2	2	-8	16	<-9	<-15	38	---	0.4×0.6
[27]*	180	4.1 to 4.6	1.8	---	---	---	---	34.7	47.5	1×2
[38]**	180	3.1 to 10.6	1.8	0	>10(3.1-9) >6 (9-10)	<-9	<-8	25.2	---	1.1×1
[40]**	180	3.1 to 4.8	---	2.57	15.57	<-10	<-10	---	5.8	1.57×0.97
[53]**	180	3.1 to 10.6	1.8	-1.5	13.1±1	<-5.5	<-7	21	---	1.05×0.76

*Simulated **Measured

In [24], [26], [49], a one-stage cascode with current reused configuration has been proposed to decrease the power consumption. Good gains of 10.3 dB, 18 dB, and 15 dB in the frequency range of 3.1 to 4.8 GHz, 3.1 to 10.6 GHz, and 3 to 5 GHz have been achieved, respectively. The proposed PA in [24] achieved good linearity and high efficiency of 40.5% with a power consumption of 24 mW. In [34], a folded topology one-stage has been utilized in the range of 3 to 5 GHz. It attained a high gain of 16 dB ±0.5 dB flatness while consumed only 23.2 mW from 1.2 V supply voltage.

Two-stage cascode scheme has been implemented in [25], [27], [38], [40] for broadband matching and better input-output isolation. In [25], two stages cascode power amplifier with single-ended input and a differential output has been employed. It achieved 16 dB gain in a range of 2 to 5.2 GHz with 38 mW power consumption. Also in [27], a two-stage cascode PA achieved higher power added efficiency by 47.5% in the frequency range of 4.1 to 4.6 GHz. The proposed PA in [38] provided a power gain greater than 10 dB in the operating band of 3.1 to 9 GHz, with a power consumption of 25.2 mW. Also in [40], two stages cascode scheme with shunt-shunt feedback has been utilized in the 3.1 to 4.8 GHz frequency range. It achieves 15.57 dB power gain, however with low power added efficiency of 5.8%. Additionally in [53], two stages cascode with the current-reused scheme have been utilized for low-power consumption and high-gain performance in the full range of 3.1 to 10.6 GHz. The average gain is 13.1 ±1 dB, and the power dissipation of 21 mW.

3.3. Summary of the published wideband hybrid-technique power amplifiers

In the hybrid technique, more than one of the different implementation schemes of the wideband power amplifier was combined together to get the advantage of each scheme which makes that scheme the most attractive for the design of PAs. This technique has been widely used [13]–[15], [18], [21], [28]–[33], [13], [37], [41]–[44], [46], [48]–[51], [57], [58]. A summary of the published wideband hybrid-technique power amplifiers is presented in Table 3. Almost all these configurations are composed of two stages of amplification. A cascode topology has been employed in the first stage and a common-source amplifier has been employed in the second stage.

Table 3. Summary of the published wideband hybrid-technique power amplifiers

Reference	Process (nm)	Frequency range (GHz)	Supply voltage (V)	Output P1dB (dBm)	Gain (dB)	S11 (dB)	S22 (dB)	Power (mW)	PAE%	Area (mm^2)
[13]**	180	3.1 to 6	1	5.8	10±1	<-6	<-7	30	---	---
[14]*	180	5 to 9	1.8	3	16±0.4	<-4	<-5	25	12.4	0.95×0.98
[15]**	180	5 to 10.6	1	2	14±1	<-5.5	<-7	20	10	0.87×0.89
[18]**	180	3.1 to 6	---	5.8	10±1	<-6	<-7	30	15.5	0.86×0.78
[21]*	180	6 to 10.6	1.5	0	11	<-8	<-11	18	---	0.94×0.82
[28]*	180	3 to 7.9	1.8	---	18.8	<-2	<-6.6	30	---	---
[29]**	180	2.6 to 5.4	1.5	11.4	15.8	<-5	<-6	25	34	1.1×1.5
[30]**	180	3.1 to 4.8	1.8	9.8	22.3	<-5.7	<-5.5	25	26	1.1×1.5
[31]*	180	3 to 7	1.8	8.2(5GHz)	19±0.3	<−7.5	<-6	28	29(5GHz)	0.88×0.852
[32]**	180	1.5 to 5	1.8	6.7	20(4GHz)	---	---	24.5	22	1.222×1.004
[33]*	180	2.2 to 5	1.8	14.5	15.6	<-1.29	<-10.11	77.3	39.6	---
[36]*	180	3.1 to 4.8	1	6(4GHz)	18.4±1	<-5	<-5	22	18	0.95×1.02
[37]**	180	3 to 7	1	7	14.5±0.5	<-6	<-7	24	---	0.85×1.03
[41]**	180	3.1 to 10.6	0.9	4.3	15±1	<-6.5	<-7.6	14.4	---	0.74×0.71
[42]**	180	3 to 5	1.8	10.1	16.2	<-6	<-0.5	25	47	---
[43]*	40	5-13	1	---	>10	<-10	<-10	---	24	---
[44]**	180	3 to 10.6	---	9(7GHz)	11.5±0.8	<-8.5	<-8	34	26(7GHz)	0.93×0.87
[48]**	180	3.1 to 4.8	1	8	23.9±1.6	<-4.6	<-1.3	26.7	---	1.612×1.266
[49]*	180	3 to 5	1.8	---	25	<-7.5	<-17.5	22.6	23.81	---
[50]*	180	3.1 to 10.6	---	---	28.7±2	<-10.2	<-13.7	---	33	---
[51]**	130	3.1 to 5.1	1.8	---	20.3±0.8	<-1.5	<-6	27.3	---	---
[57]**	65	3.1 to 10.6	1.2	6.8	22.8±1.2	<-7	<-10	15.5	29.5(6GHz)	1.17
[58]*	130	3 to 5	1.2	-3	18.8±0.3	<-5	<-3	---	---	1.22×0.8
[46]*	180	3.1 to 10.6	1	---	12.4±1.1	<-8.6	<-8.6	19	---	0.99×0.96

*Simulated **Measured

Three schemes of the cascode power amplifiers are adopted. First, cascode topology has been employed in the first stage followed by a common source amplifier in the second stage to attain optimal output power and gain through wide bandwidth [28]–[30], [33], [42], [48]. Second, cascode topology with shunt feedback has been utilized in the first stage to provide wideband input matching, followed by a common-source amplifier [13], [18], [21], [31]. Third, cascode current-reused configuration has been used in the first-stage with common-source amplifier in the second stage to reduce the consumed power while obtain good gain performance [14], [15], [32], [36], [37], [41], [44], [49]–[51], [57].

Differently, in [43], two-stage PA in the 40 nm CMOS process has been utilized to achieve high gain in the band of 5 to 13 GHz. The PA employd CS with resistance shunt feedback in the first stage and cascode topology in the second stage to provide good matching of less than -10 dB and stability with power added efficiency of 24%. Also in [46], two stages common source amplifier with resistive shunt feedback followed by a cascode amplifier scheme operating in the frequency band of 3.1 to 10.6 GHz have been employed. The power gain of 12.4±1.1 dB and less power dissipated of 19 mW have been achieved. In [58], two stages of cascode amplifiers with a common source (CS) scheme as the third stage have utilized to increase the power gain. Nearly 18.86 dB power gain has been accomplished and attained an excellent flatness of about ±0.3.

A number of the published power amplifiers used a single-stage common-source amplifier [21], [47]–[49]. The proposed single-stage PA topology [21] has been achieved with a gain of 8.95 dB and power consumption of 23 mW. In [47], the amplifier attains PAE of 23.2% in the frequency band 6-9 GHz. The proposed PA [48] uses a single-stage amplifier and accomplishes a power gain of 7.05 dB at 3.25 GHz while consuming 21 mW. The implemented PA [49] accomplished a power gain of 11.5 ± 0.4 dB. The power consumption is 7.67 mW at 1.8 V DC supply voltage.

Figure 7 shows the percentage of employing one, two, and three amplification stages [11]–[59]. As presented in this figure, using a one-stage amplifier [21], [23], [24], [26], [34], [35], [47]–[49] and a three-

stage amplifier [11], [17], [39], [45], [55] are slightly used. The most used number of stages for power amplification is a two-stage amplifier [12], [16], [48]–[50], [53], [57], [21], [22], [25], [27], [28], [30], [38], [40]. It is considered a compromise regarding gain, gain flattens, bandwidth, power consumption, and area.

There is a tradeoff between gain, power consumption, impedance matching, and power added efficiency (PAE). As a compromise between higher gain and lower power consumption, the cascode scheme and cascode current-reused scheme are employed. For ultra-wide CMOS power amplifiers for WBAN applications, higher power gain levels are required without sacrificing power consumption. Cascode schemes can achieve high gain and less power consumption for power amplifier implementation which makes that scheme the most attractive for WBAN applications [23], [24], [26], [30], [34], [35], [48]–[50], [57].

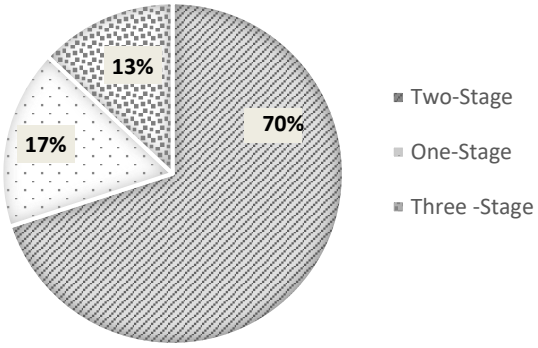


Figure 7. The percentage of one-stage, two-stage, three-stage published papers

Figures 8 to 14 present comparisons among different PA techniques for five published papers in terms of the power gain (dB), PAE (%), power consumption (mW), area (mm^2), gain flatness (±dB), input matching S11 (dB), and output matching (dB), respectively. Among the PA techniques are one-stage common-source amplifier [21], [47]–[49], two-stage cascaded amplifier [12], [16], [21], [22], [48], three-stage cascaded amplifier [11], [17], [39], [45], [55], one-stage cascode amplifier [23], [24], [26], [34], [35], two-stage cascode amplifier [25], [27], [38], [40], [53], and two-stage hybrid amplifier [30], [48], [49], [50], [57].

Concluding the results demonstrated in Tables 1 to 3 and Figures 8 to 14:

- As expected, employing the cascode scheme (one-stage, or two-stage, or hybrid) increases the power gain. The highest power gain of 25 dB, 28.7 dB, and 22.8 dB has been achieved by [49], [50], [57], respectively, which utilized cascode current-reused configuration followed by a current-source amplifier as shown in Figure 8.
- The greatest PAE of 47.5% has been achieved utilizing the two-stage cascode technique [27]. The two-stage hybrid amplifier technique attains high values of PAE by 26%, 23.81%, 33%, 29.5 % [30], [49], [50], [57], respectively, as shown in Figure 9.
- From a low-power point of view, utilizing a single-stage common-source PA minimizes the power consumption [21], [48], [49] as shown in Figure 10. Also, employing the cascode scheme helps to reduce the power consumption [23], [24], [34], [35].
- Area comparisons among different PA techniques are shown in Figure 11. A conservative area of less than 1 mm^2 has been achieved by employing the cascaded common-source techniques.
- High gain flatness can be achieved by employing more than one stage [17], [45] as shown in Figure 12. The first and second stages accomplish gain at lower corner and upper-end frequency respectively, whilst the third stage smoothed the gain flatness curve. Also, stagger tuning technique is employed to enhance the gain flatness [11], [26].
- For broad input matching, a common-gate (CG) stage is employed in the first stage [16], [22], [45], [55]. The input return loss (S11) is less than -15.8 dB, -10 dB, -14 dB, -11.1 dB [16], [22], [45], [55], respectively, as shown in Figure 13.
- In addition, employing the resistive shunt feedback technique in the first stage decreases the input return loss. This technique has been proposed in most published work [11], [17], [26], [35], [40]. Less than -10 dB input return loss S11 has been achieved [11], [17], [26], [35], [40]. The same for the output matching is shown in Figure 14.
- Also, to summarize Figures 8 to 14, a performance comparison among different PA configurations of the published wideband CMOS power amplifiers is listed in Table 4. Two-stage hybrid configuration is the best solution for high power gain and PAE with moderate power consumption.

– Figures 15 and 16 report the power gain versus the PAE%, and the power gain versus the power consumption for several CMOS power amplifier techniques [11]–[20], [21]–[30], [31]–[40], [41]–[50], [51]–[59].

Clearly, for the CMOS power amplifier designers, Figures 15 and 16 with Table 4 help in studying different optimizations that have been achieved to compromise the power gain with PAE%, power consumption, gain flatness, and input/output matching.

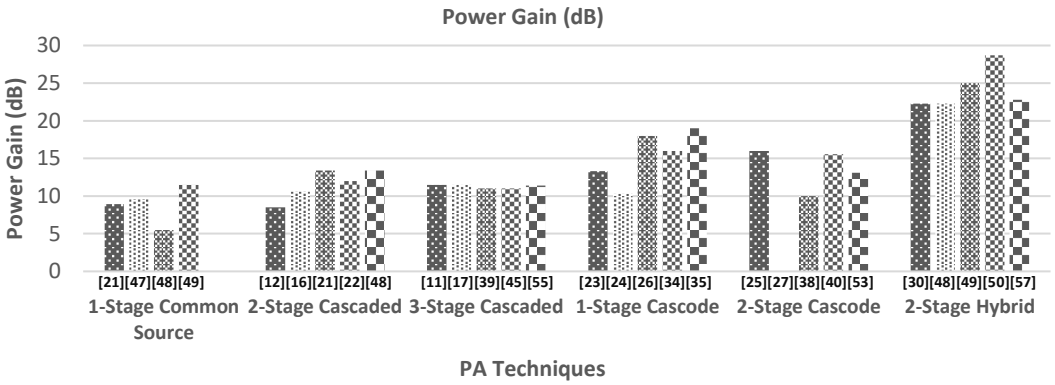


Figure 8. Power gain comparison among different PA techniques for five published papers

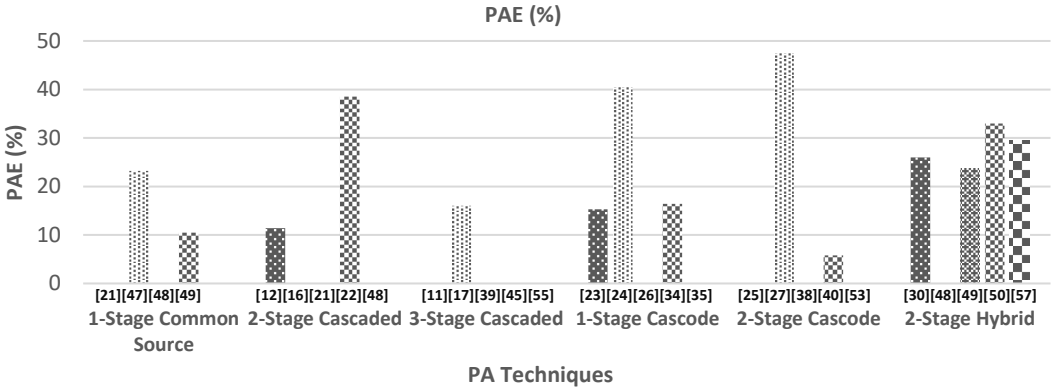


Figure 9. Power added efficiency (PAE%) comparison among different PA techniques for five published papers

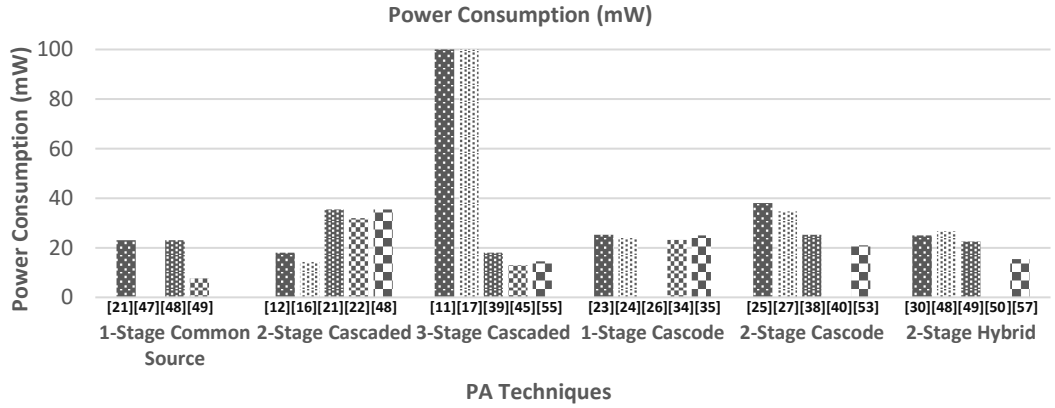


Figure 10. Power consumption comparison among different PA techniques for five published papers

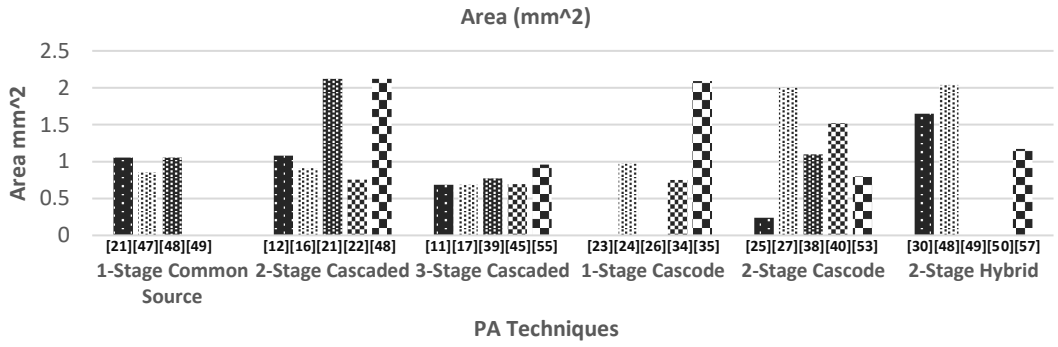


Figure 11. Area comparison among different PA techniques for five published papers

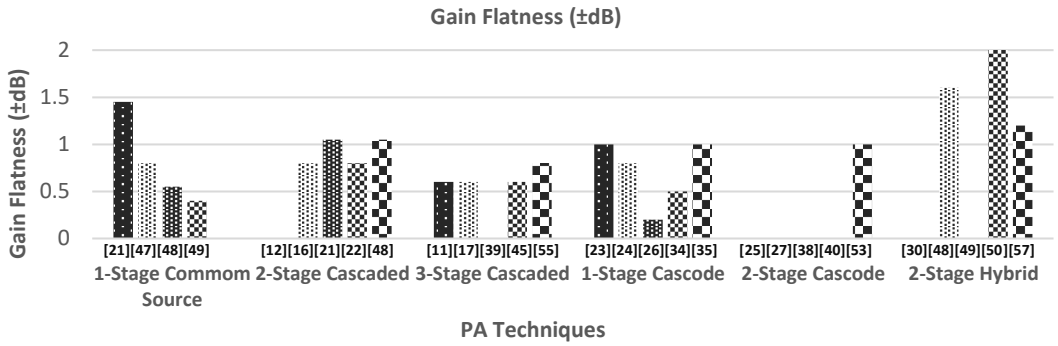


Figure 12. Gain flatness comparison among different PA techniques for five published papers

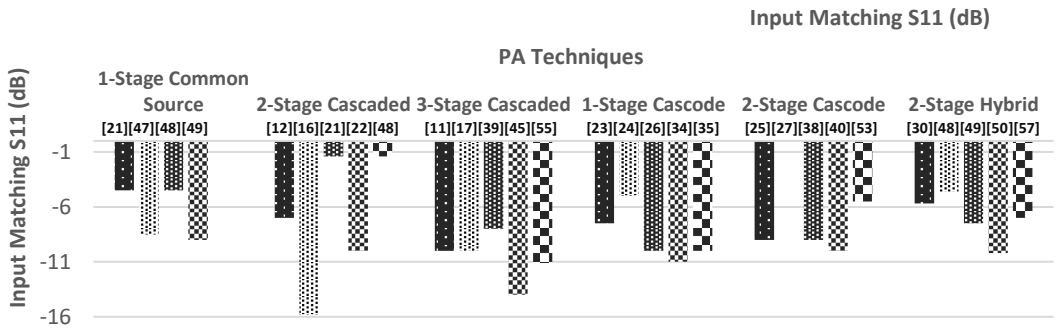


Figure 13. Input matching (S11) comparison among different PA techniques for five published papers

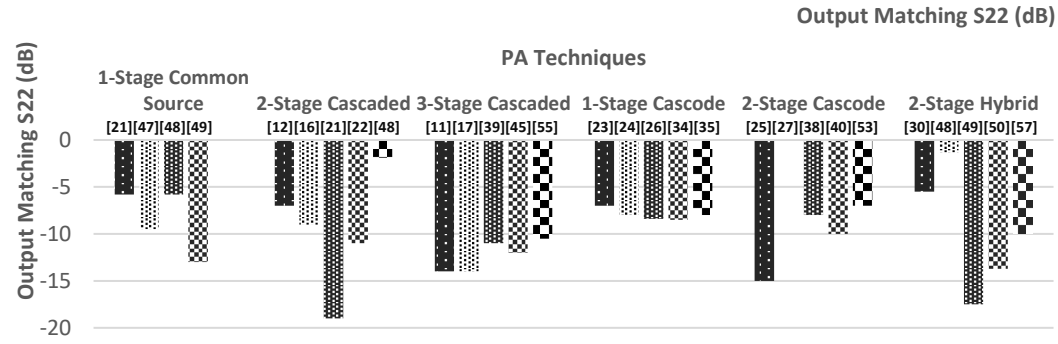


Figure 14. Output matching (S22) comparison among different PA techniques for five published papers

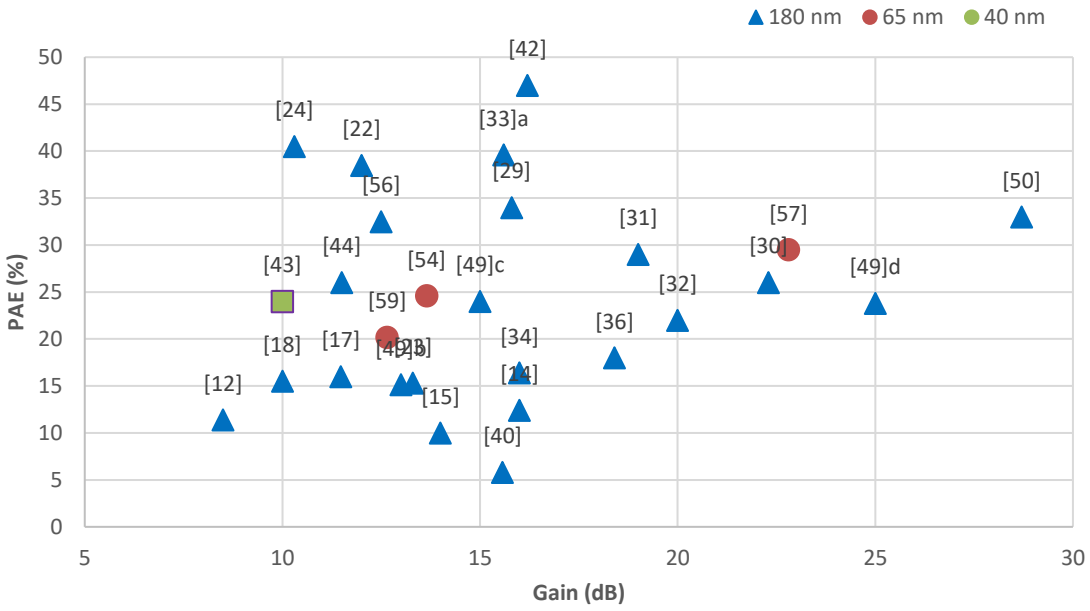


Figure 15. The power gain versus the PAE% for several CMOS power amplifier techniques [11]–[59]

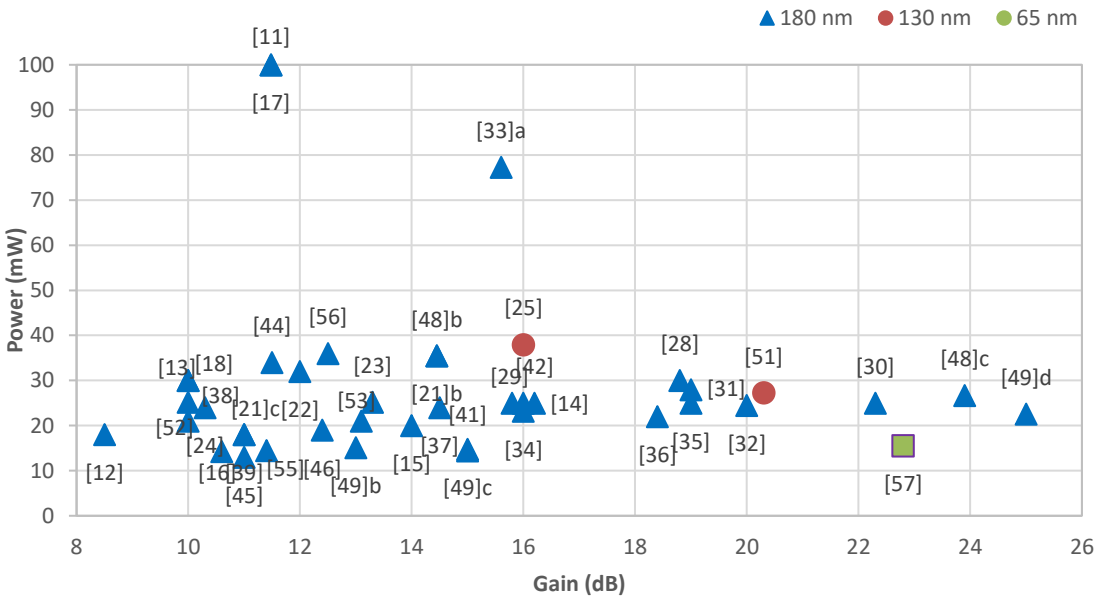


Figure 16. The power gain versus power consumption for several CMOS power amplifier techniques [11]–[59]

Table 4. Performance comparison among different PA configurations of the published wideband CMOS power amplifiers

Architecture	One-Stage Common Source	Two-Stage Cascaded	Three-Stage Cascaded	One-Stage Cascode	Two-Stage Cascode	Two-Stage Hybrid
No. of Transistors	One	Two	Three	Two	Four	Three
Power Gain	Moderate	Moderate	Moderate	High	High	Highest
Gain Flatness	Good	Poor	Very Good	Poor	Poor	Very Poor
PAE	Low	Moderate	Low	High	Moderate	Highest
Power Consumption	Moderate	High	Highest	Moderate	High	Moderate
Total Area	Moderate	Large	Small	Moderate	Large	Large

4. CONCLUSION

UWB technique is a preferable solution for WBAN applications because of the advantage of low cost, less area, and great power savings. The most hardware expensive part of the UWB transceivers is the PA. Different design schemes for wideband PA have been demonstrated in this review. Cascaded topology with CS configuration has been utilized to enhance the gain and provide the required output power in the UWB transmitter. A common gate scheme has been used to attain a broad range of input matching. Also, RLC matching networks support a broad range of matching with low power dissipation. Shunt feedback topology produces the required matching at both the I/O, and in addition provides high stability and achieves flat gain. A cascode current-reused topology which share the same bias current has been employed to attain lowest power consumption. Modern prior wideband power amplifier architectures have been presented in this survey.

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