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Inductively coupled distributed static compensator for power quality analysis of distribution networks

Praveen Kumar Yadav Kundala[1], Mrutyunjaya Mangaraj[2], Suresh Kumar Sudabattula[1]
[1]School of Electronics and Electrical Engineering, Lovely Professional University, Punjab, India
[2]Department of Electrical and Electronics Engineering, Lendi Institute of Engineering and Technology, Vizianagaram, India

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ABSTRACT

In this research paper, an inductively coupled distributed static compensator (IC-DSTATCOM) for three phase three wire (3P3W) electric power distribution system (EPDS) is proposed. The contraction of power quality (PQ) was marked as a perilous droop mode bump into direct coupled distributed static compensator (DC-DSTATCOM). To regain the PQ, inductive coupling transformer is assisted in conjunction with DC-DSTATCOM. The system equivalent circuit of IC-DSTATCOM is accomplished by take into account of impedance of both transformer and DC-DSTATCOM to reveal the filtering technique. The filtering *icos∅* mechanism is performed by following the generalized mathematical approach using MATLAB/Simulink. A case education is reviewed in detail to illustrate the performance of both DC-DSTATCOM and IC-DSTATCOM. The IC-DSTATCOM is amplified healthier as compared to other in terms of harmonics shortening, good power factor, load balancing, and potential regulation. To examine the effectiveness, simulation outputs of the IC-DSTATCOM with different PQ parameter indices are presented by following the benchmark measure of IEEE-2030-7-2017 and IEC-61000-1 system code.

Corresponding Author:

Praveen Kumar Yadav Kundala
School of Electronics and Electrical Engineering, Lovely Professional University
Punjab, India
Email: praveen263@mail.com

1. INTRODUCTION

The proportion of power electronics and microprocessor based nonlinear load in the electric power distribution system (EPDS) has been increasing in recent years. Including these, electric vehicle charging station, electric traction as well as renewable energy system are also playing a growing role in the EPDS. Hence, improvement for sustainability and flexibility of EPDS is very challenging and important task for such scenarios [1]–[4]. As a result, possibility of quality power delivery to the consumers using improved technology will make EPDS very attractive.

Of course, lot of researchers are done very good research on droop mode bump into direct coupled distributed static compensator (DC-DSTATCOM) with self-supported capacitance. The main advantages of DC-DSTATCOM: i) it achieves reduced static error and quick convergence characteristics and ii) the features like heftiness, tracking and adaptive capabilities under adjustable loading periodicity are obtained. But in DC-DSTATCOM, the point of common coupling (PCC) possesses various severities due to the direct connection of DSTATCOM, supply and load. Hence, flow of short circuit current, poor protection, some thermal losses are occurred [5]–[8].

Due to these drawbacks of DC-DSTATCOM, nowadays the development was started in the area of inductively coupled distributed static compensator (IC-DSTATCOM). It is obtained by connecting the non-linear loads to the source through a coupling transformer. It bears number of merits such as less switching stress, flexibility, controllability, improved balance voltage at PCC, increasing the compensation capability, and different possible combinations for extension etc. In view of the design aspect of the DC-DSTATCOM, the self-supported capacitor and split capacitor topology are suitable for three phase three wire (3P3W) EPDS. But, three leg voltage source converter (VSC) topology is widely put forward due to its own popularity, in the literature survey [9]–[14].

Keeping extend improvement of the above-mentioned DC-DSTATCOM, the need of the IC-DSTATCOM is anticipated to execute better in the real situation. The DC-DSTATCOM topologies with star/delta transformers for other two isolated topologies are shown in cited literature. In this case, a star/delta transformer with a kilovolt ampere (kVA) rating equal to the necessary reactive power injection is required [15]–[19]. However, the inductive transformer creates isolation between the device and system as well as for the desired application. This type of DC-DSTATCOM can, however, be configured in a number of ways using different transformers.

The proposed scheme provides flexibility for further improvement for connecting additional converters and loads. With the target of better compensation and stability of inductively filter converting transformer (IFCT), the matching of impedance design structure between DC-DSTATCOM, converting transformer is structured in detail. Balancing of supply current, input supply current harmonics drop, balancing of load at output, improvent in power factor (PF), potential control are all examples of efficiency improvements [20]–[26].

The filtering mechanism is performed by following the generalized mathematical approach using *icosØ* algorithm using MATLAB/Simulink. The subsequent conclusions can be drawn from the proposed IC-DSTATCOM scheme's control algorithm; i) improved convergence performance can be achieved; ii) this algorithm's most notable features are its enhanced tracking, adaptive, and compensation abilities; and iii) it cares the proposed structure for accomplishing the various PQ issues such as harmonics drop, healthier potential regulation, pf modification, and output load balancing and lesser DC link potential of the IC-DSTATCOM.

Here in this research presentation, an overview of research and research inspiration is roofed in section 1. In section 2, the network alignment and modelling of DC-DSTATCOM and IC-DSTATCOM is presented and deliberated. In section 3, modelling and design of inductive transformer is analyzed. The section 4 describes about the detailed implementation of *icosϕ* control algorithm under the different case studies. Simulation outcomes are presented to validate the effectiveness of the suggested topology in section 5. At last, the conclusion is careworn in section 6.

2. MODELING OF THE PROPOSED IC-DSTATCOM

The arrangement of the 3P3W EPDS with DC-DSTATCOM and IC-DSTATCOM are portrayed in Figures 1 and 2 respectively. The DC-DSTATCOM which covers of a balanced 3-phase supply, DSTATCOM, 3-phase non-linear load. Whereas The IC-DSTATCOM which consists of a balanced 3-phase supply, converter transformer DSTATCOM, three-phase non-linear load. The voltage source inverter (VSI) linked at PCC of EPDS is exposed in Figure 3. A customized technique of self-supported capacitor-based DC-DSTATCOM and IC-DSTATCOM are utilized as a compensator to diminish the PQ disputes. Switching signals for the IGBTs of the both compensators are engendered by the *icosϕ* control technique. The study's main goal is to pick the scrupulous structure by applying *icosϕ* control algorithm.

2.1. Innovations of the projected topology

The suggested topology over DC-DSTATCOM has a number of novelties. In this sub-section, the different aspects are considered for the comparison study. Among those the important contributions which are outlined:

- Reduction of the cost of system down time: The total output load current is dependent on converter transformer and VSC interfacing impedance, this reduces the IGBT's failure rate. Because of this, reducing the cost of system downtime will improve EPDS reliability.
- Lowered VSC's ranking: VSC reduces the amount of current it feeds due to converter transformer and VSC interfacing impedance therefore the rating of VSC is reduced.
- Flexible operation of inverter: AS VSC is connected through the converter transformer which consents to easy maintenance. It further enhances the system's adaptability.
- Increase in system efficiency: The system efficiency is increased due to matching impedance in between converter transformer and VSC interfacing impedance.

- Reduced DC link potential: The dc link potential rating of individual VSI of the IC-DSTATCOM is diminished approximately 10.30% from 749.9 to 680 V, as liked to classic VSI.
- Drop in THD of the input source current: The %THD are achieved from DC-DSTATCOM is 4.51 and 27.90 belongs to input and output currents respectively. While, the %THD are achieved from IC-DSTATCOM is 3.57 and 27.90 belongs to input and output currents respectively.

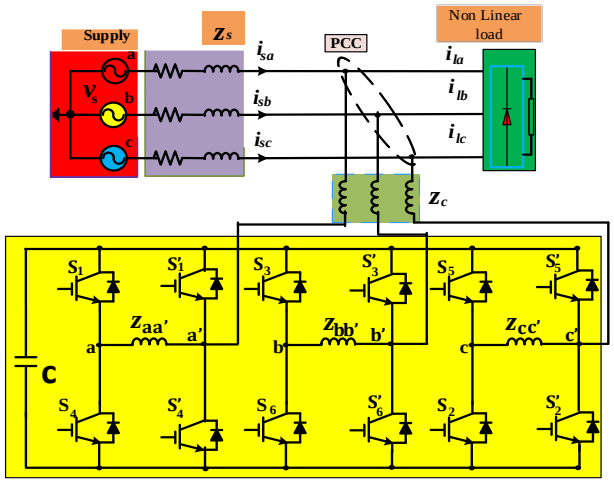

Figure 1. EPDS with DC-DSTATCOM

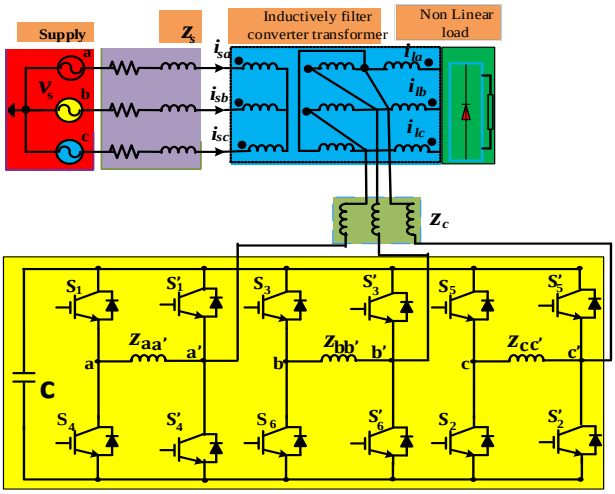

Figure 2. EPDS with IC-DSTATCOM

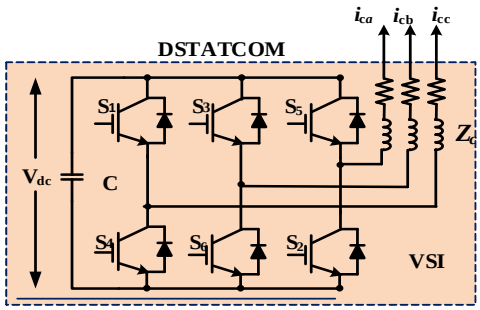

Figure 3. Two-level self-supported capacitor supported VSC based DSTATCOM

3. MODELLING AND DESIGN OF INDUCTIVE TRANSFORMER

The detailed winding structure of the projected IC-DSTATCOM was exposed in Figure 1. The projected IC-DSTATCOM arranges IFCT, DSTATCOM consisting VSC and non-linear load. The IFCT structure contains three winding through which DSTATCOM and non-linear load are connected. Among three windings, the primary winding (PW) with star connected wiring by grid, secondary side winding (SW) with star connected wiring by non-linear load, and the filtering winding (FW) with delta type wiring is connected by DSTATCOM. The special winding IFCT is to reach the balanced potential between grid, load, DSTATCOM. That is to say the PW harmonics are inaccessible. The detailed mathematical model of the IFCT and filtering mechanism are discussed in the later subsections. The voltage balance mathematical equation can be written as (1).

$$\begin{cases} N_1 \mathrm{i_{ap}} + N_2 \mathrm{i_{as}} + N_3 \mathrm{i_{af}} = 0 \\ N_1 \mathrm{i_{bp}} + N_2 \mathrm{i_{bs}} + N_3 \mathrm{i_{bf}} = 0 \\ N_1 \mathrm{i_{cp}} + N_2 \mathrm{i_{cs}} + N_3 \mathrm{i_{cf}} = 0 \end{cases} \quad (1)$$

According to Kirchhoff's current law (KCL), the current equations are written as (2).

$$\begin{cases} \mathrm{u_{abf}} = (i_{zb} - i_{za}) * Z_o \\ \mathrm{u_{bcf}} = (i_{zc} - i_{zb}) * Z_o \\ \mathrm{u_{caf}} = (i_{za} - i_{zc}) * Z_o \end{cases} \quad (2)$$

$$\begin{cases} \mathrm{i_{ap}} = \frac{u_{sa} - u_{apo}}{Z_{line}} \\ \mathrm{i_{bp}} = \frac{u_{sb} - u_{bpo}}{Z_{line}} \\ \mathrm{i_{cp}} = \frac{u_{sc} - u_{cpo}}{Z_{line}} \\ \mathrm{i_{as}} = i_{al} + i_{zal} \\ \mathrm{i_{bs}} = i_{bl} + i_{zbl} \\ \mathrm{i_{cs}} = i_{cl} + i_{zcl} \\ \mathrm{i_{ap}} + i_{bp} + i_{cp} = 0 \\ \mathrm{i_{as}} + i_{bs} + i_{cs} = 0 \\ \mathrm{i_{af}} + i_{bf} + i_{cf} = 0 \\ \mathrm{i_{af}} = i_{cf} + i_{cat} = i_{cf} + i_{ra} + i_{za} \\ \mathrm{i_{bf}} = i_{af} + i_{cbt} = i_{af} + i_{rb} + i_{zb} \\ \mathrm{i_{cf}} = i_{bf} + i_{cct} = i_{bf} + i_{rc} + i_{zc} \end{cases} \quad (3)$$

$$\begin{cases} \mathrm{u_{apo}} - \frac{\mathrm{N_1}}{\mathrm{N_3}} \mathrm{u_{abf}} = \mathrm{i_{ap}} \mathrm{z_p} - \frac{\mathrm{N_1}}{\mathrm{N_3}} \mathrm{i_{af}} \mathrm{z_f} \\ \mathrm{u_{bpo}} - \frac{\mathrm{N_1}}{\mathrm{N_3}} \mathrm{u_{bcf}} = \mathrm{i_{bp}} \mathrm{z_p} - \frac{\mathrm{N_1}}{\mathrm{N_3}} \mathrm{i_{bf}} \mathrm{z_f} \\ \mathrm{u_{cpo}} - \frac{\mathrm{N_1}}{\mathrm{N_3}} \mathrm{u_{caf}} = \mathrm{i_{cp}} \mathrm{z_p} - \frac{\mathrm{N_1}}{\mathrm{N_3}} \mathrm{i_{cf}} \mathrm{z_f} \end{cases} \quad (4)$$

According to the theory of multi-winding transformer, the voltage transfer equations are obtained in (4).

4. PROPOSED *ICOSϕ* CONTROL METHOD

The constructed control structure of the scheme is structured in Figure 4. The three-phase non-linear output load current is used to fed the reference input supply amperes which aims the healthier pf and current harmonics deduction. The gate signals are generated with the help of *icosϕ* controller for switches of inverter and owing to its rapid and robust dynamic response to both steady-state and transient responses, this technique was chosen. Figure 5 depicts the *icosϕ* control algorithm's internal control signal. The gate signals are generated in 4 stages for controlling the DC-DSTATCOM as well as IC-DSTATCOM: i) the base quantity of the 3-ϕ output load current i_L is figured by means of fourier block; ii) the method used to generate both the active and the reactive components of the load current is described; iii) following the topology, the active and reactive portion of output amperes are employed to breed the reference supply currents; and iv) the cumulation of active part and reactive part of output current served to hysteresis current controller (HCC), which feeds the switching pulses.

In terms of fundamental output current, i_{lap} can be stated as the active power component as (5).

$$\begin{bmatrix} i_{lap} \\ i_{lbp} \\ i_{lcp} \end{bmatrix} = \begin{bmatrix} Re(i_{la}) \\ Re(i_{lb}) \\ Re(i_{lc}) \end{bmatrix} = \begin{bmatrix} i_{la}cos\phi_{la} \\ i_{lb}cos\phi_{lb} \\ i_{lc}cos\phi_{lc} \end{bmatrix} \quad (5)$$

The weighted mean worth of the real active power module w_p

$$w_p = \left(\frac{i_{la}cos\phi_{la}+i_{lb}cos\phi_{lb}+i_{lc}cos\phi_{lc}}{3}\right) \quad (6)$$

The reactive power component can be stated.

$$\begin{bmatrix} i_{laq} \\ i_{lbq} \\ i_{lcq} \end{bmatrix} = \begin{bmatrix} Im(i_{la}) \\ Im(i_{lb}) \\ Im(i_{lc}) \end{bmatrix} = \begin{bmatrix} i_{la}sin\phi_{la} \\ i_{lb}sin\phi_{lb} \\ i_{lc}sin\phi_{lc} \end{bmatrix} \quad (7)$$

The weighted mean value of the reactive power module w_q.

$$w_q = \left(\frac{i_{la}sin\phi_{la}+i_{lb}sin\phi_{lb}+i_{lc}sin\phi_{lc}}{3}\right) \quad (8)$$

The error v_{de} is fed to the PI controller and its output can be stated as (9).

$$w_{dp} = k_{pdp}v_{de} + k_{idp}\int v_{de}dt \quad (9)$$

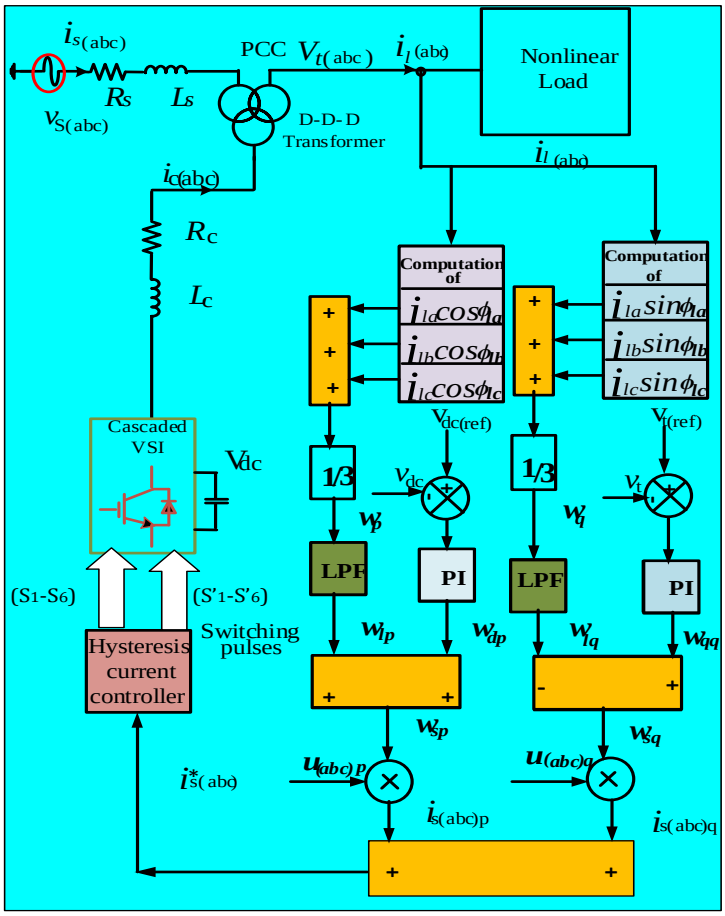

Figure 4. Switching signals generation for IC-DSTATCOM

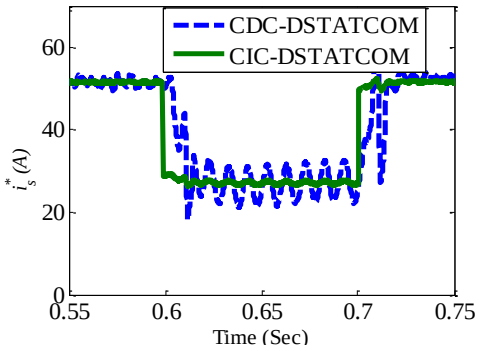

Figure 5. Inside control signal of the control technique

The mean value of active and reactive weighted modules is 'w_p', 'w_q'respectively. The' w_p', ' w_q' are the clustered weight and no assurance to give an adjusted value. These boundaries are overwhelmed by suggesting the LPF exposed in the Figure 4. These masses are handled through LPF and mitigate the larger order harmonics element. Thus, the tuned mass active element (w_{spt}) and reactive element (w_{sqt}) of the output current are attained. At last, the advised commanding scheme is directed to bring a filtered and adjusted mass. The adjusted mass is less disturbed with noise and hence become more stable and also fit for any disturbance occupied in the network, with which the PCC's compensator current can be immunized. The totaling of PI controller production and the weighted mean worth of the real active power element w_p offers the total active elements of the reference source input current.

$$w_{spt} = w_{dp} + w_{lp} \tag{10}$$

In the identical way, the entire reactive factors can be computed as (11).

$$w_{sqt} = w_{qq} - w_{lq} \tag{11}$$

A low frequency pass filter which cut of rate was 20.5 Hz applied for filtration of active and reactive weighting factor of output current. Instantaneous worth of active input currents i_{sp}, can be stated as (12).

$$\begin{bmatrix} i_{sap} \\ i_{sbp} \\ i_{scp} \end{bmatrix} = w_{spt} \begin{bmatrix} u_{ap} \\ u_{bp} \\ u_{cp} \end{bmatrix} \tag{12}$$

Instantaneous worth of reactive supply currents i_{sq}, can be stated as (13)

$$\begin{bmatrix} i_{saq} \\ i_{sbq} \\ i_{scq} \end{bmatrix} = w_{sqt} \begin{bmatrix} u_{aq} \\ u_{bq} \\ u_{cq} \end{bmatrix} \tag{13}$$

At last the reference input currents can be illustrated as (14)

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \begin{bmatrix} i_{sap} \\ i_{sbp} \\ i_{scp} \end{bmatrix} + \begin{bmatrix} i_{saq} \\ i_{sbq} \\ i_{scq} \end{bmatrix} \tag{14}$$

Both the actual source currents ($i_{sa,}i_{sb}, i_{sc}$) and the reference supply currents ($i_{sa}^*, i_{sb}^*, i_{sc}^*$) of the corresponding phases are matched, then current error signals are fed to the HCC. It is widely applied here for this reason: easier to develop and diminishes the hardware complications than other modulation controller. The following is the procedure to be followed:

when $i_{sa} < i_{sa}^*$, $s_1$is ON and s_4 is OFF (ii) when $i_{sa} > i_{sa}^*$, $s_1$is OFF and s_4 ON

5. SIMULATION OUTCOMES and ANALYSIS

The EPDS is fed by a sinusoidal balanced potential 230 V/phase with an input inductance 2 mH and an input resistance 0.5 Ω. The performance analysis of the both DC-DSTATCOM and IC-DSTATCOM are indicated in Table 1. The basic rating parameters and active with reactive power of IFCT is presented Tables 2 and 3. The constraints taken for the simulation of both DC-DSTATCOM and IC-DSTATCOM using *icosϕ* algorithm is given in the Table 4. Simulation outcomes are structured by MATLAB/Simulink computer software and the outcomes are justifying to pick the right technique for EPDS. The performance of IC-DSTATCOM for PQ betterment, equated with DC-DSTATCOM, is structured here in the following sub-sections.

Table 1. Performance parameter of DC-DSTATCOM and IC-DSTATCOM

Performance parameter	DSTATCOM at PCC	
	DC-DSTATCOM	IC-DSTATCOM
i_s(A), %THD	55.01, 4.51	53.67, 3.57
v_s (V), %THD	321.4, 2.23	321, 1.42
i_l (A), %THD	51.76, 27.90	51.34, 27.90
Power Factor	0.94	0.99

Table 2. Basic name plate rating parameters of the IFCT

	Grid side	Load side	Filtering side
Wiring scheme	Wye	Wye	Wye
Power and frequency	10 kV, 50 Hz	10 kV, 50 Hz	10 kV, 50 Hz
Voltage (ph-ph), R, and L	230 V, 0.002 (pu), 0.08 (pu)	230 V, 0.002 (pu), 0.08 (pu)	230 V, 0.002 (pu), 0.08(pu)
Magnetic resistance, inductance	500 Ω,500 Ω	500 Ω,500 Ω	500 Ω,500 Ω

Table 3. Measured active and reactive power of IFCT

Grid side	Active power	26 kW
	reactive power	1.388 kVAR
Load side	Active power	15 kW
	reactive power	1.388 kVAR
Filtering side	Active power	24 kW
	reactive power	570 VAR

Table 4. Simulation outline parameters

Symbol	Definition	Value
v_s	3- phase supply potential	230 V/phase
f_s	Frequency	50 Hz
R_s	input resistance	0.5 Ω
L_s	input inductance	2 mH
K_{pr}	AC P- controller	0.2
K_{ir}	AC Integral controller	1.1
v_{dc}	DC link potential	600 V
C_{dc}	Capacitor	2,000 µF
K_{pa}	DC P-controller	0.01
K_{ia}	DC Integral controller	0.05
R_c	VSC resistance	0.25 Ω
L_c	VSC inductance	1.5 mH

5.1. Simulation results of DC-DSTATCOM

The DC-DSTATCOM is avoiding output load current distortions with great THD to pass into the supply path and enlightening the pf. The proposed DC-DSTATCOM controller's effectiveness and feasibility have been demonstrated in various scenarios. It was verified in reaction to a step change of mean DC-link potential of VSC (681 to 750 V) at the time of 0.6 sec. The steady-state and transient reaction of VSI's current tracking features were showed in Figure 6(a) from up to down supply potential, supply current, output current, compensator current and DC-link potential.

Hence, DC-DSTATCOM can be improved power factor and diminished THD at source side. Later parallel compensation, the pf is progressed to 0.94 portrayed in Figures 6(b) and 6(c) and THD% 4.51 which portrayed in Figure 6(d). The output load current THD% 27.90 portrayed in Figure 6(e).

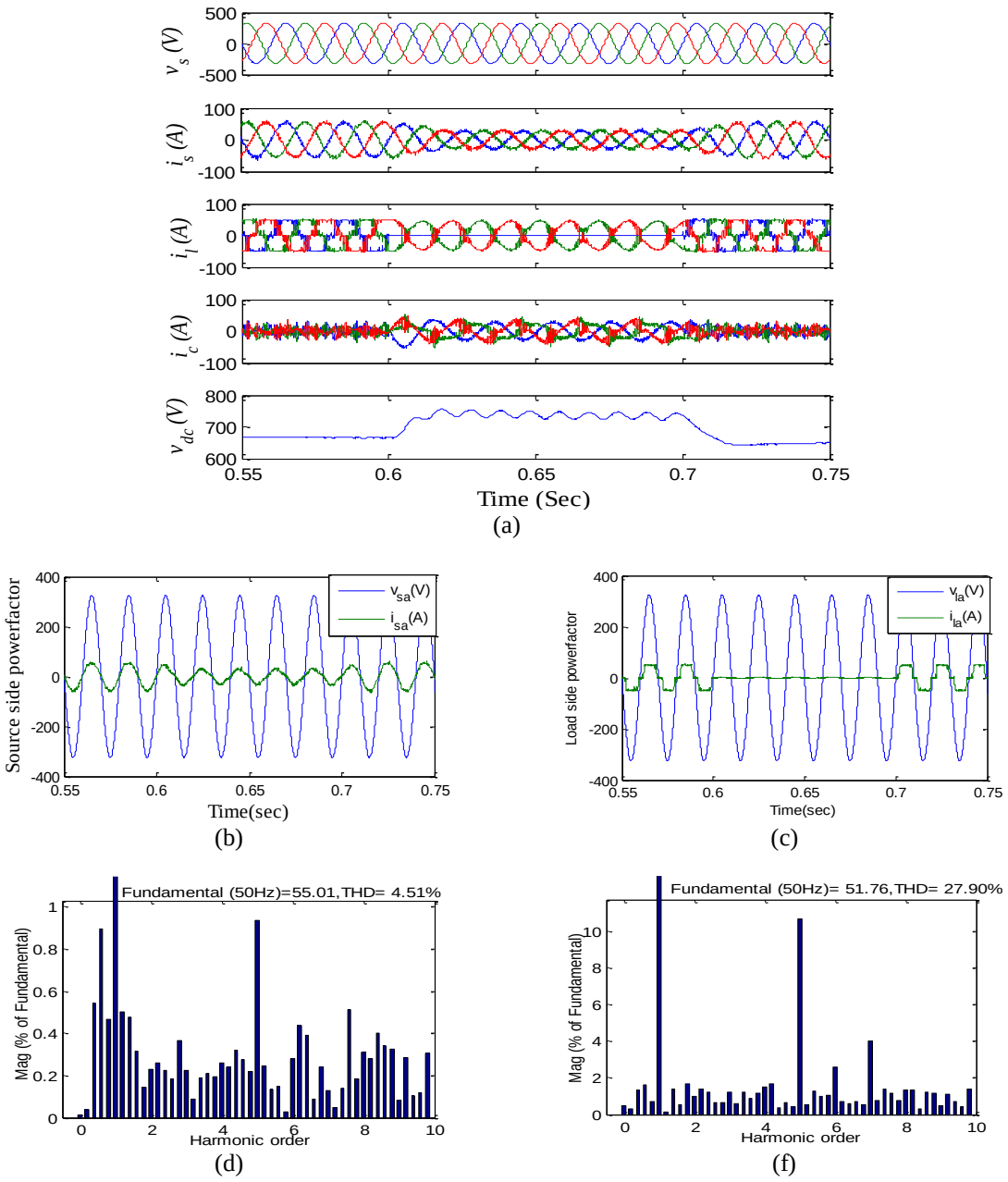

Figure. 6 represents the system performance (a) waveform of three phase input potential, supply current, output current, compensator current and DC-link potential with DC-DSTATCOM, (b) source side power factor with DC-DSTATCOM, (c) load side power factor with DC-DSTATCOM, (d) source current THD with DC-DSTATCOM, and (e) load current THD with DC-DSTATCOM

5.2. Simulation results of IC-DSTATCOM

The proposed IC-DSTATCOM controller's effectiveness and feasibility have been demonstrated in various scenarios. It was verified in reaction to a step variation of mean DC-link potential (600 to 680 V) at the time of 0.6 sec. The steady-state and transient reaction of IC- DSTATCOM characteristics were indicated in Figure 7(a). All the subplots are arranged in the order of up to down wise like supply potential, input supply current, output load current, compensator current, DC-link potential.

The proposed IC-DSTATCOM affords a healthy pf and supply current THD percentage. Later parallel compensation, the pf is reached to 0.99 portrayed in Figures 7(b) and 7(c) and THD% dropped to 3.57 depicted in Figure 7(d). The load output current THD% 27.90 is in Figure 7(e). The performance analysis of the both DC-DSTATCOM and IC-DSTATCOM are indicated in Table 1. The proposed IC-DSTATCOM filtered a greatly polluted supply current harmonics of the EPDS as compared to other.

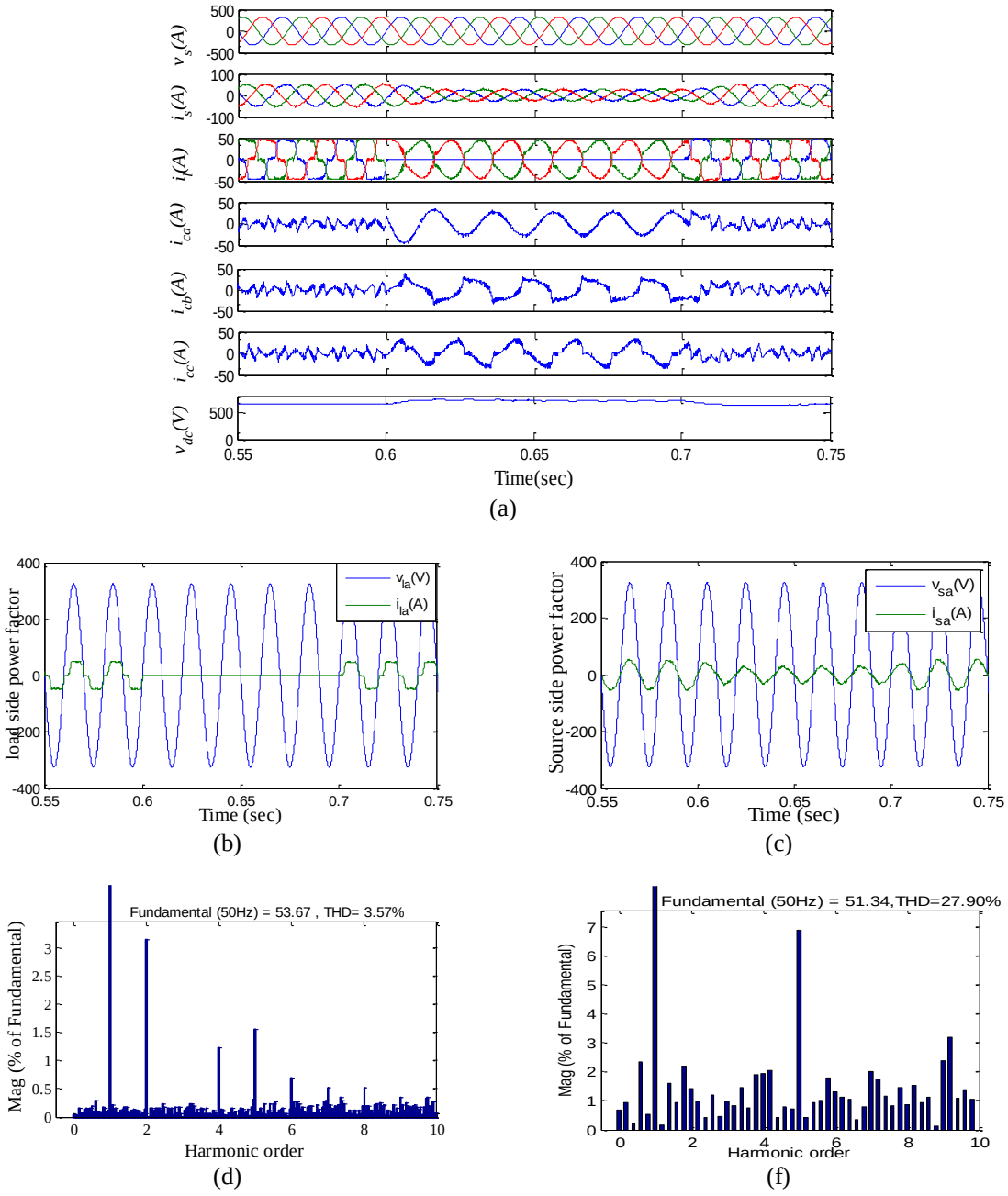

Figure 7. represents the system performance (a) waveform of three phase input potential, supply current, output current, compensator current, DC-link potential with IC-DSTATCOM, (b) source side power factor with IC-DSTATCOM, (c) Load side power factor with IC-DSTATCOM, (d) source current THD with IC-DSTATCOM, and (e) load current THD with IC-DSTATCOM

5.3. Analysis and calculation of kVA rating, derating factor, harmonic compensation ratio, distortion index, form factor, ripple factor, harmonic factor and C-message weights [22]

5.3.1. Analysis of kVA rating

This is calculated by considering the dc link potential and filter current. The volt ampere (kVA) rating can be obtained as:

$$\text{VA rating}=\sqrt{3} * \frac{v_{dc}}{\sqrt{2}} * \frac{I_f}{\sqrt{2}}$$

where v_{dc} the DC is link voltage of distributed static indeterminacy (DSI) and I_f is the inverter current.

kVA rating of DC-DSTATCOM = $\sqrt{3} * \frac{535}{\sqrt{2}} * \frac{12.5}{\sqrt{2}} = 5.794\ kVA$

kVA rating of IC-DSTATCOM = $\sqrt{3} * \frac{535}{\sqrt{2}} * \frac{10.5}{\sqrt{2}} = 4.867\ kVA$

5.3.2. Calculation of derating factor (DF)

It depends on efficiency of the system

DF= 1-efficiency $\quad Efficiency = \frac{output\ power}{input\ power} * 100$

kVA rating of DC-DSTATCOM = 5.79 kVA, power factor cosϕ = 0.97
kW output of the CDC-DSTATCOM = kVA cosϕ = 5.794*0.97 = 5.62 kW*
Power losses of CDC-DSTATCOM = $3I_f^2 * R_c$
I_f *is the inverter current= 12.5 A,* R_c*= 0.25 Ω*
$3I_f^2 * R_c$ *= 3*$12.5^2 * 0.25$ *= 117.18 W*
$Power\ input = output\ power + losses = 5620 + 117.18 = 5737.18\ W = 5.737\ Kw$
DC-DSTATCOM = $\frac{5.62}{5.737} * 100$ *= 97.65%*
DF of DC-DSTATCOM = 1- 0.97 = 0.03

kVA rating of IC-DSTATCOM = 4.867 kVA, power factor cosϕ = 0.99
kW output of the CDC-DSTATCOM = kVA cosϕ, 4.867*0.99 = 4.81 kW*
I_f *is the inverter current= 10.5 A,* R_c*= 0.25 Ω*
$3I_f^2 * R_c$ *= 3*$10.5^2 * 0.25$ *= 82.68 W*
$Power\ input = output\ power + losses = 4810 + 82.68 = 4892.68\ W = 4.89\ kW$
IC-DSTATCOM = $\frac{4.81}{4.89} * 100$ *= 98.36%*
DF of IC-DSTATCOM = 1- 0.983 = 0.017

5.3.3. Harmonic compensation ratio (HCR)

The HCR of DC-DSTATCOM is calculated by using %THD values before and after compensation

HCR= $\frac{\text{THD\% after compensation}}{\text{THD\% before compensation}} = \frac{4.05}{27.90} = 0.145$

Similarly, the HCR of IC-DSTATCOM is given as

HCR= $\frac{THD\%\ after\ compensation}{\text{THD\% before compensation}} = \frac{3.14}{27.90} = 0.112$

5.3.4. Distortion index (DIN)

Taylor series expansion for small ranks of harmonics is below = THD (1- $\frac{1}{2}$ (THD))

DIN for DC-DSTATCOM = 4.05(1- $\frac{1}{2}$ 4.05) = -4.15
DIN for IC-DSTATCOM = 3.14 (1- $\frac{1}{2}$ 3.14) = -1.78

5.3.5. Form factor (FF)

The form factor is defined as FF = $\frac{I_{rms}}{I_{avg}}$

FF for DC-DSTATCOM =

I_{rms}= 39.21 A $\quad I_{rms} = \frac{\pi}{2\sqrt{2}} I_{avg}$
I_{avg}=35.30A $\quad$ FF= $\frac{39.21}{35.30}$= 1.11

FF for IC-DSTATCOM =

I_{rms}= 37.9 A $\quad I_{avg}$=34.12A $\quad$ FF= $\frac{37.9}{34.12}$= 1.11

5.3.6. Ripple factor (RF)

It is calculated by using formfactor

RF for DC-DSTATCOM = $\sqrt{(FF^2)-1}$= $\sqrt{(1.11^2)-1}$ = 0.48
RF for IC-DSTATCOM = $\sqrt{(FF^2)-1}$= $\sqrt{(1.11^2)-1}$ = 0.48

5.3.7. Harmonic factor (HF)

It is the ratio between harmonic components to the fundamental component of RMS current

The HF of the h_{th} harmonic, $HF_h = \frac{I_{rms}^{(h)}}{I_{rms}^{(1)}}$
HF for DC-DSTATCOM = $\frac{39.21}{53.25} = 0.736$
HF for IC-DSTATCOM= $\frac{37.9}{52.42}$ = 0.72

5.3.8. C-Message weights

It is measured by harmonic component and fundamental component of RMS current

The C-Message weighted index is C= $\frac{\sqrt{\sum_{i=1}^{\infty}(C_i I^{(i)})^2}}{I_{rms}}$
C-Message weights for DC-DSTATCOM = $\frac{39.21^2}{53.25^2}$ = 0.5
C-Message weights for IC-DSTATCOM = $\frac{37.9^2}{52.42^2}$ = 0.5

Comparative study on kVA rating, DF, HCR, DIN, FF, RF, HF and C-Message weight of DC-DSTATCOM and IC-DSTATCOM Is structured in Table 5. Bar chart for the indexed parameters is structured in Figure 8.

Table 5. Comparative study on kVA rating, DF, HCR, DIN, FF, RF, HF and C-Message weight of DC-DSTATCOM and IC-DSTATCOM

Sl. No.	Types of configurations	Analysis of KVA rating	DF	HCR	DIN	FF	RF	HF	C-message weight
1	DC-DSTATCOM	5.794	0.03	0.145	-4.15	1.11	0.48	0.736	0.5
2	IC-DSTATCOM	4.867	0.017	0.112	-1.78	1.11	0.48	0.72	0.5

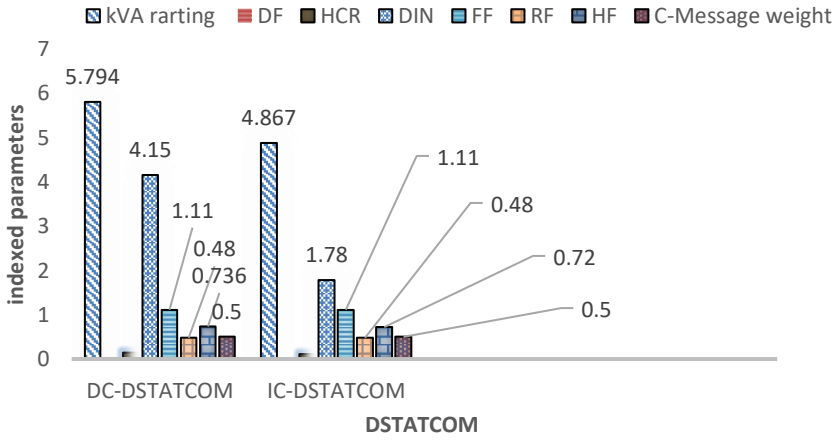

Figure 8. Bar chart for the indexed parameters

6. CONCLUSION

The present study is dealt on both DC-DSTATCOM and IC-DSTATCOM topologies for Improvements of PQ. In the proposed configuration, the total output power is provided due to proper coordination of coupled transformer and interfacing impedance of VSC. The following objectives are achieved below: i) Growth in reliability, well consumption of power, less band width necessity for inverter

and reduce in filter dimensions are achieved, ii) The diminished component stress, effortless maintenance, modularity and interleaving are deliberated as the advantages of projected topology, and iii) Apart from these, the effectiveness in terms of harmonics curtailment, improvement in pf, load potential regulation with different PQ parameter indices are presented and compared as per benchmark measure of IEEE-2030-7-2017 and IEC- 61000-1 grid code. The proposed topology can be utilized for multi-inverter, renewable sources and new intelligent controller for further.

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BIOGRAPHIES OF AUTHORS

Praveen Kumar Yadav Kundala received the B.Tech in Electrical and Electronics Engineering from JNTU Kakinada, India in 2009. He received the M.Tech in Power Industrial Drives from BPUT, Odisha, India in 2013. He is currently working as an Asst. Professor in Electrical and Electronics Engineering Dept. of LIET Vizianagaram. His area of research interest includes power quality, design and modelling of custom power devices. He can be contacted at Praveen263@gmail.com.

Mrutyunjaya Mangaraj received the B.Tech (Hons.) in Electrical Engineering from Berhampur University, India in 2006. He received the M.Tech in Power System Engineering from VSSUT, Burla, India in 2010. He obtained Ph.D. from National Institute of Technology, Rourkela in 2018. Currently continuing as a Professor in the Department of Electrical & Electronics Engineering at LIET Vizianagaram. He is associated as Principal Investigator in SERB sponsored project under the SRG grant. His area of research interest includes power system economics, design and modelling of d-FACTS devices with embedded controller, and soft computing techniques. He can be contacted at mmangaraj.ee@gmail.com.

Suresh Kumar Sudabattula received the B.Tech. And M.Tech. Degree in electrical and Electronics Engineering from JNTU, Kakinada, in 2007 and 2011, respectively. He obtained his Ph.D. degree from the Vellore Institute of Technology, Vellore, in 2018. Since 2017, he has been continuing as an Associate Professor in the School of Electronics and Electrical Engineering, Lovely Professional University, Punjab, India. His research interests include distributed generation, electric vehicles, and power system optimization, power electronics applications in power system. He can be contacted at suresh.21628@lpu.co.in.