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Reconfigurable negative bit line collapsed supply write-assist for 9T-ST static random access memory cell

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ABSTRACT

This paper presents a reconfigurable negative bit line collapsed supply (RNBLCS) write driver circuit for the 9T Schmitt trigger-based static random-access memory (SRAM) cell (9T-ST), significantly improving write performance for real-time memory applications. In deep sub-micron technology, increasing device parameter deviations significantly reduce SRAM cells' write-ability. The proposed RNBLCS write-assist driver for 9T-ST SRAM cell has 0.84×, 0.48×, 0.27× optimized write access delay and 1.05×, 1.08×, 1.19× improvement in write static noise margin (WSNM), 1.05×, 1.13×, and 1.39× improvement in write margin (WM), 0.96×, 0.89× and 0.72× minimum write trip-point (WTP) from transient-negative bit line (Tran-NBL), capacitive charge sharing (CCS), and conventional write circuits respectively. The proposed RNBLCS is functionally verified using a synopsys custom compiler with a 16 nm BSIM4 model card for bulk complementary metal-oxide semiconductor (CMOS).

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1. INTRODUCTION

For many years, energy-efficient and high-speed memory design has been a significant research focus in academia and industry. High energy efficiency and speed are required in a wide range of applications, including portable electronics and on-chip memories. Especially in military and aerospace applications accurate memory operations are expected to be performed under the availability of limited resources and temperature conditions. Low power and high speed memory operations are most important requirements for such applications [1].

For example, capacitive charge sharing collapsed supply is a write-assist driver technique for lowering energy usage by altering the system operating voltage across a wide range based on performance requirements. The static random-access memory (SRAM) cell is tested using cell characteristics and stability analysis in several operation modes. Using Monte Carlo (MC) simulation [2], the properties of ST-inverters are discovered, and the importance of constructing durable memory cells is observed. A stability analysis reveals the constraints of a stable 10T-ST SRAM cell. As a result, this research offers a 9T-ST SRAM cell structure derived from the 10T-ST SRAM cell. This adjustment has improved read-stability and hold-stability by 13% and 15%, respectively. The write-ability improvement of memory cells is a significant concern in this paper, besides read and hold stability, which was improved by proper cell design. Write-ability can be improved by modifying the memory architecture with assist circuits [3], [4].

This paper is written in the following manner: section 2 describes the capacitive charge sharing (CCS) [5] and Tran-NBL circuits that assist [6] in increasing the write-ability. The proposed write-assist driver circuit design for the 9T-ST SRAM cell is presented in section 3. Section 4 contains a statistical simulation-based analysis of the proposed work. Finally, section 5 concludes the paper by providing a summary.

2. CONVENTIONAL WRITE-ASSIST CIRCUITS TO IMPROVE WRITE-ABILITY

This section gives a brief overview and design process of conventional write-assist circuits to improve write-ability. 9T-ST SRAM cell is thermally stabile cell with high hold stability [7]. So 9T-ST SRAM cell is considered as reference SRAM cell to test the write ability improvement, during assist circuits are included.

2.1. Capacitive charge sharing write-assist circuit

As shown in Figure 1(a), the capacitive charge Sharing write-assist circuit is designed to improve write-ability. The 9T SRAM cell configuration eliminates write half-select failures and read failures for robust sub-threshold operations. Figure 1(b) shows that memory cells have enough cell stability at high voltage levels to hold cell data correctly when cell supply voltage (V_{CS}) is kept at high level voltage (V_{DD}) in Phase-1 for inactive WE. After WE assertion, P1 is turned off, and N1 is slightly conducted, so the charge across the source capacitor (CS) is discharged to another capacitor (CBOOST) through N1, as shown in Figure 1(c); this collapsed voltage (V_{CS} from V_{DD} to V_{COL}) can drive and reduce the memory cell's hold-stability as shown in Figure 2.

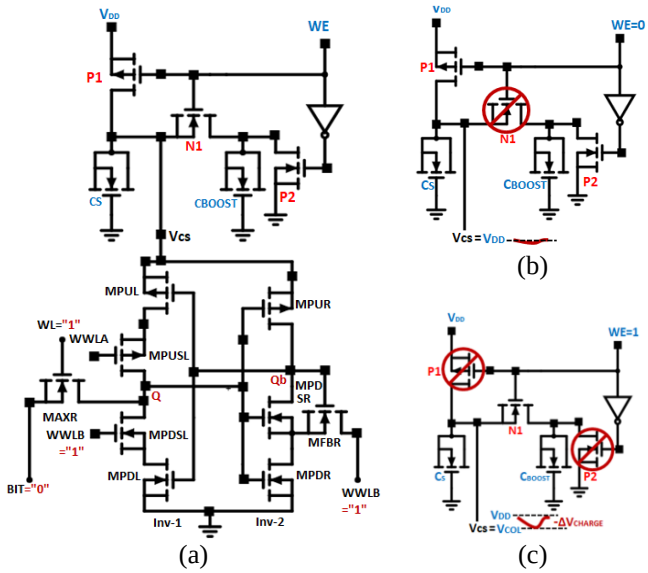


Figure 1. Capacitive charge sharing operation (a) CCS write-assist circuit for fast write accessing, (b) cell supply voltage in phase-1, when the write operation is not initiated, and (c) cell supply voltage down due to charge sharing in phase-2 when the writing process is initiated

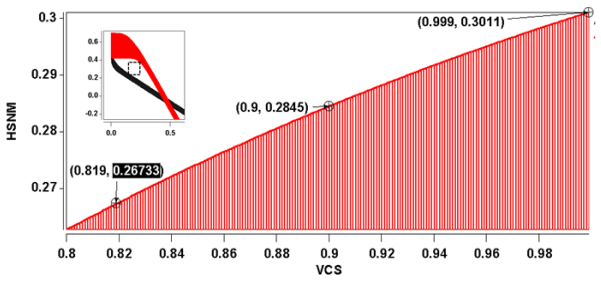
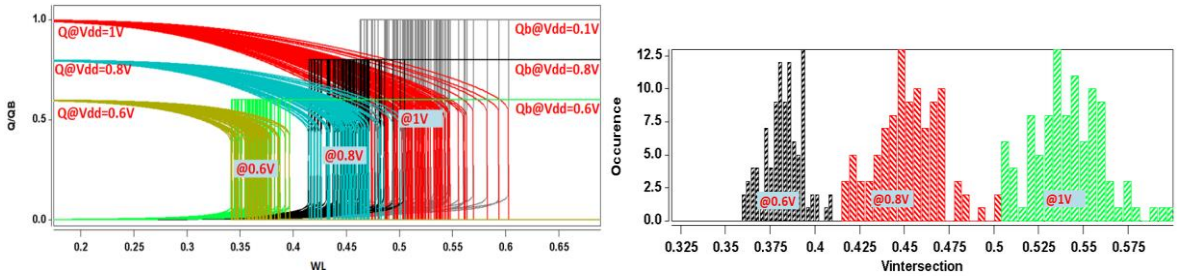


Figure 2. The plot of deteriorating hold stability for scaling the supply voltage

As the supply voltage of the cell drops, cell stability degrades, as indicated by the hold static noise margin (HSNM) stability parameter [8]. HSNM is a design parameter, which is extracted from butterfly curves of the cell. For example, when V_{CS} is scaled down, the HSNM of the cell degrades, as shown in Figure 2.

As shown in Figure 3(a), the Q-node of the memory cell is tripped at a swept word line (WL) voltage range of 0.46 to 0.61 V for a supply voltage V_{DD} of 1 V. The mean write trip points (WTP) levels are decreased with scaling the supply voltage, which indicates scaling the supply voltage makes the cell unstable and quickly accepts the changes in bit (BIT) and bit bar (BITB) lines. So, the Q-node of a memory cell is tripped at a sweep WL voltage range of 0.33 to 0.39 V for a scaled supply voltage V_{DD} of 0.6 V. So write-ability is improved by scaling the SRAM cell's supply voltage, which is done by the CCS write-assist circuit [5]. The WTP voltage occurrence levels are plotted using Monte Carlo simulation, and it was observed that all strong cell samples with high V_{DD} occurred on the right side (at maximum trip voltage levels). On the other hand, all weak cell samples with scaled V_{DD} occurred on the left side (at minimum trip voltage levels), as shown in Figure 3(b).



(a) (b)

Figure 3. Monte Carlo simulation for write operation (a) write-0 at VTP levels for different V_{CS} and (b) write trip point levels occurrence for different V_{CS}

2.2. Tran-negative BIT line (T-NBL) write-assist circuit

Tran-NBL write-assist circuit, shown in Figure 4(a), can improve the write performance with the help of two charging capacitors (C_{RBOOST} and C_{LBOOST}). One end of these capacitors is connected to the BIT line and write word line-B (WWLB) of the 9T SRAM cell, and the opposite end of the capacitors is connected to the control input 'BIT_EN', as shown in Figures 4(b) and (c) [5]. Figure 4(d) depicts the timing diagram for the circuit functioning. In a conventional write operation, the active NSEL signal turns both pass-transistors (N1/P1, N2/P2) 'ON' for the whole duration of the WL pulse and BIT, BITB is connected to ground and V_{DD}. Here, 'NSEL' is used for column selection. The NSEL and BIT EN signals are asserted together with the WL pulse in Tran-NBL, but they are de-asserted halfway through the WL. The pass transistors (N1/P1 and N2/P2) are turned off, leaving BIT and BITB lines floating at the ground and V_{DD}, respectively. Due to capacitive coupling action via capacitors (CLBOOST and CRBOOST), the negative transition of BIT_EN produces the bit-line under-shoot (BIT or BITB). Because the floating BIT line at the '0' level generates a momentary negative sudden change voltage on the bit-lines (BIT or BITB). The timing diagram for the write-'0' operation is shown in Figure 4(d). The Tran-NBL write driver circuit generates a negative voltage at the bit line to increase the strength of the accessing transistor (MAXR) to improve the write access speed [4].

The strength of the negative bit voltage depends on selecting boost capacitors CLBOOST and CRBOOST as shown in Figure 4(d). Small range capacitors need a small silicon area to fabricate. Such a small range boost capacitor (CLBOOST=110 fF) can generate a small negative bit voltage of 110 mV, observed in Figure 4(d) [6]. The transient negative voltage causes a temporary rise in the access transistor's (MAXR) discharging current, making the Q-node voltage (VQ) pull-down easier. The cross-coupled inverter pairs latch and settle with write data when VQ falls below the trip-point.

During the write-'1' operation, the column select control input word line-A (WWLA) remains "0", the driver circuit drives BL to "1", and the word line is enabled. As the WWLB is changed to "0" to disconnect the path from the V_{DD} power source by turning off MPDSL, the Q-node storing data "0" is power-gated, which helps raise the voltage at Q-node. Furthermore, the ST inverter's trip voltage is lower than that of a conventional inverter because the ST inverter's feedback mechanism is decreased with negative VWLB voltage, as shown in Table 1. The turned-on MAXR drives the power-gated Q-node to "1", and the ST inverter is switched. After the data in Qb-node is flipped, the column selects WWLB is reset to '1' [7].

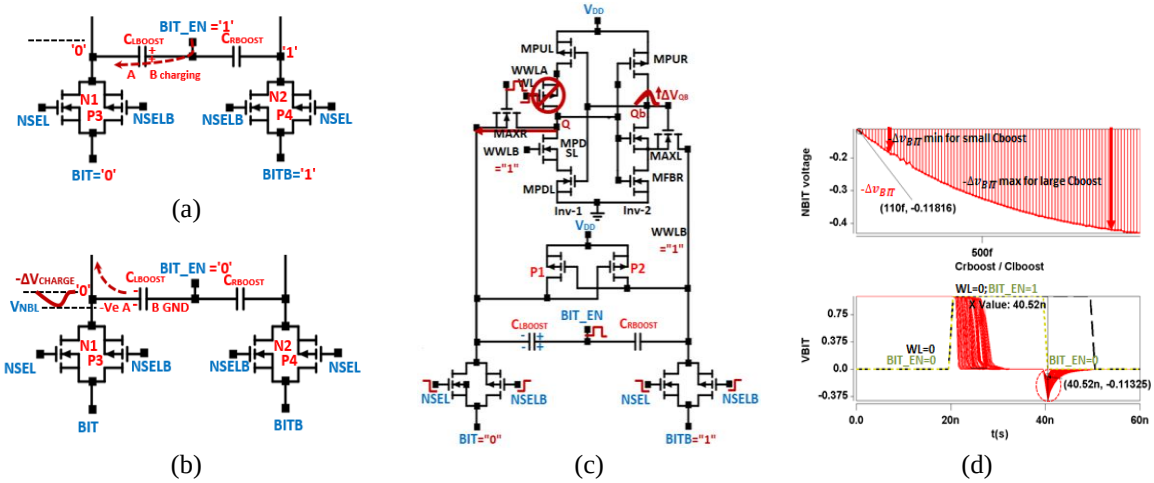


Figure 4. Write operation using T-NBL (a) capacitor charging mode through active BIT_EN, (b) negative BIT enable mode upon inactive BIT_EN, (c) Tran-NBL write driver circuit for fast write accessing (write-0), and (d) the timing diagram for the circuit operation of generating a negative BIT line for the change of WL, BIT_EN

Table 1. Minimizing trip voltage levels using column select control voltage V_{WWLB}, which are observed from the voltage transfer characteristics of ST inverter

V_{WWLB}	Feedback strength	Strength of M_{FBR}	VTP
V_{DD}	Strong	Very weak	593 mV
Ground	Very Weak	Strong	414 mV
-ve	Zero	Very Strong	353 mV

3. PROPOSED WRITE-ASSIST CIRCUIT DESIGN FOR 9T-ST SRAM CELL

A reconfigurable negative bit line collapsed supply (RNBLCS) write-assist circuit is proposed to improve the write performance (i.e., improve the write accessing speed, Write-ability) as shown in Figure 5. As shown in Figure 6(a), the boost capacitor is not adequately selected, so, a write '0' failure is observed. Write failure is overcome in the second case with the proper selection of boost capacitors during write '0' as shown in Figure 6(b).

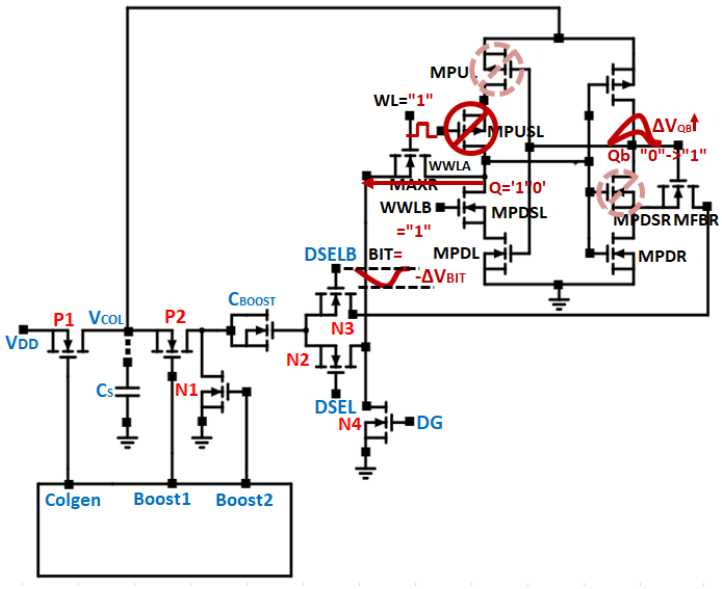


Figure 5. 9T-ST SRAM cell with RNBLCS write-assist circuit

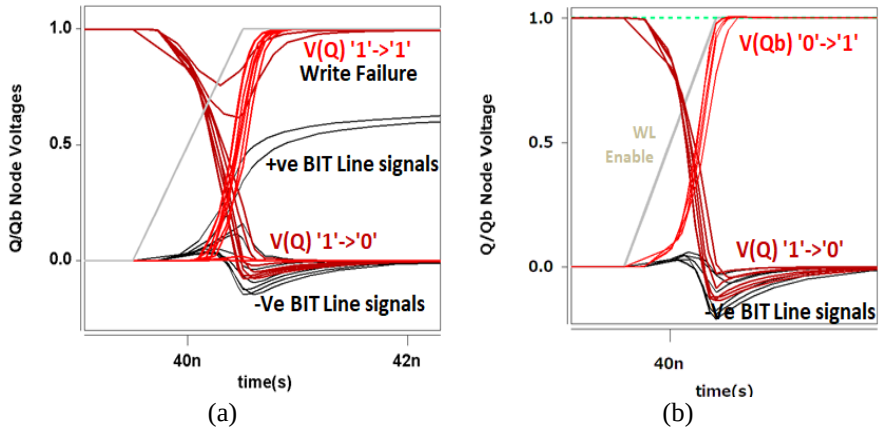


Figure 6. Write operation through transient response (a) occurring write failure for assist circuit design with minimum Cboost selection (<23fF) and (b) proper assist circuit design with no write failure

The write operation is carried out by the proposed assist circuit in three phases, i) no-Assist phase, ii) charge sharing or supply collapse phase, and iii) negative BIT line enable phase. In the no-Assist phase, P1 is turned ON using control signals (Colgen, Boost1, and Boost2) and corresponding timing response is shown in Figure 7. So, conducting P1 can fully charge the source capacitor (Cs) to the maximum level of V_{DD}, as shown in Figure 8(a). Next, when the write mode of operation is initiated upon active write enable, the capacitive charge sharing process is started from the source capacitor to the boost capacitor (CBOOST) through conducting P2 in the second phase. So, boost capacitor left plate (CBOOSTL) is accumulated with a positive charge, as shown in Figure 8(b).

Finally, in the negative BIT line enable phase as a third phase, the boost capacitor left plate is grounded by conducting N1suddenly by the boost2 signal. The capacitor does not allow sudden changes in voltage, so the right plate of the boost capacitor generates a negative voltage peak, which is directly transferred to the BIT/BITB line through N2/N3, as shown in Figure 8(c) and corresponding timing response is shown in Figure 7. The RNBLCS write-assist circuit pulls supply voltage down (V_{DD} to V_{COL}) to reduce the stability of the memory cell. It also generates negative BIT/BITB line voltage to increase the strength of the access transistor (MAXR/MAXL). As a result, RNBLCS can outperform CCS and Tran-NBL assist circuits in terms of write-ability [9].

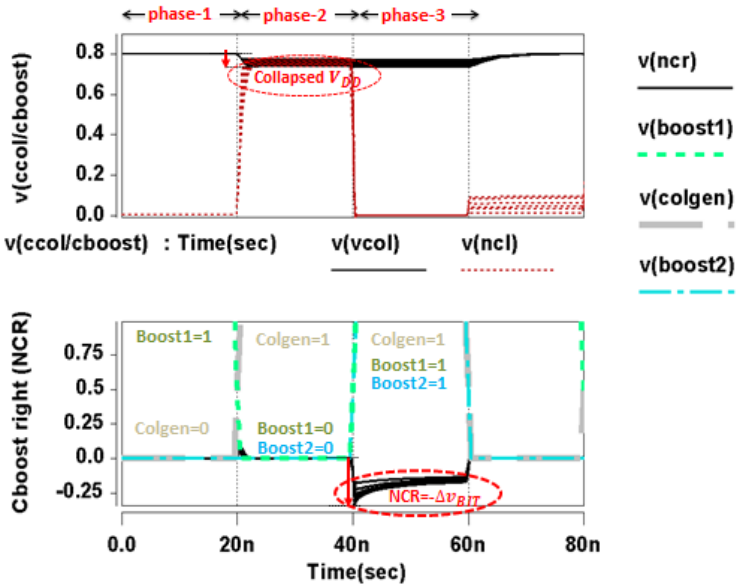


Figure 7. Negative BIT line voltage and collapsed supply voltage generation using 3 phase operation by proposed RNBLCS write-assist scheme

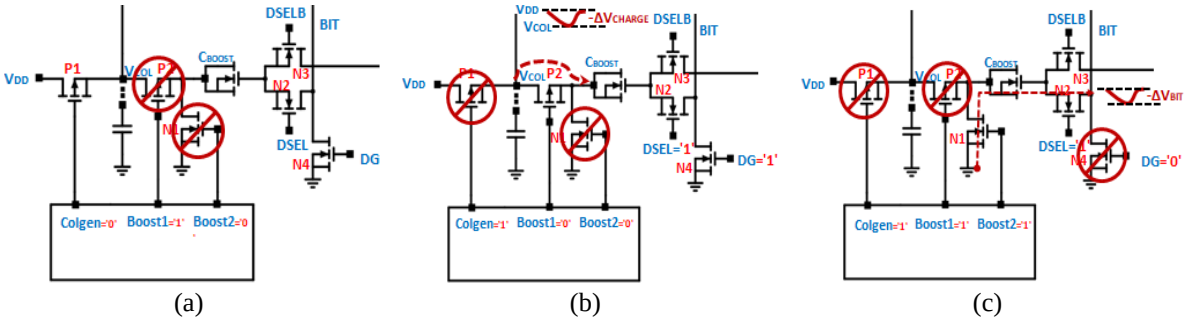


Figure 8. RNBLCS write assist operation through different phases (a) assist beginning phase, (b) charge sharing or supply collapse phase, and (c) negative BIT line enable phase

4. RESULTS AND DISCUSSION

The main concentration of this work is on improving write performance of memory. In this section write performance of memory cell is defined using following parameters. The discussion is carried as write operation using RNBLCS write-assist scheme is more efficient when compared to other assist schemes.

4.1. Write accessing delay

As shown in Figures 9(a) to (d), the conventional write driver circuit, existing write-assist circuit and proposed RNBLCS circuit simultaneously perform write-'1' operations to the 9T-ST SRAM cell [8], [10]. After WL is enabled, the write access time [11] is calculated as the time it takes for one of the storage node voltages (initially at '0') to reach 90% of V_{DD} [12]. The maximum write delay for 1,000 memory samples is plotted and compared. This comparison write delay of the proposed assist circuit is 0.84×, 0.48×, 0.27× times lower than Tran-NBL, CCS, and conventional write operations.

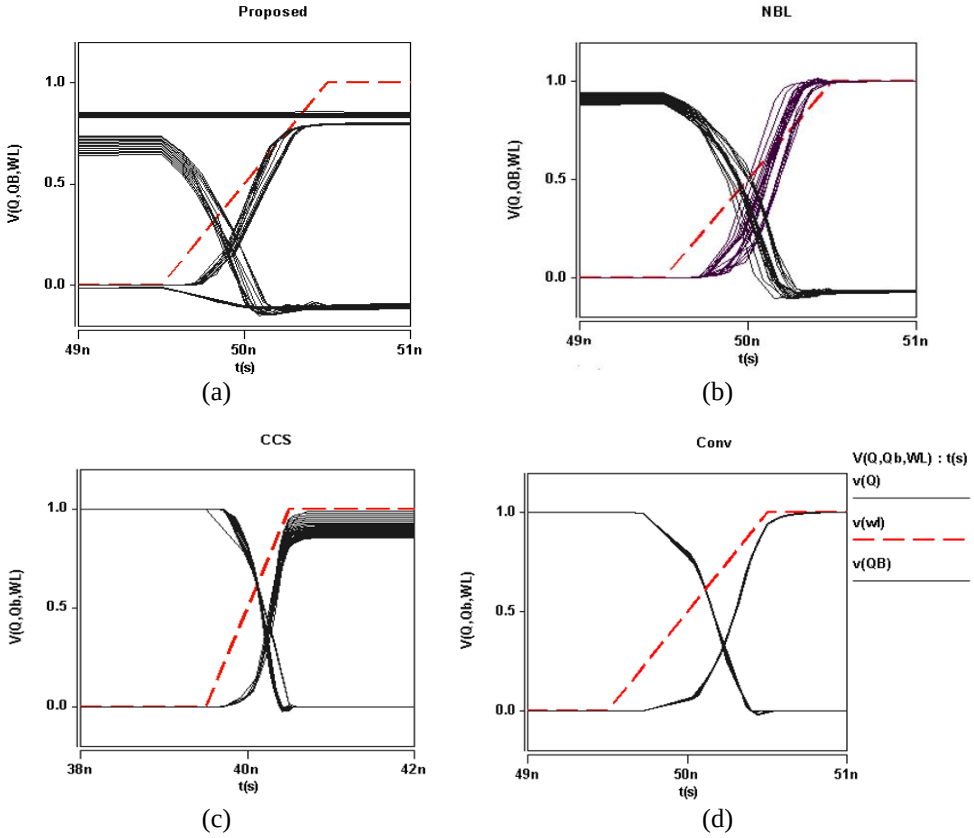


Figure 9. Capacitive sweep write accessing delay calculation (a) proposed, (b) NBL, (c) CCS, and (d) conventional write

4.2. Write static noise margin (WSNM)

WSNM indicates the write-ability of the cell, which is used as a performance metric during write operations. WSNM is calculated through butterfly curves, a combination of read and write voltage transfer curves. The read VTC is a plot of Qb-node voltage (VQb) versus Qb-node voltage (VQb) with BL, BLB WL are biased at V_{DD}. The write VTC is obtained by sweeping the voltage at the storage Q-node with BL and WL biased at V_{DD}, and BLB biased at the ground while plotting the node voltage at Qb-node [9], [13]–[18]. The width of the pull-up transistor is considered a Gaussian distribution function to perform Monte Carlo simulations to observe the effect of Write-ability due to the pull-up ratio (PR) variation. The maximum WSNM for 1000 memory samples is plotted and compared among conventional write driver circuits, existing write-assist circuits, and proposed RNBLCS circuits, as shown in Figure 10 [19]–[21].

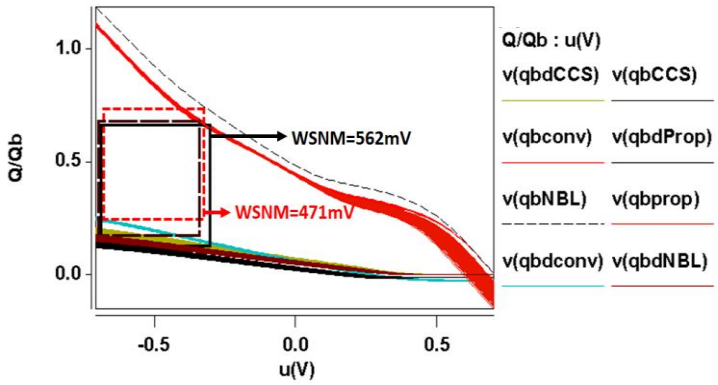
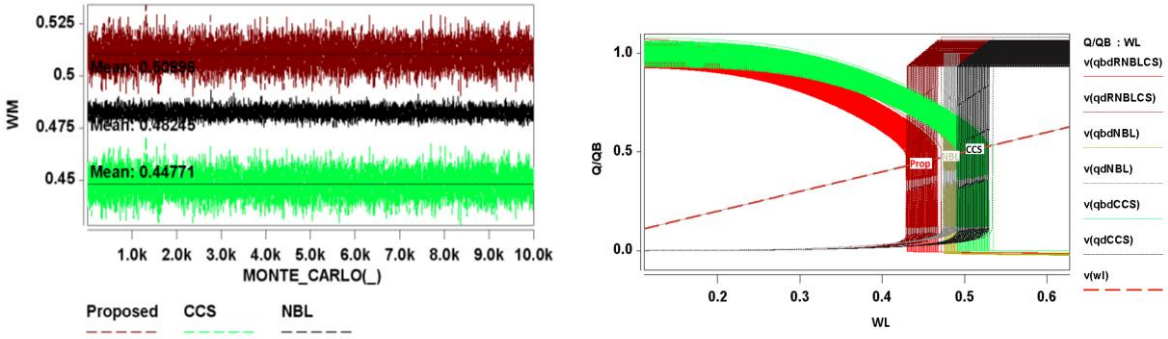


Figure 10. WSNM calculation through butterfly curves (DC transfer characteristics)

4.3. Write margin (WM) and write trip-point-voltage

WM is a metric used to characterize Write-ability, and it can be measured using the word-line sweep method [11]. Data is applied to the bit lines to measure WM, and then the word line (WL) is swept from 0V to V_{DD} to simulate an actual write process. The voltage differential between V_{DD} and WL when memory nodes (Q and Qb) update their data with write data during the write operation is known as the WM [12], [22]–[25].

WM occurrence levels are plotted using a Monte Carlo simulation in Figure 11(a). The proposed assist circuit offers 1.05× and 1.13× higher write margins than Tran-NBL and CCS, respectively, which is evident from the mean of WM calculation in Figure 11(a). WTP is identified as the sweep voltage level of WL at which memory nodes (Q and Qb) update their data with write data during the write operation. Figure 11(b) Illustrates the WTP of SRAM 10K cell samples with different write driver circuits under MC simulation and observed as the proposed Assist circuit offers 0.96× and 0.89× smaller WTP from Tran-NBL and CCS.



(a) (b)

Figure 11. MC simulation of (a) the WM for different write driver circuits and (b) WTP driver circuits

4.4. Write power

Average write power (using write-‘0' and write-‘1' power) is calculated for write-assist circuits, and comparison results are shown in Figure 12 [15]. The proposed 9T-ST SRAM with proposed RNBLCS, 20 nm HP model, has 24%,13%, and 43% and 16 nm HP model has 29%, 9%, and 36% power saving than Tran-NBL, CCS, and conventional write circuits. Cell leakage during write operations is reduced because of the collapsed power supply in CCS and the proposed RNBLCS. The ST-based SRAM cell's characteristics, which feature dual-threshold, save write power even more.

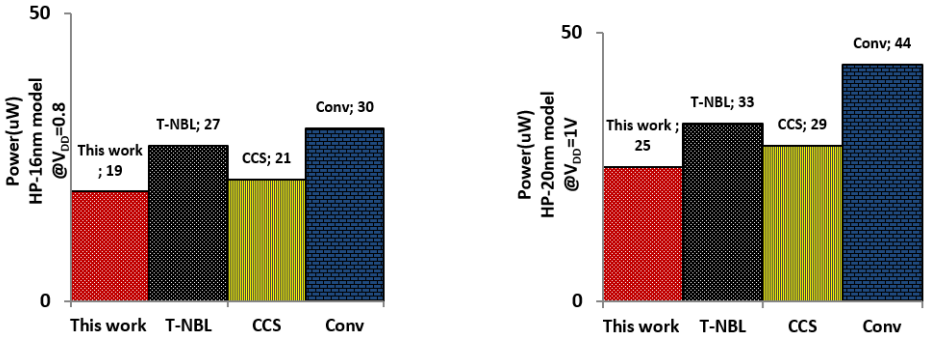


Figure 12. Comparison of write power among assist circuits during a write operation

5. CONCLUSION

The 9T SRAM cell configuration eliminates write half-select failures and read failures for robust sub-threshold operation; write-ability improvement constraints are demonstrated in this paper. A significant improvement in write performance is observed with the 9T-ST SRAM cell with reconfigurable negative bit line collapsed supply write-assist technique. The proposed ST bit cell achieves a higher read SNM (1.56×) than the conventional 6T cell (V_{DD}=400 mV). In addition, the proposed 'RNBLCS' completes a higher Write Margin (1.1×), WSNM (1.19×), and lower write delay (0.27×) compared to the convention write driver circuit. The proposed 'RNBLCS' also achieves lower write power (0.57× for 20 nm) (0.64× for 16 nm).

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