

Design and analysis of dual-mode numerically controlled oscillators based controlled oscillator frequency modulation

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ABSTRACT

In this paper, the design and analysis of dual-mode numerically controlled oscillators (NCO) based controlled oscillator frequency Modulation is implemented. Initially, input is given to the analog to digital converter (ADC) converter. This will change the input from analog to digital converter. After that, the pulse skipping mode (PSM) logic and proportional integral (PI) are applied to the converted data. After applying PSM logic, data is directly transferred to the connection block. The proportional and integral block will transfer the data will be decoded using the decoder. After decoding the values, it is saved using a modulo accumulator. After that, it is converted from one hot residue (OHR) to binary converter. The converted data is saved in the register. Now both data will pass through the gate driver circuit and output will be obtained finally. From simulation results, it can observe that the usage of metal oxide semiconductor field effect transistors (MOSFETs) and total nodes are very less in dual-mode NCO-based controlled oscillator frequency modulation.

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1. INTRODUCTION

The network crystal oscillator is mainly a controlled oscillator (CO) used in the digital communication world. In digital communication systems modems, digital radios, digital converters and computer base stations are most widely used. A look up table is utilized to crate the real and complex sinusoidal values [1]. Generating phase is mapped by the look-up table to get desired output waveform. Phase argument is generated by the digital integrator. Stability, agility, reliability, and precision are the advantages of numerically crystal oscillator compared with the other oscillators.

By using the frequency synthesis method numerically controlled oscillators (NCO) is most widely used. In digital communication and digital systems mainly direct digital synthesizer is used to generate the sequence of sinusoidal [2]. The numerically controlled oscillator is also called as voltage-controlled oscillator in the digital world. By using controller input operation of oscillator output is varied based on frequency variation [3]. Look up table using the network crystal oscillator will analyze and implement the system.

Comparison of voltage-controlled oscillator is done with the numerically controlled oscillator. Tuning time, frequency tuning range, fine frequency resolution, and short frequency will give effective output from comparison. NCO gives accurate results based on the digital communication systems. The digital world is controlled based on the convenient measures. The studies [4], [5] introduce the concept of digital synthesis frequency. But in 1974 it was came up. Oscillator which generates numerical control output frequencies are given in (1):

$$f_o = K (f_d 2N) \quad (1)$$

Here output frequency is denoted as f_o in-NCO, accumulator clock frequency is done as f_c in-NCO, the number of bits in the accumulator is denoted as N, and frequency control number is represented as K. The output frequency is given as $f_c/2N$.

By using the ideal filter, the maximum sine output frequency is given as $f_c/2$. In the field of very large-scale integration (VLSI) technology, NCO usage is gradually increasing. The main intent is to simplify the structure, extend the function, reduce the size and increase the clock frequency, and the size of read only memory (ROM) is reduced by using a memory scheme and this is based on the phase-to-amplitude converter [6]–[8]. The pipelined accumulator will increase the performance of speed using the progression state technique. Sometimes, NCO is also known as a local oscillator which will generate the samples in a digital way. 90 degrees in phase is maintained by the digital samples will be in the form of a sine wave. Both sine and cosine signals are generated and created. Sine/cosine look-up tables are utilized by the digital phase accumulator. In numerically controlled oscillator clock of analog to digital converter (ADC) is connected to the local oscillator. Local oscillator sampling is equal to ADC sample clock frequency (f_s). Based on digital samples local oscillator depends. The sampling rate frequency in NCO is represented as f_s [9]. In this, both data rate sources will mix the input sources which are coming from ADC sampling rates. Figure 1 shows the NCO block diagram with basic model input and output elements in Figure 1(a) and internal elements are in Figure 1(b).

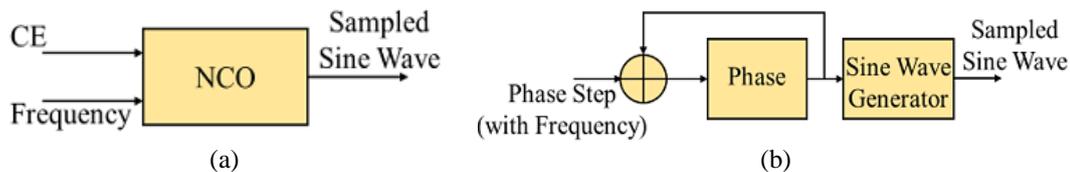


Figure 1. Block diagram of NCO and (a) basic model with input and output elements and (b) NCO internal blocks

To maintain the phase information as an input signal, both input signals of sine and cosine from the local oscillator should create the in-phase and quadrature output (I and Q). The full ADC sampling rate frequency is obtained by decreasing the low pass filter frequency rate. Similarly, in this, the input samples will be mixed at the output to get full sampling rate frequency. To implement finite impulse response (FIR) filter transfer function, in this digital signal processing is used [10]. Basically, the signals which consist of cut-off frequency, then those signals will be accepted as input by the NCO and those signals which consist of above cut-off frequency then the NCO will reject. By using mixer both I and Q signals will be processed by the digital filter which is also known as a complex filter. The section 2 shows the overview of NCO and standard NCO [11]. In section 3 literature survey of NCO. In section 4, dual-mode NCO-based controlled oscillator frequency modulation is given in a detailed manner. In section 5, simulation results are given. In section 6, conclusion is given [12]–[15]. This is mainly used in the applications of computers, digital systems, instrumentation, phase-locked loop systems, marine, modems, sensors, telecommunications, and disk drives.

- Numerically controlled linear chirp oscillator [16]: by using liner chirp, the recursive generator will generate the complex samples. By using the minimum tuning time and minimum possible memory, the generator is characterized.
- Implementation of a 6.5 MHz 34-8 NCO [17]: by using standard 2um P well complementary metal-oxide semiconductor (CMOS) technology, the numerically controlled oscillator is implemented. In this, the numerically controlled oscillator will use the pipeline structure. The clock rate is set up to maximum while giving input. The data acquiring rate of ROM will limit the speed factor and delay and it

- will be based on the accumulator. The clock rate will be improved by the usage of N well CMOS technology and pipeline structure.
- Analysis and design of numerically controlled oscillators based on linear time-variant systems [18]: by using the linear periodically time-variant system, the NCO are designed. The generalization and description analysis are allowed in the numerically controlled oscillator. High spectral purity will be obtained by the demonstration of NCO.
 - Comparison of various numerically controlled oscillators [19]: compared with the other direct digital NCOs, coordinate rotation digital computer (CORDIC) based NCO will use less hardware and cost is also very low. Nyquist frequency is used in the NCO. In this, the number of bits is represented as N. CORDIC based NCO main intent is to use the hardware low compared with the popular lookup table-based NCO. But both CORDIC-based NCO and look-up table (LUT) based NCO need an additional clock. At last, the synchronization will be easier in the CORDIC-based NCO and LUT-based NCO.
 - A numerically controlled oscillator based on de Moivre's identity and linear approximation [20]: in digital communication systems, discrete sinusoidal quadrature signal generators are most widely used. This will control the data using quadrature signal generators. Hence in this paper, de Moivre trigonometric identity is introduced for the numerically controlled quadrature sinusoidal signal generator. By using the linear approximation and some trigonometric identities, a coarsely generated de Moivre oscillator is introduced. A number of look-up tables are used in this method which will limit the frequency range by using a multiplier. Low power requirements, excellent spectral characteristics, and good controllability are obtained from the implementation and simulation results. The proposed method will use both simulation results and error analysis. This numerically controlled oscillator is implemented using VLSI and field programmable gate array (FPGA) implementations.
 - FPGA implementation and performance evaluation of a digital carrier synchronizer using different numerically controlled oscillators [21]: the three different NCOs are designed and evaluated in the paper based on the digital carrier synchronizer (DCS). This technology is based on the FPGA which is the combination of modulator-demodulator applications. By using the CORDIC, Xilinx ROM-based NCO, and LUT configurations the data will be adopted. Based upon each configuration the data will provide a good trade-off. Hence by using Xilinx ROM the NCO will perform a better operation and gives effective results.
 - Design and implementation of numerically controlled oscillator [22]: basically, the digital communication system is the combination of modems, computer base stations, digital radio, computers, and digital converters. All these are the parts of an NCO. Both complex and real values are created by the look-up table. By using the ModelSim software tool the entire NCO design is simulated. The shorter improvement cycle, overall performance, and decreased cost are increased by the FPGA implementation technique. By using Xilinx ISE 14.7 version FPGA, the entire paper represents NCO design and implementation.
 - A high-speed pipelined CMOS accumulator for implementing numerically controlled oscillators [23]: In this paper design of a numerically controlled oscillator is done by using high-speed CMOS technology. In this, the mainly used techniques are device sizing, pipelined structure, exhaustive logic partition, and single-phase clocking. Under the fabrication process, they have used 2 pm p-well and 1.6 pm n-well MOSIS CMOS processes. The capability of the microprocessor is controlled by the interfacing of frequency.
 - Design and analysis of operating mode digital-control step-up switched-capacitor power converter with pulse-skipping and numerically controlled oscillator-based frequency modulation [24]: 3 to 5 V integrated operating mode digital-control step-up switched-capacitor (SC) power converter is implemented in this paper. By using a low-power analog-to-digital converter, the feedback control circuit is monitored. This monitored data is feedback to the digital controller. By using the pulse skipping mode, the control loop will be operated. The operating control loop will have high-frequency modulation and this will depend on the numerically controlled oscillator.
 - Area optimized CORDIC-based numerically controlled oscillator for electrical bio-impedance spectroscopy [25]: In this 10-bit NCO based on iterative architecture is implemented. Mainly NCO will be based on the CORDIC. This CORDIC-based NCO will optimize in terms of area. The CORDIC-based NCO is implemented using TSMC CMOS 180 nm technology process. To apply electrical bioimpedance spectroscopy (EBS) to cervical cancer detection (CCD), design specifications will be required. 32 different frequencies are generated using the architecture. This is based on the sinusoidal output signals. The maximum error frequency values are obtained while compared with the theoretical and experimental results.

2. NUMERICALLY CONTROLLED OSCILLATORS (NCO) AND STANDARD NCO

NCO has become an important hardware solution for generating high-speed high-precision standard periodic function waveforms like sine, cosine, triangle, saw-tooth, and square-wave. Hardware-implemented algorithm delivers the periodic functions which are considered based on the digital signal processors. Digital word sequences are rendered by the NCO in time by converting into an analog oscillatory signal. As usual, the additionally required digital-to-analog converter (DAC) is not included in the NCO. The phase accumulator is included in the numerical crystal oscillator which is the simplest among all oscillators. Phase accumulator will provide some output bits by using address input. Because of this, the data will be saved in ROM.

Figure 2(a) shows the basic table which is based on NCO. The output frequency will be controlled by using accumulator input. Based on the phase truncation of bits the frequency is controlled. Random-access memory (RAM) is utilized to save the data of NCO which are depending on the FGPAs. Depend on operating conditions the content can be changed. Hence NCOs are fitted to digital designs. Consumption of more power and memory is done when data is not accessed with look-up table-based NCOs. To overcome the usage of more power and memory standard NCO is introduced. High output signal quality is obtained by using the standard numerically controlled oscillator. Linear and non-linear interpolation uses sample points to identify the identities. ROM is used to store the identities. Quality of generated sinusoidal signal is measure by using the spurious free dynamic range (SFDR) technique. Amplitude-frequency and frequency spectrum difference is provided by this technique. SFDR consists of high signal rate and generated signals purity is represented by this technique. Quality of signal is measured by using both sine and cosine signals based on NCOs. At the same amount the sinusoidal signal rate will be increased. Output rate will be fixed when the signal of frequency is determined. Both the phase value and sine value will be known when the signal will be known. Signals are realized in straight forward by describing the signal in NCO. Block diagram of the standard NCO is shown in Figure 2(b). Memory and accumulator are both combination of standard numerically controlled oscillator. Signals are computed by the phase when sine values and accumulator are utilized. By using memory, the obtained values will be saved. V bit accumulator register is interpreted in value A while two's complement is performed. Non-negative integer is nothing but interruption of value. For every clock pulse data of N is added to A. Hence for every clock pulse there is an increment.

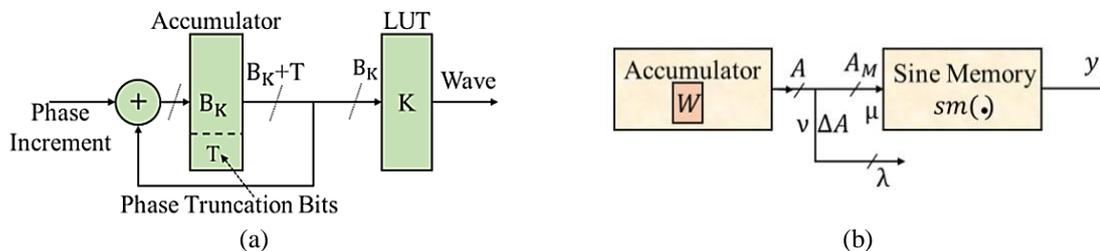


Figure 2. NCO table model with bits representation and SNCO block (a) basic table-based NCO and (b) SNCO block diagram with indication of Latina parameters

3. DUAL-MODE NCO BASED CONTROLLED OSCILLATOR FREQUENCY MODULATION

The block diagram of dual-mode NCO-based controlled oscillator frequency modulation is shown in Figure 3. Initially, input is given to the ADC converter. This will change the input from analog to digital converter. After that, the pulse skipping mode (PSM) logic and PI are applied to the converted data. After applying PSM logic, data is directly transferred to the connection block. The proportional and integral block will transfer the data will be decoded using the decoder. After decoding the values, it is saved using a modulo accumulator. After that, it is converted from one hot residue (OHR) to binary converter. The converted data is saved in the register. Now both data will pass through the gate driver circuit and output will be obtained finally. Based on the present error, the proportional (P) will be dependent. Based on the past error, the integral I will be dependent. The combination of these two factors will give proportional and integral. This will adjust and control the circuit in various systems. Basically, proportional is inversely proportional to the proportional gain. By multiplying the error using constant K_p is nothing but a proportional gain and which is also known as proportional response. This can be adjusted by using constant error. The proportional term is represented as shown in (2).

$$P = K_p \cdot Error(t) \tag{2}$$

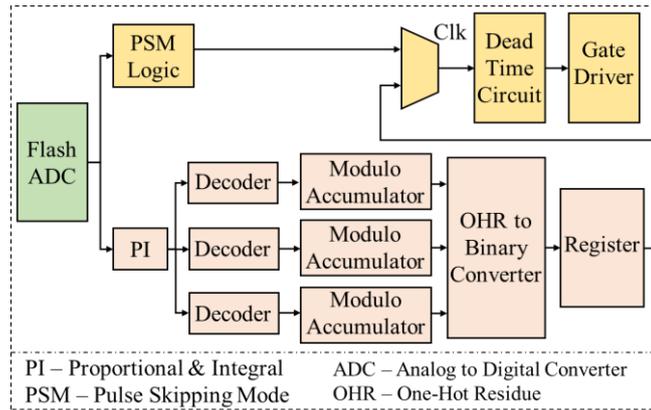


Figure 3. Block diagram of dual-mode NCO based controlled oscillator frequency modulation

For a given change, there will be errors obtained in the output in the proportional gain results. The entire system will become unstable when the proportional gain is high. If a small gain is obtained in a small output response, a large input error is obtained. The control action will be very low when the control action is very small. Because of this, there will be some disturbances. In this proportional controller (K_p) is used to reduce the rise time and errors. Both duration of error and magnitude of error is proportional to the Integral controller (IC). The sum of instantaneous error will give the integral in a PI controller. This is accumulated based on the offset which is corrected previously. By eliminating the steady-state error, integral control (K_i) will be obtained. The combination of 'n' input lines and 2^n output lines is nothing but a decoder. Depending on the combination of inputs; the outputs will be active high. At this time the decoder will be enabled. Hence the decoder will use a particular code to detect.

The energy storage device is nothing but a modulo accumulator. The modulo accumulator will accept the data and store the data when it is needed. The energy will be delivered based on the long interval and short interval time. Long time interval time is obtained at a low rate and short time interval time is obtained at a high rate. OHR number system is simple in nature and it gives minimum energy dissipation for the circuit. The main intent of using the OHR number system is to increase the speed of operation. In the OHR number system, signals are represented using m modulus. In this one signal is high and active at one clock cycle and another signal is low at another clock cycle. This data is obtained from the forward voltage. By using the module set, each data in the OHR number system will be represented.

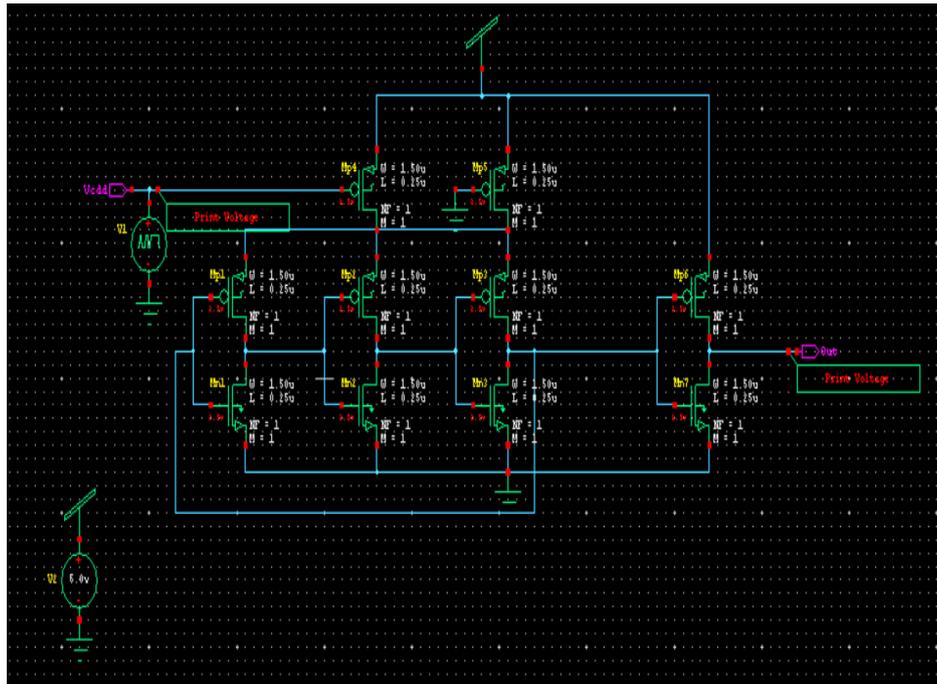
The dead-time circuit is used to lose the data which is obtained from the forward voltage of the diode. This will switch the data to the low side based on metal oxide semiconductor field effect transistors (MOSFET). At the dead time, the load current is obtained. By using voltage input and ground, the short circuit state gives effective results. Basically, the main intent of the gate driver circuit is to amplify the low power input from the controller. In the same way to produce the high current drive input based on the high-power transistor. By using a chip or discrete model, the gate drivers are provided. Figure 4 shows the comparing simulation results in NCO based controlled oscillator frequency modulation performance with dual mode. Figure 4(a) shows the schematic design of dual-mode NCO-based controlled oscillator frequency modulation. 10 MOSFETs are utilized while designing this circuit. 8 total nodes are utilized, 3 boundary nodes and 5 independent nodes are utilized while designing this circuit.

4. RESULTS AND DISCUSSION

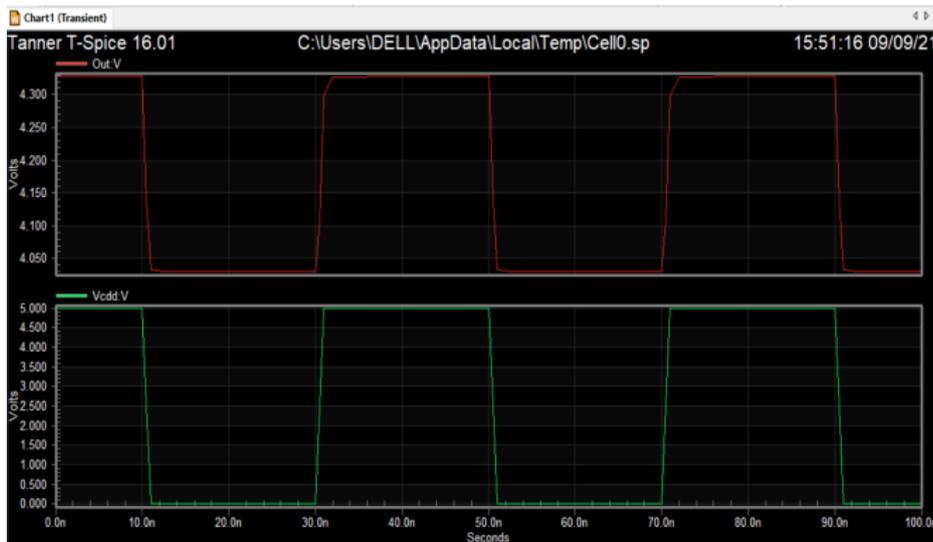
Figure 4(b) shows the output waveform of dual-mode NCO-based controlled oscillator frequency modulation. The Table 1 shows the comparison tabular form of recursive numerically controlled polynomial phase signal oscillator, numerically controlled oscillator based on linear approximation, NCO based controlled oscillator, and dual-mode NCO based controlled oscillator. In this tabular form utilization of the number of MOSFET's and number of total nodes, boundary nodes, and independent nodes are given in detailed manner.

The Figure 5(a) shows the comparison of the utilization of a number of MOSFETs. Compared with recursive numerically controlled polynomial phase signal oscillator, NCO based controlled oscillator, the dual-mode NCO based controlled oscillator takes 10 MOSFET's to design. From this, it can observe that a dual-mode NCO-based controlled oscillator takes less number of MOSFETs to design. The Figure 5(b) shows the comparison of the utilization of a number of total nodes. Compared with recursive numerically

controlled polynomial phase signal oscillator, NCO based controlled oscillator, the dual-mode NCO based controlled oscillator takes less number of total nodes to design. The Figure 5(c) shows the comparison of accuracy for recursive numerically controlled polynomial phase signal oscillator, NCO-based controlled oscillator and dual-mode NCO-based controlled. Compared with recursive numerically controlled polynomial phase signal oscillator, NCO based controlled oscillator, the dual-mode NCO based controlled will improve the accuracy in a very effective way. The Figure 5(d) shows the comparison of delay for recursive numerically controlled polynomial phase signal oscillator, NCO-based controlled oscillator, and dual-mode NCO-based controlled. Compared with recursive numerically controlled polynomial phase signal oscillator, NCO based controlled oscillator, the dual-mode NCO based controlled will reduce the delay in a very effective way.



(a)

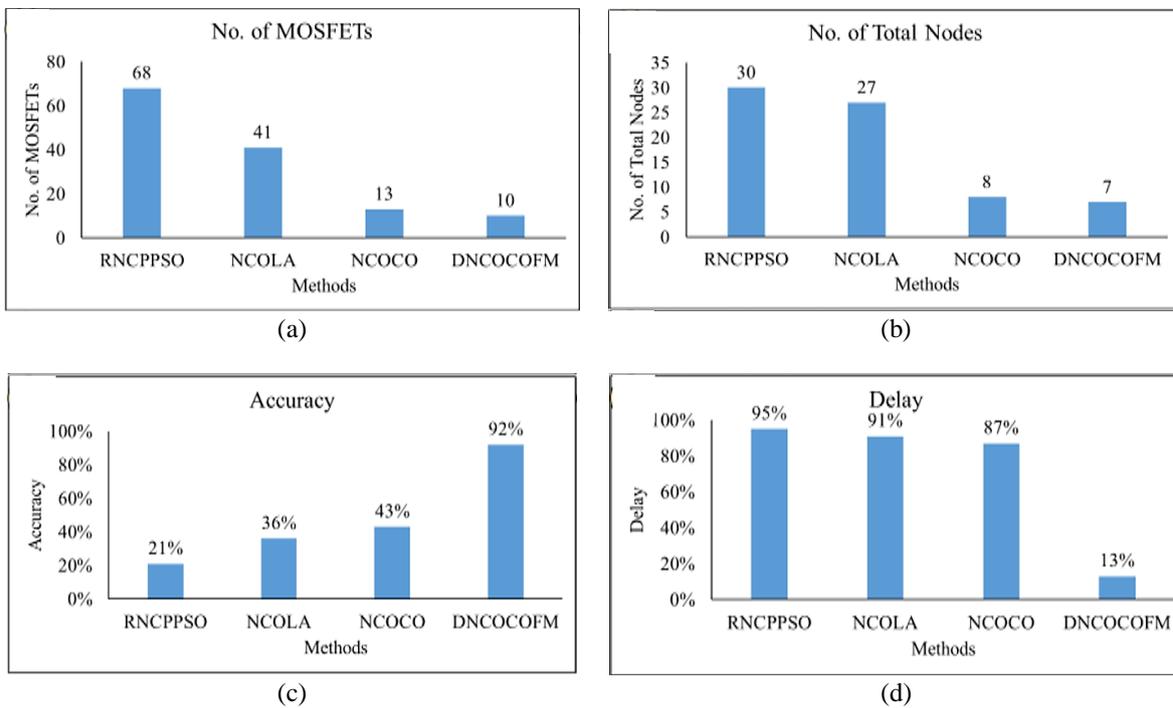


(b)

Figure 4. Comparing simulation results in NCO based controlled oscillator frequency modulation performance with dual mode in (a) schematic design of NCO based controlled frequency modulation and (b) resultant waveforms of dual mode NCO based controlled oscillator frequency modulation

Table 1. Several parameters comparison of NCO based controlled oscillator and dual mode NCO based controller oscillator frequency modulation

SI No.	Parameter	Recursive numerically controlled polynomial phase signal generator	Numerically controlled oscillator based on linear approximation	Numerically controlled oscillator based controlled oscillator	Dual-mode NCO based controlled oscillator frequency modulation
1	Number of MOSFETs	68	41	13	10
2	Number of independent nodes	20	14	5	4
3	Number of boundary nodes	10	13	3	3
4	Number of total nodes	30%	27%	8%	7%
5	Accuracy	21%	36%	43%	92%
6	Speed	9%	11%	16%	96%
7	Delay	95%	91%	87%	13%
8	Noise	98%	94%	91%	9%



- RNCPPSO – Recursive Numerically Controlled Polynomial Phase Signal generator
- NCOLA – Numerically Controlled Oscillator based on Linear Approximation
- NCOCO – Numerically Controlled Oscillator based Controlled Oscillator
- DNCOCOFM – Dual-mode NCO based Controlled Oscillator Frequency Modulation

Figure 5. Comparison chart (a) number of transistors uses, (b) total number of nodes used in each method, (c) accuracy estimates for all used methods, and (d) delay for RNCPPSO, NCOLA, NCOCO, and DNCOCOFM methods

5. CONCLUSION

Hence in this paper, the design and analysis of dual-mode NCO based controlled oscillator frequency modulation was implemented. The study of NCO and standard NCO is given in a detailed manner. The combination of proportional and integral (P&I) will reduce the errors in a very effective way. From simulation results, it can observe that the usage of MOSFET’s and total nodes are very less in dual-mode NCO based controlled oscillator frequency modulation.

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