Multiple inputs all-optical logic gates based on nanoring insulator-metal-insulator plasmonic waveguides

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ABSTRACT

In this paper, we report new nanoscale plasmonic multiple inputs logic gates based on insulator-metal-insulator (IMI) nanoring waveguides. The proposed all-optical gates are numerically analyzed by the finite element method. NOT, AND, NAND, NOR, and EX-NOR all-optical logic gates were suitably designed and investigated based on the linear interface between the propagated waves through the waveguides. The operation wavelength was 1550 nm. The simulation results show that the optical transmission threshold of (0.26) which performs the operation of planned logic gates is accomplished. Moreover, simulation results show that our compact structure of all-optical logic gates may have potential applications in alloptical integrated networks.

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1. INTRODUCTION

For years, researchers have been focusing their attention on all-optical devices in preparation for alloptical systems. To get over the constraints of conventional photonic devices such as diffraction limit, and power consumption, all-optical processing systems have been actively studied in recent years. As a result, alloptical logic gates have a low power consumption of a few microwatts and fast temporal response of a few picoseconds [1], [2]. Despite the widespread use of plasmonic in all-optical processing, several disadvantages remain, such as substantial metal resistive losses; as a result, plasmonic systems are known as lossy systems when it comes to surface plasmon polaritons (SPPs), losses limit their wave propagation length to a few nanometers or micrometers at the most [3]. Interference between waves in input and control waveguides at cavity resonance wavelengths serves as the basis for operation [4]. The phase of the incident light wave at inputs and control ports will be tuned, and the total propagation losses in each state of activation will be modified correspondingly, to realize the behavior of all-optical logic gates according to their truth tables. As a result of substantial propagation losses, if the activation states of the three inputs in an AND gate are (OFF-OFF-ON), the output state should be (OFF). There has been a slew of designs for all-optical devices in optical processing in the wake of their widespread use [5]-[9]. There are a variety of two and three input alloptical plasmonic logic gates [10]–[23]. All-optical plasmonic logic gates with three inputs have only seen a few theoretical demonstrations yet, according to our understanding. All-optical logic gates with three inputs are ultra-compact (nano-scale size) and can transmit optical signals reaching 100% in some circumstances. In

our work, we have demonstrated the maximum number (five) of three inputs all-optical logic gates. The demonstrated all-optical gates are; NOT, AND, NAND, NOR, and EX-NOR.

Here are the sections of the article's structure: in section 2 the design and layout of the suggested structure are presented, together with the theoretical principles of operation. Part 3 presents all-optical logic gates with three inputs and simulation results. Part 4 represents the culmination of our investigation.

2. METHOD

Figure 1 depicts the suggested design of three input all-optical logic gates. The proposed structure has dimensions of (400×400) nm. Four linear waveguides (straight waveguides) and three nano-ring resonators based on plasmonic IMI technology are used in the structure. The second straight waveguide (L_T) is 400 nm long, while the other straight waveguides (L) are 240 nm long; the waveguide's width (w) is 15 nm. The outer (R) and inner (r) ring resonators have radii of 40 and 25 nm, respectively. The straight waveguides and ring resonators are separated by a spacing distance (d) of 5 nm. The Johnson and Christy data model was employed in our simulation design to characterize the permittivity of the metal material, which was silver [24], and the insulator material's refractive index (n) was 1.292. The operation wavelength of 1,550 nm was chosen for use in our proposed system due to its numerous applications in optical communications.



Figure 1. The proposed structure of three inputs all-optical logic gates

The effective refractive index and structural characteristics of the material dictate the resonance wavelengths of plasmonic systems [25]. The proposed gates are evaluated by considering the transmitted optical power as a function of incident wavelength, and the contrast ratio (CR) between the (ON and OFF) states. It is possible to consider the optical power transmission from the input and control ports to the output port by setting a transmission threshold of (0.26). Any transmission value larger than (0.26) is in a (logic 1) or (ON state; otherwise, it is in a (logic 0) or (OFF state). These proposed gates operate better when their contrast (extinction ratios) is higher, suggesting that they work less well when this ratio is lower. The optical transmission and contrast (extinction) ratios are explained by (1) [12] and (2) [21].

$$T = \frac{P_{out}}{P_{in}} (For the two states ON and OFF of the output port)$$
(1)

Where P_{out} is the output power at the output port, while P_{in} is the input power at the incoming port, and T denotes optical transmission.

$$\frac{ON}{OFF}Contrast(extinction)ration(dB) = 10 \log \left[\frac{P_{out}(ONstate)}{P_{in}(OFFstate)}\right]$$
(2)

Where $P_{out}(ONstate)$ is the transmitted signal in ON state (logic 1), and $P_{in}(OFFstate)$ is the transmitted signal in OFF state (logic 0). The transmitted optical power can be optimized based on the proposed design parameters, and other factors such as the material's refractive index and phase. In the proposed plasmonic gates, linear interference between waves in waveguides is used as the basis for operation. Phase and placement of active ports (input, control) influence the amount of interference between incident light waves in the near field regime, where the (SPR) is strongest. Increasing the spacing distance (d) increases transmitted power. To attain the desired activation state on the output port, the all-optical logic gate's truth table determines how the incident wave's phase is regulated, resulting in different total losses. The waveguide losses are described in (3) [26].

 $T + R + A \tag{3}$

Where (T) is the transmitted power, (R) is the reflected power, and (A) is the absorbed power. The reflected (R) and absorbed (A) power is taken into consideration as power losses.

3. RESULTS AND DISCUSSION

The proposed structure of multiple inputs logic gates has a total of five ports. Three ports for inputs, one for control (activation), and one for output. The inputs and activation ports' activation statuses are controlled to provide the output port's plasmonic logic gate functionality.

3.1. All optical AND logic gate

To implement the plasmonic AND gate functionality in our design, port 2 is regarded as the control (activation) port, ports 1, 3, and 4 are considered the input ports, and port 5 is considered the output port. According to the AND gate's truth table, the output state is ON only when all three input states are ON. Due to the destructive interference between the light waves propagating via the active ports (*input+control*) as a result of the varying phase angles, the output state of this gate is always (OFF), unless when all inputs are in the (ON) state. When all input states are (ON), the constructive interference between the propagating light waves causes the normalized transmission to be as high as possible (exceeds 100%). The proposed AND gate's transmission threshold is (0.26). The AND logic gate's symbol and truth table are depicted in Figure 2(a). Figure 2(b) depicts the normalized transmission spectrum of the proposed plasmonic AND gate as a function of wavelength. Figures 2(c) and 2(d) illustrate the magnetic field of the proposed all-optical AND gate under various situations. The proposed AND gate's operation is summarized in Table 1.

3.2. All optical NAND logic gate

A NAND logic gate's output is (OFF) only when all inputs are (ON); otherwise, the output is (ON). To simulate the NAND logic gate, we use the constructive and destructive phenomena between the inputs and control ports. The input ports selected are (2 to 4), the control port is (port 1), and the output port is (port 5). The proposed NAND gate's transmission threshold is (0.26). Figure 3(a) depicts the NAND logic gate's symbol and truth table. As demonstrated in Figure 3(b), the suggested plasmonic NAND gate's normalized transmission spectrum is plotted against wavelength. Figures 3(c) and 3(d) demonstrate the proposed plasmonic NAND gate's operational data.

3.3. All optical NOR logic gate

In our suggested design, we used ports 2 to 4 as input ports and ports 1 as control (activation) ports to achieve NOR logic gate functionality. When all three input states are (OFF), the output is (ON). Because of the phase difference between the propagating light waves in the inputs and control ports, destructive interference occurs in all other input states, resulting in an output state that is (OFF). The proposed NOR gate's transmission threshold is (0.26). Figure 4(a) depicts the NOR logic gate's symbol and truth table. Figure 4(b) shows a plot of the wavelength-dependent optical transmission spectrum of the proposed gate. A plasmonic NOR gate with different magnetic field profiles is depicted in Figures 4(c) and 4(d). Table 3 provides an overview of the plasmonic NOR gate's functionality.

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Figure 2. AND logic gate structure (a) symbol and truth table, (b) optical transmission as a function of wavelength at different status, (c) and (d) the magnetic field at different input states: 000 and 111 respectively



Figure 3. NAND logic gate structure (a) symbol and truth table, (b) normalized transmission as a function of wavelength at different conditions, (c) and (d) the magnetic field profile at different input states: 000 and 111 respectively



Figure 4. NOR logic gate structure (a) symbol and truth table, (b) normalized transmission as a function of wavelength at different statuses, (c) and (d) the magnetic field at different input states: 000 and 111 respectively

Table 1. Specifications of the proposed all-optical AND gate								
Port 1 Input	Port 3 Input	Port 4 Input	Port 2 Status	Port 5	Optical	Propagation	Contrast	
Status and	Status and	Status and	and (Phase°)	Output	Transmission T	Losses (1-T)	Ratio (CR)	
(Phase°)	(Phase°)	(Phase°)	Control	Status		L033C3 (1-1)	Katio (CK)	
OFF (0°)	OFF (0°)	OFF (0°)	ON (0°)	OFF	0.04	0.96		
OFF (0°)	OFF (0°)	ON (180°)	ON (45°)	OFF	0.004	0.996		
OFF (0°)	ON (180°)	OFF (0°)	ON (45°)	OFF	0.005	0.995		
OFF (0°)	ON (180°)	ON (180°)	ON (45°)	OFF	0.037	0.936	10.62 (dB)	
ON (45°)	OFF (0°)	OFF (0°)	ON (180°)	OFF	0.11	0.89	10.02 (UD)	
ON (45°)	OFF (0°)	ON (180°)	ON (180°)	OFF	0.012	0.988		
ON (45°)	ON (180°)	OFF (0°)	ON (180°)	OFF	0.043	0.957		
ON (0°)	ON (0°)	ON (0°)	ON (0°)	ON	1.271	0		

Table 2. Operation information of the proposed all-optical NAND gate

Port 2 Input Status and	Port 3 Input Status and	Port 4 Input Status and	Port 1 Control Status and	Port 5 Output	Optical	Propagation	Contrast Ratio
(Phase°)	(Phase°)	(Phase°)	(Phase°)	Status	Transmission T	Losses $(1-T)$	(CR)
OFF (0°)	OFF (0°)	OFF (0°)	ON (0°)	ON	0.289	0.711	
OFF (0°)	OFF (0°)	ON (0°)	ON (0°)	ON	0.626	0.374	
OFF (0°)	ON (0°)	OFF (0°)	ON (0°)	ON	0.451	0.549	
OFF (0°)	ON (0°)	ON (0°)	ON (0°)	ON	0.857	0.143	14.6
ON (0°)	OFF (0°)	OFF (0°)	ON (0°)	ON	0.546	0.454	(dB)
ON (0°)	OFF (0°)	ON (0°)	ON (0°)	ON	0.985	0.015	
ON (0°)	ON (0°)	OFF (0°)	ON (0°)	ON	0.762	0.238	
ON (45°)	ON (180°)	ON (180°)	ON (180°)	OFF	0.01	0.99	

Table 3. Specifications of the proposed all-optical NOR gate

Port 2 Input Status and (Phase°)	Port 3 Input Status and (Phase°)	Port 4 Input Status and (Phase°)	Port 1 Control Status and (Phase°)	Port 5 Output Status and (Phase°)	Optical Transmission T	Propagation Losses (1-T)	Contrast Ratio (CR)
OFF (0°)	OFF (0°)	OFF (0°)	ON (0°)	ON	0.289	0.711	
OFF (0°)	OFF (0°)	ON (180°)	ON (45°)	OFF	0.085	0.915	
OFF (0°)	ON (180°)	OFF (0°)	ON (45°)	OFF	0.164	0.836	
OFF (0°)	ON (180°)	ON (180°)	ON (45°)	OFF	0.029	0.971	2.46 (dD)
ON (180°)	OFF (0°)	OFF (0°)	ON (45°)	OFF	0.114	0.886	2.46 (dB)
ON (180°)	OFF (0°)	ON (180°)	ON (45°)	OFF	0.012	0.988	
ON (180°)	ON (180°)	OFF (0°)	ON (45°)	OFF	0.043	0.957	
ON (180°)	ON (180°)	ON (180°)	ON (45°)	OFF	0.01	0.99	

3.4. All optical EX-NOR logic gate

When an even number of inputs are in the (ON) state or when all inputs are in the (OFF) state, the EX-NOR gate's output is (ON); otherwise, the output is (OFF). The input ports of our suggested EX-NOR gate are (2 to 4), the control port is (1), and the output port is (5). The constructive and destructive interference between light waves in the input and control ports is used to implement the EX-NOR gate's function. The transmission threshold of the proposed EX-NOR gate is at least (0.26).

Figure 5 shows the EX-NOR logic gate symbol and truth table of EX-NOR gate. The normalized transmission spectra of the proposed plasmonic EX-NOR gate as a function of wavelength are shown in Figure 5(a) and Figure 5(b). The magnetic profiles of the proposed EX-NOR gate at different statuses are shown in Figure 5(c) and Figure 5(d). The specifications of the proposed EX-NOR gate are presented in Table 4.

3.5. All optical NOT logic gate

Only three ports are utilized in our proposed construction to achieve the all-optical NOT gate's behavior, and the remaining two ports are not used. There are three ports: the input, the control, and the output ports. Destructive interference between input and control port signals, resulting from their different phase angles, flips the applied light wave at its output, enabling the NOT gate action. The proposed NOT gate's transmission threshold is (0.26).

Figure 6(a) depicts the NOT logic gate's symbol and truth table. Figure 6(b) depicts the proposed plasmonic NOT gate's normalized transmission spectrum as a function of wavelength. In various situations, a plasmonic NOT gate's magnetic field is depicted in Figures 6(c) and 6(d). Table 5 summarizes the operational details of the proposed plasmonic NOT gate.



Figure 5. EX-NOR logic gate structure (a) symbol and truth table, (b) optical transmission as a function of wavelength at different statuses, (c) and (d) the magnetic profile at different states: 000 and 111 respectively



Figure 6. NOT logic gate structure (a) symbol and truth table, (b) normalized transmission as a function of wavelength at different conditions, (c) and (d) the magnetic field profile at different input states: 0 and 1 respectively

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Table 4. Specifications	of the propo	sed all-optical	EX-NOR gate
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Tuble 1. Specifications of the proposed an optical EXTING gate								
Port 2 Input Status and (Phase°)	Port 3 Input Status and (Phase°)	Port 4 Input Status and (Phase°)	Port 1 Control Status and (Phase°)	Port 5 Output Status	Optical Transmission T	Propagation Losses (1-T)	Contrast Ratio (CR)	
OFF (0°)	OFF (0°)	OFF (0°)	ON (0°)	ON	0.289	0.711		
OFF (0°)	OFF (0°)	ON (180°)	ON (45°)	OFF	0.085	0.915		
OFF (0°)	ON (180°)	OFF (0°)	ON (45°)	OFF	0.164	0.836		
OFF (0°)	ON (0°)	ON (0°)	ON (0°)	ON	0.857	0.143	2.46 (dB)	
ON (180°)	OFF (0°)	OFF (0°)	ON (45°)	OFF	0.114	0.886	2.40 (uB)	
ON (0°)	OFF (0°)	$ON(0^\circ)$	ON (0°)	ON	0.985	0.015		
ON (0°)	ON (0°)	OFF (0°)	ON (0°)	ON	0.762	0.238		
ON (180°)	ON (180°)	ON (180°)	ON (45°)	OFF	0.01	0.99		

Table 5. Specifications of the proposed all-optical NOT gate

Port 2 Input Status and (Phase [°])	Port 3	Port 4	Port 1 Control Status and (Phase [°])	Port 5 Output	Optical Transmission T	Propagation Losses (1-T)	Contrast Ratio (CR)
OFF (0°) ON (180°)	Not Used	Not Used	ON (0°) ON (45°)	ON OFF	0.289 0.113	0.711 0.887	4.07 (dB)

4. CONCLUSION

In this study, five fundamental multiple-input all-optical gates were proposed and realized using two-dimensional finite element modeling (FEM). The gates that have been realized so far are the AND, NAND, NOR, XNOR, and NOT gates, among others. Constructive and destructive interference between light waves flowing through waveguides is the basis for the operation of the suggested gates. The coupling process between the structure waveguides and the ring resonators is employed to realize the proposed logic gates. The coupling operation is used to realize the plasmonic logic gates. By manipulating the positions of the input and control ports, as well as the phase of the signal propagating via these ports, the transmission of the optical signal can be regulated (either maximized or minimized). Particle all-optical gates of the suggested design are widely considered to be a fundamental component of ultra-fast all-optical integrated systems.

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