

Design and implementation a novel single switch high gain DC-DC converter based on coupled inductor with low-ripple input current

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ABSTRACT

A novel high-gain and high-efficiency direct current to direct current (DC-DC) converter is introduced in this paper. The presented converter is suitable for low-voltage renewable energy resources such as photovoltaic (PV) and fuel cell (FC). The existence of series inductance with the input source ensures continuous and low-ramp input current, which is important for extracting maximum power from resources. Using coupled inductor technology and an intermediate capacitor in the suggested converter leads to a high gain voltage. In the presented topology for recovering energy from the leakage inductor, reducing voltage stress on the power switch, and so decreasing overall converter losses, a passive clamp circuit is used. The suitable operation range of duty cycle in the converter, besides the leakage inductor, decreases the problem of reverse recovery in diodes. The low value of the leakage inductor and the low volume and cost of the proposed converter are due to the low turn ratio of the coupled inductor. Details of the operation principles of the proposed converter have been discussed in this paper. The presented simulation and laboratory prototype results verify the theoretical analysis and performance of the suggested topology.

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1. INTRODUCTION

The consumption of electrical energy has increased significantly during the past few decades. This has led to a considerable lack of fossil fuel reserves, an increase in greenhouse gases, and global warming. Therefore, in recent years, scientists have concentrated on research to find renewable energy-based solutions to avoid this problem. Photovoltaic (PV), fuel cell (FC), wind, and geothermal are examples of renewable energy resources (RERs). PVs are more popular due to their simple structure and lower cost and maintenance in comparison with other RERs [1]–[7]. Figure 1 shows the simple schematic of a photovoltaic-connected power system. Due to the low output voltage (25 to 50 V) and low efficiency (12% to 25%) of PV panels, their voltage level must be increased to be applicable in grid-connected and/or standalone operations [1]. Two methods are mentioned in the literature for boosting the voltage level of PV panels: i) cascading PV modules or cascading the output terminals of each direct current to direct current (DC-DC) converters together and ii) implementation of high gain DC-DC converters [8]–[11].

The first method has some disadvantages: an increasing number of PV panels will require a vast installation area. Besides, voltage increments on the PV side will cause protection and insulation problems. In [12], the simulation results of different DC-DC converters for PV applications are presented. Nallusamy and Rukmani [13] present a DC-DC converter for low and medium power applications. Partial shading and therefore, reduction of PV array efficiency should also be considered [14]–[17].

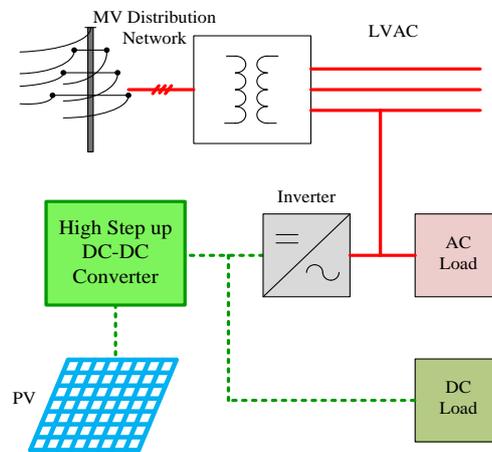


Figure 1. Schematic of a PV-based power system

To obtain high voltage gain from a traditional boost converter, higher duty cycle (D) values should be selected that increase voltage stress on switching components, resulting in low efficiency due to high losses [2], [4]. Also, the diode would not have sufficient time for reverse recovery. Various structures have been introduced to obtain high voltage gain with proper D values. Among them, a coupled inductor is a suitable choice due to its high voltage gain that is obtained with proper D and by adjusting the turn ratio (n) [4]. A suitable DC-DC converter for PV applications must have acceptable efficiency besides its high gain. It should also be able to harvest maximum power from PV with low input current ripple. Das and Agarwal [1] suggests a high-step-up, high-efficiency DC-DC converter. This topology faces high input current variations because it has no input inductor. Therefore, maximum power point tracking (MPPT) is difficult and somehow impossible. Also, a high turn ratio leads to a big leakage inductor and a high volume of the converter. A modified single-ended primary-inductor converter (SEPIC) converter is proposed in [18] that introduces higher voltage gain than the conventional SEPIC through the implementation of coupled inductors. This topology has a lower gain than our proposed converter. Forouzesh *et al.* [19], Liang *et al.* [20] present single-switch coupled inductor-based switched capacitor high-gain converters that have used the voltage doubler technique. These two converters have the same voltage gain but are both lower than the topology presented in this paper. The DC-DC topologies presented in [21], [22] are based on a coupled inductor with an asymmetrical voltage multiplier network and continuous input current, respectively, for PV applications. Both converters provide lower voltage gains than the proposed converter for the same turn ratio n and D conditions. A new high-gain converter based on a coupled inductor and voltage doubler circuit is introduced in [23], [24] that has lower voltage gain and higher input current ripple in comparison with the proposed converter. In [25], a coupled inductor-based high step-up converter based on a voltage doubler circuit and clamp circuit is presented that has lower efficiency, higher input current ripple, and lower voltage gain in comparison with the topologies discussed above. A new topology of DC-DC converters with two coupled inductors and two switches is presented in [26]. Besides implementing two coupled inductors, its voltage gain is lower than the suggested converter in this paper. In [27], a coupled inductor high-step-up converter with three windings and a voltage doubler is presented for PV applications. Higher input current ripple and lower voltage gain are its disadvantages in comparison with the proposed topology. Barmoudeh *et al.* [28] presents a high-step DC-DC converter with a parallel structure whose input current ripple is high and has low voltage gain in comparison with the proposed converter. Non-isolated high-gain DC-DC converters are also used as building blocks for multi-port converters (MPCs). In [29], [30], two novel multi-port DC-DC converters are implemented for PV, storage, and streetcar applications that have at least one step-up building block. All abovementioned gain comparisons with the proposed converter are conducted for similar n and D values.

In this paper, a low ripple input current, non-isolated, high-gain, high-efficiency DC-DC converter is presented. Switched capacitor and coupled inductor technologies lead to the high voltage gain of this converter. Characteristics of the quadratic boost circuit are used in the proposed structure. Passive clamp circuits increase the efficiency of the converter by recovering the stored energy from the leakage inductor and reducing switch voltage stress. The operation principles of the proposed converter for continuous conduction mode (CCM), discontinuous conduction mode (DCM), and boundary modes are presented in section 3. Simulation and experimental results are also provided in section 4.

2. ANALYSIS OF THE PROPOSED TOPOLOGY

Due to the low output voltage and low efficiency of PV panels, converters with high voltage gain and acceptable efficiency are necessary to extract the maximum power from PV with low input current ripples. An exact design procedure that has led to efficient topology derivation makes it a good candidate for PV applications. Figure 2 shows the proposed converter.

L_1, L_2, L_m and L_k are primary side, secondary side, magnetizing and leakage inductors, respectively. The input side of the converter consists of L_{in} , diodes D_1 and D_2 , capacitor C_1 and primary side of the coupled inductor. C_2 and D_3 together are passive clamp circuit. The intermediate capacitor C_3 , diode D_4 and secondary side of the coupled inductor boost the voltage level and finally D_5 is the output diode of the topology. High voltage gains are available with appropriate choices of n and D that lead to lower voltage stress on power switch and optimal size of coupled inductor, respectively. To simplify the analysis of proposed converter, the following assumptions are considered: i) coupling coefficient k is obtained by $\frac{L_m}{L_m+L_k}$ and its turn ratio (n) is $\frac{N_2}{N_1}$ where N_2 and N_1 are the numbers of turns for secondary side and primary side inductors, respectively; and ii) capacitors C_1, C_2, C_3 and C_o are large enough, so the voltage changes over one switching period are ignored and the voltage of the capacitors is considered almost constant.

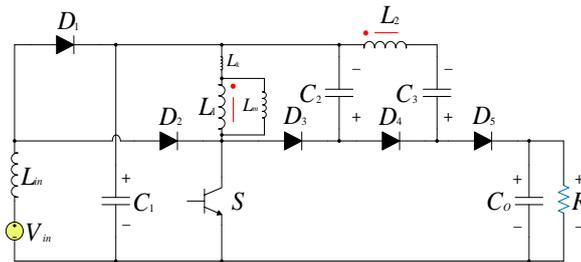


Figure 2. Proposed converter

2.1. Operating modes for CCM

The proposed converter at continuous conduction mode (CCM) has five operating modes that are depicted in Figures 3(a) to 3(e) and 4. These five operating modes are repeated in any switching period.

- Mode 1 [t0-t1]; Figure 3(a): This mode starts when the power metal oxide semiconductor field effect transistor (MOSFET) switch is turned on. D_1 and D_2 are reverse and forward biased, respectively. Input inductor L_{in} is charged by input source through D_2 and S . The magnetizing and leakage inductors are charged via capacitor C_1 . The energy stored in C_3 and secondary side inductor charges output capacitor C_o and feeds load through D_5 . The current of the leakage inductor starts increasing in this short duration to get equal to the current of magnetizing inductor. This mode is finished when the currents of inductors L_k and L_m become equal.

$$I_{D5} = \frac{1}{n} (I_{Lm} - I_{Lk}) \tag{1}$$

- Mode 2 [t1-t2]; Figure 3(b): S is still on and direction of current in inductor L_2 is changed by increasing the value of I_{Lk} to more than I_{Lm} . Energy stored in inductor L_2 and C_2 charges the capacitor C_3 through D_4 . Diodes D_1 and D_5 are reverse biased. Input inductor L_{in} is charged via input source through D_2 and S and also its current increases. Capacitors C_1 and C_o are discharged to charge magnetizing and leakage inductors. The load is fed by C_o . This mode continues until the switch gets turned off.

$$I_{D4} = I_{C3} = -I_{C2} = \frac{1}{n} (I_{Lk} - I_{Lm}) \tag{2}$$

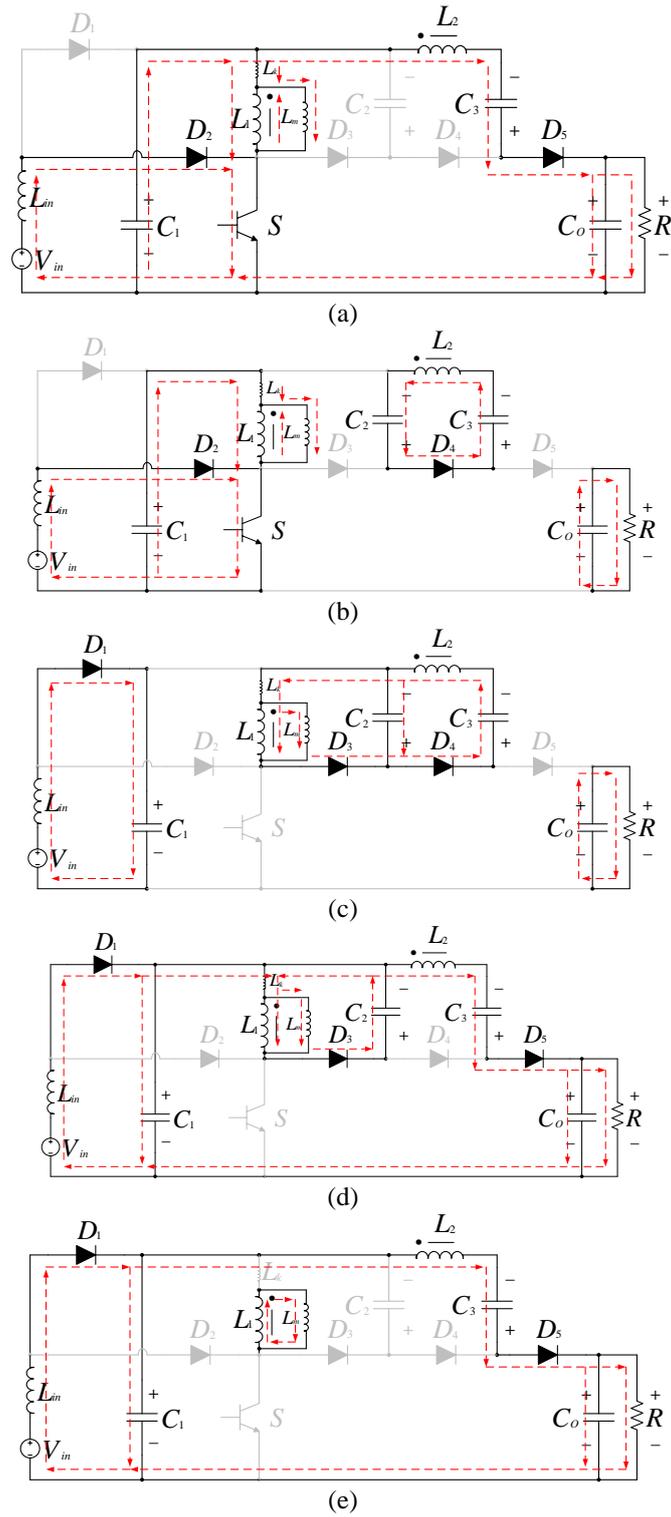


Figure 3. Operating modes of proposed topology during CCM

From modes 1 and 2, the (3) can be derived.

$$\begin{cases} I_{Lin} = I_{D2} \\ I_{Lin}(t_2) = \frac{1}{L_{in}} \int_{t_0}^{t_2} V_{in} \cdot dt + I_{Lin}(t_0) \rightarrow \Delta I_{Lin} = \Delta I_{D2} = \frac{V_{in} \cdot D}{L_{in} \cdot f_s} \\ t_2 - t_0 = DT_s \end{cases} \quad (3)$$

- Mode 3 [t2-t3]; Figure 3(c): By turning off the switch in this mode, D_3 becomes forward biased and transfers the energy of leakage inductor to C_2 , therefore C_2 is being charged. D_1 and D_2 are forward and reverse biased, respectively. Capacitor C_1 is charged via input voltage source and input inductor and the current of leakage inductor is decreasing. This short duration mode is finished when I_{Lm} becomes equal to I_{Lk} .

$$I_{C2} = -\left(\frac{1}{n}(I_{Lk} - I_{Lm}) - I_{Lk}\right) \tag{4}$$

- Mode 4 [t3-t4]; Figure 3(d): Diode D_5 becomes forward biased when direction of the current in primary and secondary windings is changed. Energy stored in C_3 and secondary side inductor feeds the load besides charging the output capacitor. D_1 and D_3 are forward biased in this mode, but D_4 is not conducting.
- Mode 5 [t4-t5]; Figure 3(e): Current of the leakage inductor starts to decrease from the end of mode 2 and mode 5 starts when this current becomes zero; thus, diode D_3 becomes reverse biased. Only D_1 and D_5 are conducted in this mode. Capacitors C_0 and C_1 are being charged, but C_3 is discharged.

$$I_{C1} = I_{Lin} - \frac{1}{n} I_{Lm} \tag{5}$$

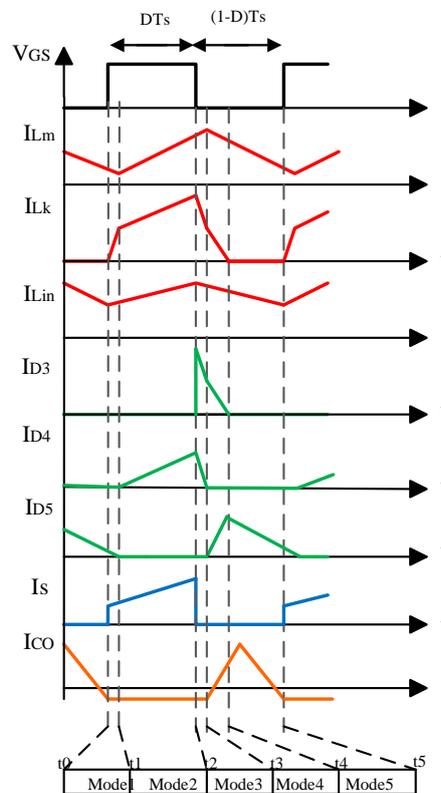


Figure 4. Typical waveforms during CCM operation

2.2. Operating modes for DCM

Discontinuous conduction mode (DCM) for this converter consists of five operating modes. These operating modes and typical waveforms during DCM are depicted in Figures 5(a) to 5(e) and 6, respectively.

- Mode 1 [t0-t1]; Figure 5(a): By turning on the power switch S , this mode is started. D_2 and D_4 are conducting but D_1 , D_3 and D_5 are reverse biased. Input inductor L_{in} is charged by input voltage source through D_2 and S . Magnetizing and leakage inductors are also charged through capacitor C_1 and their currents start increasing from zero. The current of the secondary side inductor passes through D_4 and C_2 is discharged on C_3 . Output capacitor C_0 feeds the load. This mode continues till the switch gets turned off.
- Mode 2 [t1-t2]; Figure 5(b): By turning off the power switch S , this mode is started. Diode D_2 is reverse biased and C_1 is charged via input voltage source and the stored energy in input inductor through D_1 . Diode

D_3 gets forward biased and the energy of leakage inductor is stored in capacitor C_2 . Current of the leakage inductor decreases in this time interval. This mode is finished when I_{Lm} becomes equal to I_{Lk} .

- Mode 3 [t2-t3]; Figure 5(c): In this mode, D_5 becomes forward biased when direction of the coupled inductor's current is changed. The energy of secondary side inductor and capacitor C_3 charge the output capacitor C_o and feed the load. D_1 and D_3 are still forward biased, but D_2, D_4 and S are not conducting.

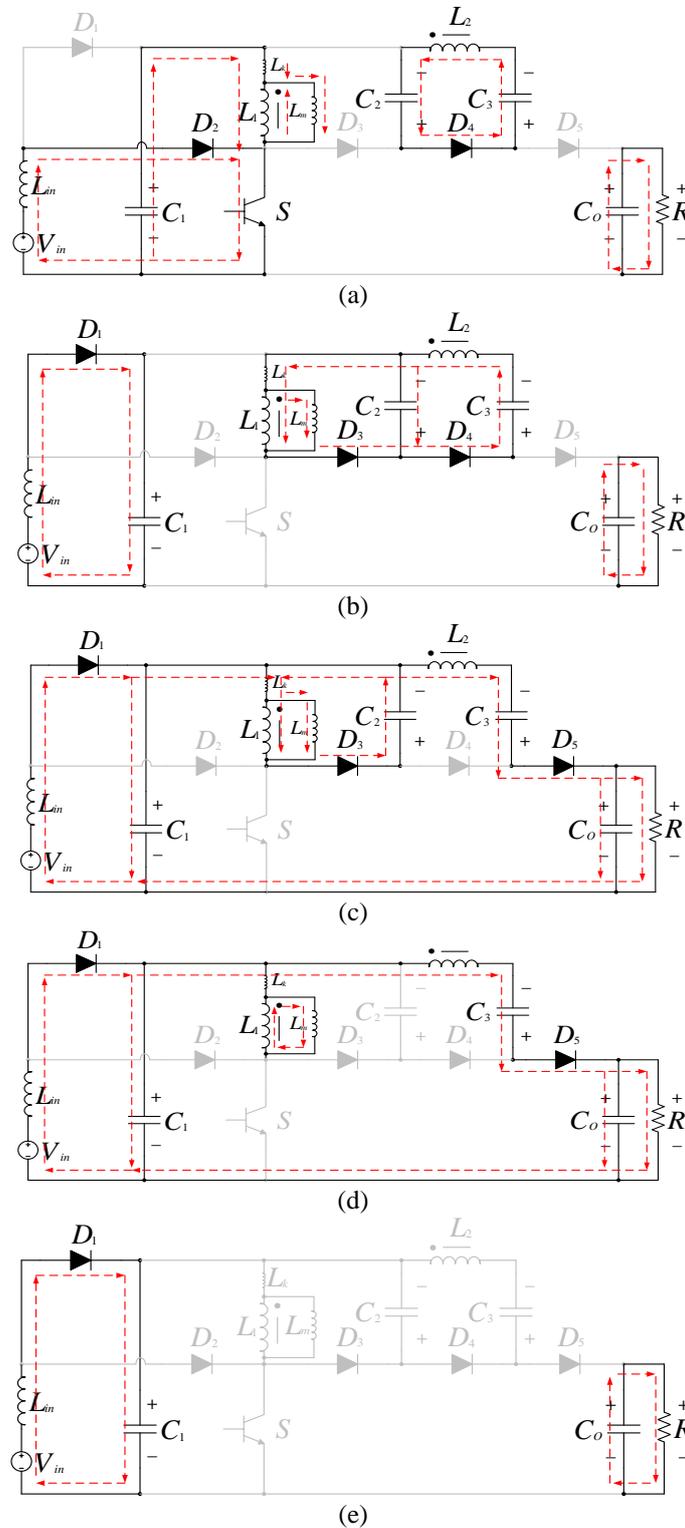


Figure 5. Operating modes of proposed topology during DCM

- Mode 4 [t3-t4]; Figure 5(d): Current of the magnetizing inductor becomes zero in this mode and diode D_3 gets reverse biased. Other components remain at their previous states.
- Mode 5 [t4-t5]; Figure 5(e): This mode starts when the current of magnetizing inductor becomes zero. The secondary side current of the coupled inductor becomes zero and D_5 gets reverse biased. Only D_1 is being conducted, but other diodes and S are turned off.

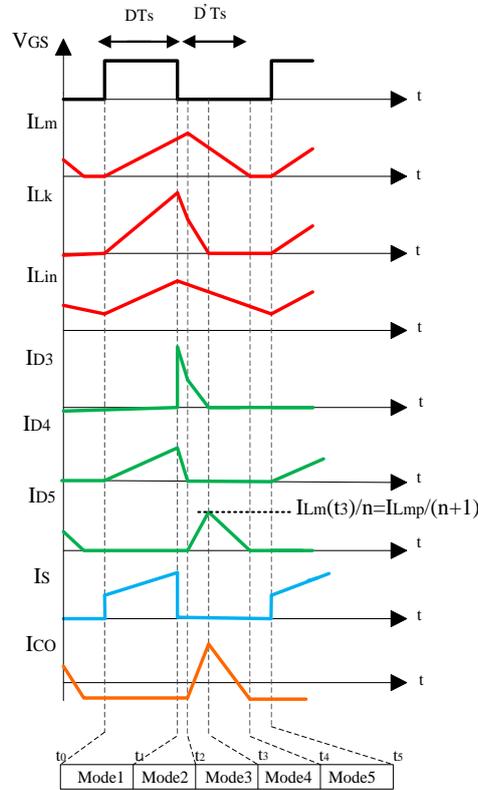


Figure 6. Typical waveforms during DCM operation

3. STEADY STATE ANALYSIS

3.1. Continuous conduction mode

Modes 2, 4, and 5 together from CCM are selected for steady-state analysis to simplify the process. Modes 1 and 3 are neglected due to their short time intervals. The secondary side voltage of the inductor during modes 4 and 5 is as (6).

$$V_{L2} = V_{C1} + V_{C3} - V_{Co} \tag{6}$$

Therefore, the primary side voltage of the inductor in two mentioned modes is similar and can be written as (7).

$$\begin{cases} V_{L1} = -V_{C2} \\ V_{Co} = V_{Load} = V_O \\ V_{in} = V_i \end{cases} \tag{7}$$

From mode 2, the (8) can be obtained.

$$\begin{cases} V_{Lin} = V_i \\ V_{L2} = V_{C3} - V_{C2} \\ V_{L2} = nV_{L1} \\ V_{L1} = V_{C1} - V_{Lk} \end{cases} \tag{8}$$

And from modes 4 and 5, the (9) are derived.

$$\begin{cases} V_{Lin} = V_i - V_{C1} \\ V_{L2} = V_{C1} + V_{C3} - V_{Co} \\ V_{L2} = nV_{L1} \\ V_{L1} = -V_{C2} - V_{Lk} \end{cases} \quad (9)$$

By applying volt-seconds balance law to the inductors L_{in} , L_1 and L_2 have (10)–(13).

$$V_{C1} = \frac{V_i}{1-D} \quad (10)$$

$$V_{C2} = \frac{D \cdot k}{(1-D)^2} V_i \quad (11)$$

$$V_{C3} = \frac{D+(1-D)nK}{(1-D)^2} V_i \quad (12)$$

$$M_{CCM} = \frac{1+nk}{(1-D)^2} \quad (13)$$

The voltage gain waveform versus duty cycle for different coupling coefficient values is shown in Figure 7. This figure shows that the voltage gain of the proposed converter is not very sensitive to coupling coefficient variations, and the ideal voltage gain relation for $k=1$ is as (14).

$$M_{CCM} = \frac{1+n}{(1-D)^2} \quad (14)$$

The $k=1$ is considered for analysis in the following sections. A comparison of the suggested converter’s voltage gain with other references at CCM mode for $n=2$ and $k=1$ is presented in Figure 8. This figure shows that the proposed topology presents higher voltage gain than other structures for a wide range of duty cycle values. Voltage stresses on power switches and diodes are as (15)–(19).

$$V_{SD} = V_{C1} + V_{C2} = \frac{V_i}{(1-D)^2} = \frac{V_o}{(1+n)} \quad (15)$$

$$V_{D1} = \frac{V_i}{1-D} \quad (16)$$

$$V_{D2} = \frac{D}{(1-D)^2} V_i \quad (17)$$

$$V_{D3} = \frac{V_i}{(1-D)^2} \quad (18)$$

$$V_{D4} \text{ and } V_{D5} = \frac{n}{(1-D)^2} V_i \quad (19)$$

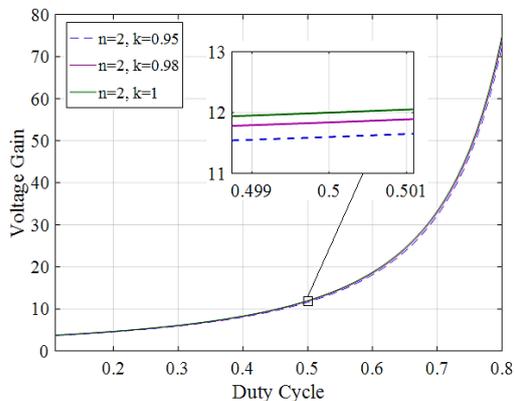


Figure 7. Voltage gain versus duty cycle at CCM operation for $n=2$ and different k

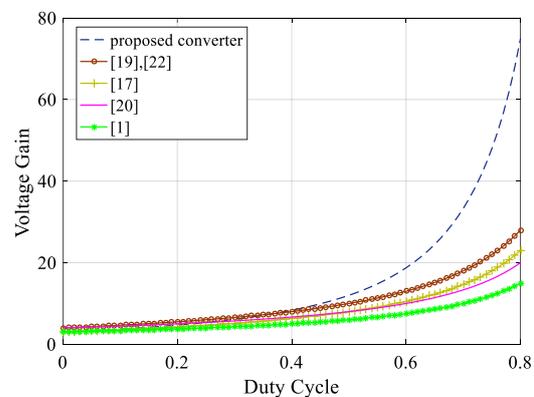


Figure 8. Voltage gain comparison of the suggested topology and other structures for $n=2$

3.2. Discontinuous mode

As discussed before, discontinuous operation consists of five modes. D is the period during which the current of the magnetizing inductor decreases from its peak value to zero. By considering only modes 1, 3, 4, and 5 and ignoring L_k , DCM analysis is simplified. From mode 1, the (20) are derived:

$$\begin{cases} V_{Lin} = V_i \\ V_{L1} = V_{C1} \\ V_{L2} = V_{C3} - V_{C2} \end{cases} \quad (20)$$

During modes 3, 4 and 5, V_{Lin} has a constant value for $(1-D)T_s$ interval and V_{L1} and V_{L2} are constant during $D'T_s$.

$$\begin{cases} V_{Lin} = V_i - V_{C1} \\ V_{L1} = -V_{C2} \\ V_{L2} = V_{C3} + V_{C1} - V_{C0} \\ V_{L2} = nV_{L1} \end{cases} \quad (21)$$

Applying volt-seconds balance principle on inductors L_{in} , L_1 and L_2 , equations are as follows:

$$V_{C1} = \frac{V_i}{(1-D)} \quad (22)$$

$$V_{C2} = \frac{D}{D'(1-D)} V_i \quad (23)$$

$$V_{C3} = \frac{D+D'n}{D'(1-D)} V_i \quad (24)$$

$$M_{DCM} = \frac{(1+n)(D+D')}{D'(1-D)} \quad (25)$$

Calculating D' from (25):

$$D' = \frac{(1+n).D}{M(1-D)-(1+n)} \quad (26)$$

where, M is M_{DCM} . Considering that ΔI_{Lm} is the maximum current value for magnetizing inductor and (22), the (27) is presented:

$$I_{Lmp} = \frac{V_{C1}}{L_m} DT_s = \frac{D.T_s}{L_m} \cdot \frac{V_{in}}{1-D} \quad (27)$$

where, I_{Lmp} is the maximum current of L_m during DCM. According to the fact that average current values for capacitors C_1 , C_2 , C_3 and C_0 are zero in one switching period, the (28) and (29) can be obtained.

$$\langle I_0 \rangle = \langle I_{D5} \rangle = \langle I_{D4} \rangle = \langle I_{D3} \rangle \quad (28)$$

$$\langle I_{D5} \rangle = \langle I_{C0} \rangle + \langle I_0 \rangle \quad (29)$$

It has to be mentioned that the load here is considered to be resistive. Calculating peak current of D_5 based on the current of magnetizing inductor from Figure 6 similar to the DCM approach of [4] and using (27) and (29), the following equations is derived:

$$\frac{1}{2} D' \frac{I_{Lmp}}{n+1} = 0 + I_0 \rightarrow \frac{1}{2} D' \frac{D.T_s.V_{in}}{L_m.(1-D).(n+1)} = \frac{V_o}{R} \quad (30)$$

Then, the normalized magnetizing inductor time constant is written as:

$$\tau_{Lm} = \frac{L_m}{R.T_s} = \frac{L_m.f_s}{R} \quad (31)$$

Replacing (26) in (30) and using (31), M_{DCM} is obtained as follows:

$$M_{DCM} = \frac{V_o}{V_i} = \frac{(1+n) + \sqrt{(1+n)^2 + \frac{2.D^2}{\tau_{Lm}}}}{2.(1-D)} \quad (32)$$

3.3. Boundary mode

The boundary area is the common region of continuous and discontinuous operating modes for the presented converter. Considering that the converter operates in boundary mode, by equalizing (14) and (32), τ_{LmB} constant is defined as (33).

$$\tau_{LmB} = \frac{D.(1-D)^2}{2.(1+n)^2} \quad (33)$$

Figure 9 shows the curve of τ_{LmB} versus duty cycle for the suggested converter. The proposed topology would operate in continuous mode if τ_{Lm} was greater than τ_{mB} . This figure proves that the proposed converter operates at CCM for a wide range of duty cycles. The minimum value for C_o based on the voltage ripple of the load can be derived as follows:

$$\begin{cases} V_{Co}(t_2) = \frac{1}{C_o} \int_{t_1}^{t_2} (-I_o) dt + V_{Co}(t_1) \\ I_o = \frac{V_o}{R} \\ t_2 - t_1 \cong DT_s \end{cases} \quad (34)$$

$$\Delta V_{Co} = \frac{V_o.D.T_s}{R.C_o} \rightarrow C_o = \frac{V_o.D.T_s}{R.\Delta V_{Co}} \quad (35)$$

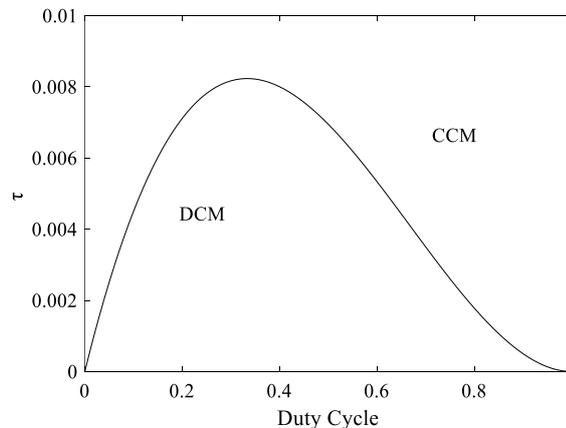


Figure 9. Boundary conduction mode condition of the presented topology for $n=2$

4. DYNAMIC PERFORMANCE OF PROPOSED CONVERTER

To show the dynamic performance of the suggested converter, a closed-loop voltage control based on a conventional PI controller is simulated, and results are presented in this section.

- In the first scenario, a step and sinusoidal disturbances are added to the input voltage. Figure 10(a) shows the step disturbance in the input voltage, and Figure 10(b) shows the output voltage. It can be seen from this figure that using the close-loop control system, well regulates the output voltage to the reference value. Figures 11(a) and 11(b) show sinusoidal disturbances of input voltage and output voltage, which are not affected by this disturbance.
- In the second scenario for evaluating the dynamic performance of the suggested converter, a step change in the reference value of the output voltage is considered. In this scenario, the input voltage is kept at 30 V, and the reference output voltage is changed from 330 to 250 V at 0.25 sec. Figures 12(a) and 12(b) show input and output voltage under the mentioned conditions. It can be seen from this figure that, using a closed-loop control system, the output voltage follows the changes in the reference voltage.

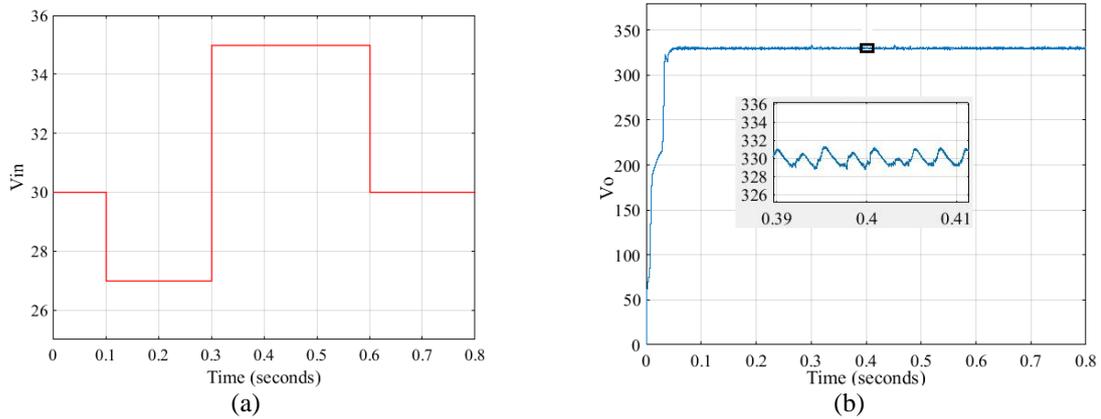


Figure 10. Output and input voltages under step disturbance: (a) input voltage and (b) output voltage

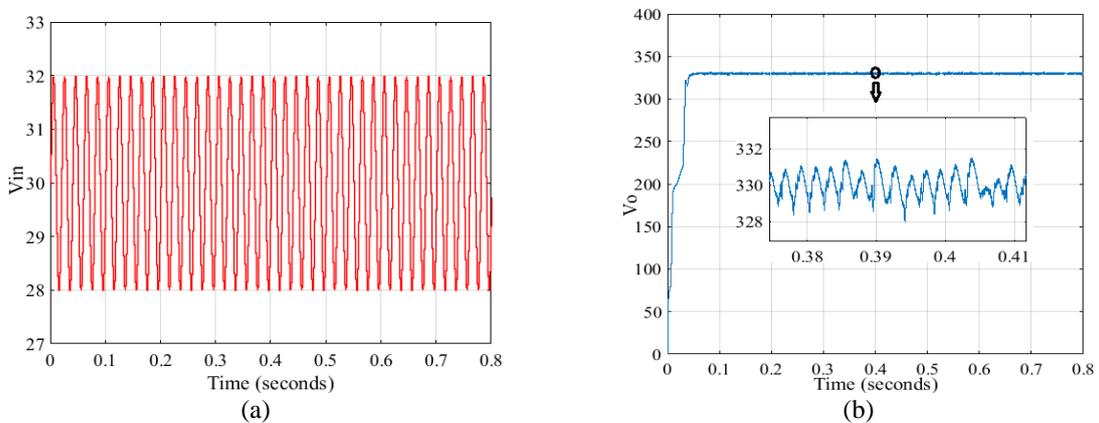


Figure 11. Output and input voltages under sinusoidal disturbance: (a) input voltage and (b) output voltage

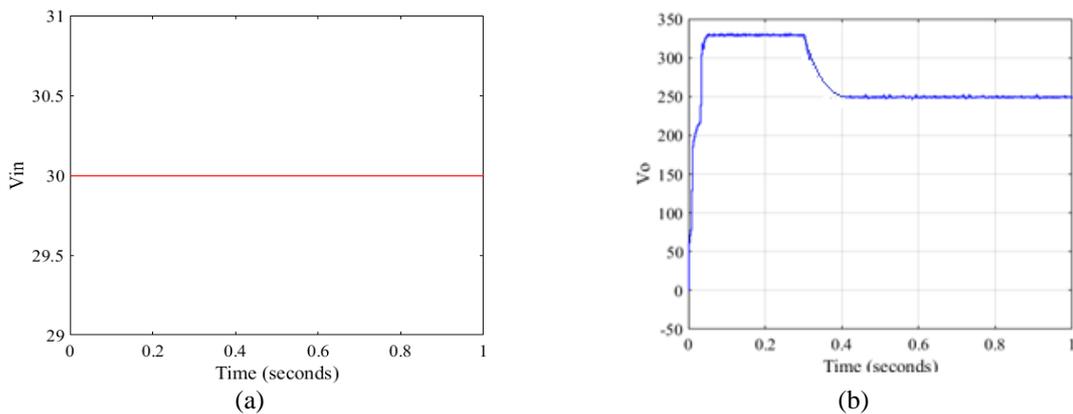


Figure 12. Output and input voltages under changing in reference value of output voltage: (a) input voltage and (b) output voltage

5. EXPERIMENTAL VALIDATION

To validate the operation of the proposed high-gain DC-DC converter, a 240-watt prototype is developed in the laboratory, and results are recorded. The converter operates in CCM, and the input voltage is considered to be 30 volts with a resistive load. Elements values and their characteristics for laboratory-implemented converters are presented in Table 1. Figure 13 shows the proposed converter prototype. The Arduino Mega 2560 board, based on an AVR microcontroller, is used for pulse generation purposes. A

HCPL A3120 MOSFET driver is implemented, which is highly capable of driving power switches in high-frequency conditions.

Table 1. Elements and characteristics of the proposed topology

Parameter	Value/Type
V_{in}	30 v
V_O	360 v
D	50%
f_s	30 kHz
D_1, D_2, D_3, D_4, D_5	STTH30R04W
S	IRFP264
Rated Power	240 W
L_{in}	220 μ H
L_m	90 μ H
n	2
C_1	100 μ F
C_2	10 μ F
C_3	47 μ F
C_4	220 μ F

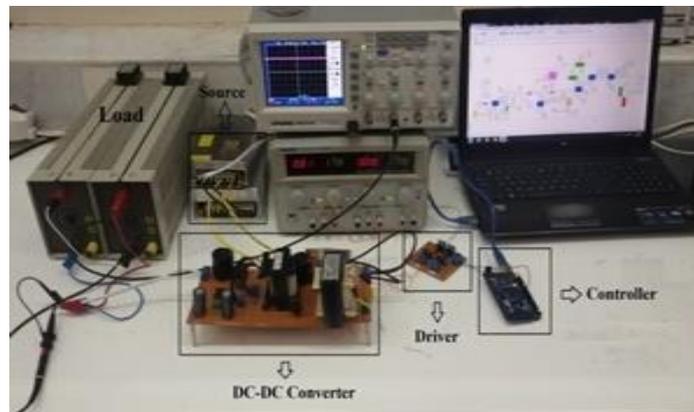


Figure 13. Proposed lab-scale test prototype

The steady-state analysis of the converter is validated through the laboratory prototype results. Figure 14(a) shows input and output voltages and proves the capability of converters in efficient high-gain voltage conversion. According to (11) and the given parameters in Table 1, it can be seen that the obtained output voltage in the laboratory prototype is almost the same as with the theoretical calculation. Figure 14(b) illustrates a gate-source signal (VGS) with a duty cycle of 50%. Figure 14(c) presents the input-side current, which is continuous with an acceptable ripple value. The nominal power of the prototype proposed converter is 240 watts. With a 30 V input voltage, the input current should be 8 A, and from (36) the ripple of the input current is equal to 2.2 A. The practical results are consistent with these calculations.

By replacing the parameter values of Table 1 in (3), following values can be concluded:

$$\Delta I_{Lin} = \frac{30 \times 0.5}{220 \times 10^{-6} \times 30000} \cong 2.2 \text{ A} \quad (36)$$

This equation shows that input current ripple is about 25% which is an acceptable ripple for high gain converters and it is significantly lower than the ripples proposed in recent literature. For example, in [1], [18], [19] and [22] the input current ripple is reported to be more than 60%.

Figures 14(d)–(f) show the voltages of the capacitors C_1 , C_2 , and C_3 , respectively, that are compatible with the theoretical results from (10)–(12). The presented experimental results show the validity of the theoretical analysis and the suitability of the proposed converter. Efficiencies are also recorded for the proposed converter in both simulations and experiments. Maximum efficiencies of 94.2% and 93.4% are recorded for simulations and experiments, respectively, which is a proper high value for non-soft switching high step-up converters. Figure 15 shows the efficiency curve of the converter based on output power variations.

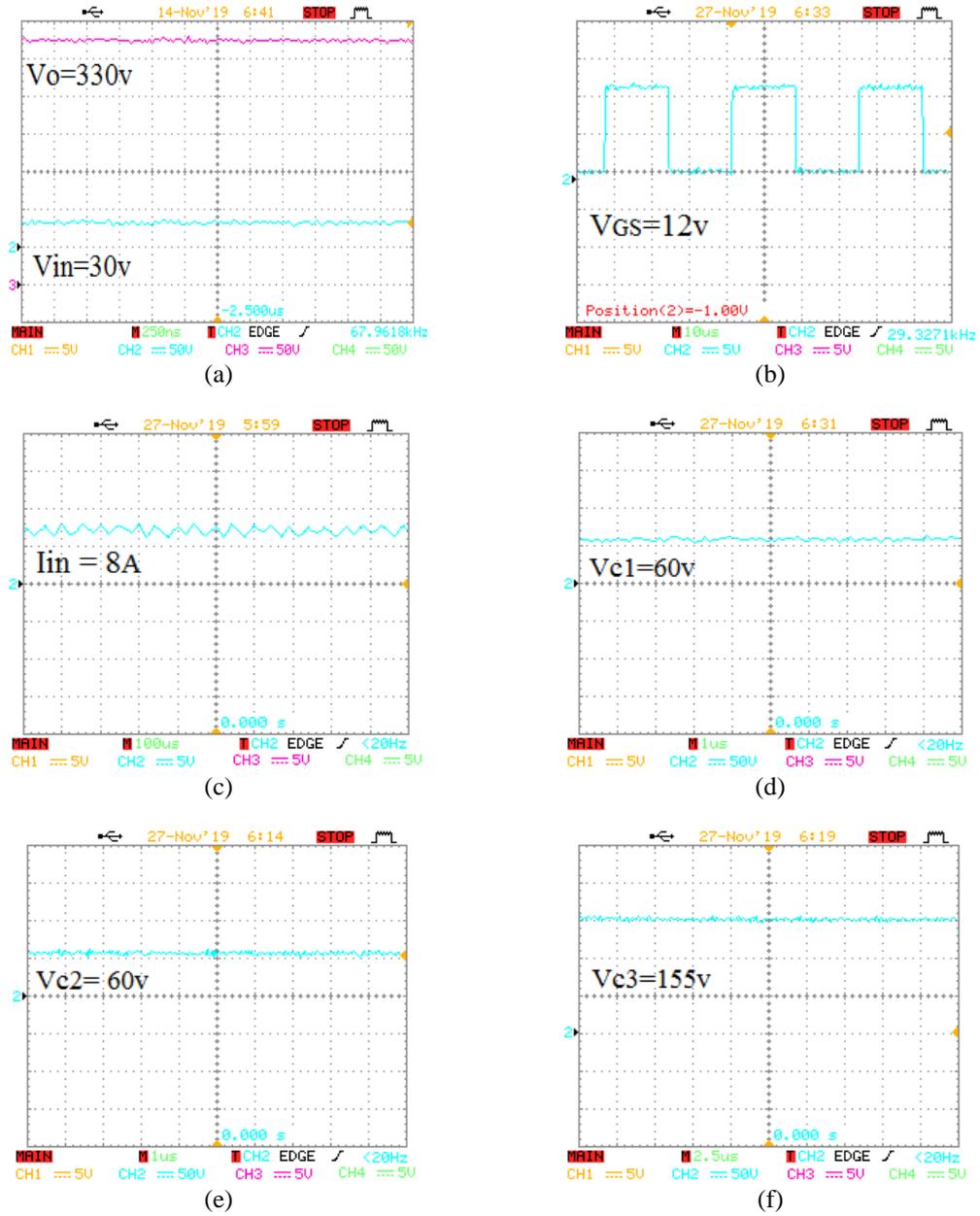


Figure 14. Experimental results for 240 W resistive load

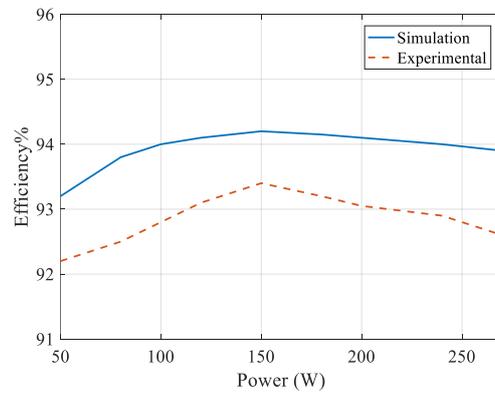


Figure 15. Efficiency versus output power

6. CONCLUSION

A high-gain, low-ripple input current DC-DC converter is presented in this paper, which is suitable for low-voltage applications like photovoltaic systems. Using coupled inductor technology in the proposed topology, high voltage levels became available with only an adjustment of the turn ratio and without an increment in duty cycle values that might lead to high voltage stress on the power switch. Continuous input current is guaranteed, which leads to low current stress at the input source and proper MPPT capability. The clamp circuit of the converter efficiently recovered the energy of the leakage inductor and reduced voltage stress on the power MOSFET; therefore, switches with lower resistance could be used. A 240 W prototype was tested to validate the operation of the presented converter, and maximum efficiencies of 94.2% and 93.4% were recorded for simulations and experiments, respectively. A proposed converter with proper operation and improved characteristics can be a suitable choice for low-voltage DC applications.

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