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A 27-MHz frequency shift keying wireless system resilient to in-band interference for wireless sensing applications

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ABSTRACT

A 27-MHz wireless system with binary frequency shift keying (BFSK) modulation at 400-kHz is reported. The receiver has been designed to handle in-band interference corrupting the BFSK signal with the use of complex filters and amplitude comparison method. The BFSK modulation is carried out with a voltage-controlled oscillator before up-converting with a 27-MHz local oscillator. The bipolar junction transistors (BJT-based) power amplifier with 30% efficiency pumps 220 mW into a spiral antenna. The inductive-degenerated low-noise amplifier with a voltage of more than 30 dB amplifies an incoming signal before feeding into a mixer for complex direct down conversion. With deliberate Gaussian interference injection, the minimum ratios between the signal with interference and the interference only at the distance of 2.5, 10 and 15 m are 3.3, 8.5 and 11.5 dB, respectively at a maximum data rate of 20 kbps. Without any interference included, the system can achieve a data rate of 40 kbps at the maximum transmission distance of 15 m. Conceptually agreed with the presented bit-error-rate (BER) analysis, the BER measurements with Gaussian and single-tone/two-tone in-band interferences also confirm superiority offered by the amplitude comparison method where the signal-to-noise ratio is at 1 dB for BER=10^{-3} at 10 kbps (10 dB better than the phase detection counterpart).

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1. INTRODUCTION

The frequency shift keying (FSK) modulation [1]–[4] plays a significant role in wireless communication applications for the present and future technological demands [5]–[9], [10]–[13]. In wireless sensor networks, millions of devices and sensors are seamlessly connected together over limited spectral bandwidth. The restricted spectrum bandwidth could practically make interference among these devices unavoidable. To avoid severe interference from an adjacent-channel image signal and to maintain receiver's power consumption at the minimum without circuit complexity, a direction-conversion or zero-intermediate frequency (zero-IF) architecture is usually selected in modern wireless receiver [14]–[16]. Although this direct-conversion receiver structure can effectively remove such image signal, an in-band interference still poses a major design challenge. This is a quite difficult scenario where the wanted and undesired signals are sitting inside the same frequency band and they cannot be separated by means of simple filtering.

In order to withstand the in-band interference without any complicate coding and multiple-access methods, a simple FSK modulation can be employed for low-cost wireless sensor nodes since its frequency-division nature (i.e. the modulated carrier signal sits at different places on the spectrum according to the information values) could help combat the interference [13], [17]–[22]. More specifically, in the case

of FSK modulation with a direct-conversion receiver, a phase comparison method has long been a popular choice as a data-bit extraction part of the FSK demodulation process owing to its simplicity [23]–[26]. This phase comparison technique usually employs a digital logic circuit. A small down-converted signal needs to be amplified and limited for logic operation. This thus makes the phase detecting method prone to interference causing a high bit-error rate unless special techniques are employed [24]–[26].

A key feature of the direct-conversion binary frequency shift keying (BFSK) receiver explored in this work is its ability to handle in-band interference when an appropriate demodulation and data bit extraction technique has been exercised. Specifically, an amplitude comparison technique after complex filtering is investigated and compared with a well-established phase detection method. With a mathematical analysis on bit-error rate (BER) comparing to the phase detection technique, the frequency-energy conversion counterpart co-operating with complex filtering and amplitude comparison process shows superior tolerant capability to a significant level of in-band interference. A 27 MHz wireless system concept has been implemented and tested with low-cost discrete components to demonstrate this interference resilient property of the studied FSK receiver. BFSK modulator, power amplifier (PA), low-noise amplifier (LNA), up and down conversion mixers as well as the core BFSK demodulators have been constructed from easy-to-find integrated-circuit and semiconductor components to illustrate promising versatility of the proposed architecture. The system has been thoroughly tested for both wireline and wireless connections where in-band interferences (Gaussian, single-tone and two-tone) has been injected at the intermediate frequency (IF) band on the transmitter end. BER measurements and extensive experimentation under various interference conditions strongly suggested that the proposed receiver system significantly outperforms the phase-detection system but with not much extra cost on circuit complexity.

A receiver system architecture and proposed method are reviewed in section 2 where bit-error rate analysis has also been carried out to compare the well-known phase detection technique to its amplitude comparison method. The important circuit building blocks employed in the proposed system are explained in section 3. Various experimentation methods and measured results are described and summarized in section 4 before concluding the study in section 5.

2. SYSTEM ARCHITECTURE DESIGN AND PROPOSED METHOD

A conceptual spectrum diagram for direct down-converting BFSK signal from a radio frequency (RF) band to 0 Hz (zero-IF) before extracting the digital data bits is depicted in Figure 1(a). The direct down conversion is done with a complex local-oscillator (LO) signal, $S_{LORx}(t)=A_{LO}\exp(j\omega_{LORx}t)$. This renders a complex binary signal around $+\omega_1$ and $-\omega_0$ representing bits "1" and "0", respectively (typically, $|\omega_1|=|-\omega_0|=\omega$) as shown as the signal $S_{ZIF}(t)$ at the bottom of Figure 1(a), so the main complex signal for the bit data will be

$$S_{ZIF} = A\,exp(+j\omega_1 t) \text{ for bit "1"} \quad (1a)$$

$$S_{ZIF} = A\,exp(-j\omega_0 t) \text{for bit "0"} \quad (1b)$$

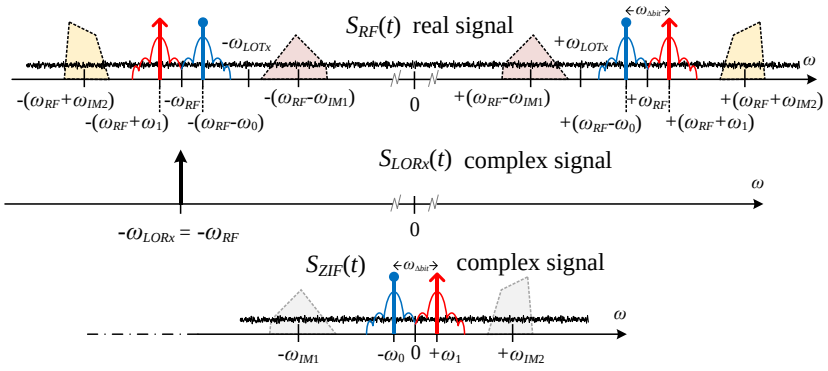
By focusing only on the data signals of $S_{ZIF}(t)$ in time domain with all the images and interference removed for simplicity as illustrated on left of Figure 1(b) which is corresponding to the "1" (red) and "0" (blue) bit spectrum, the data bit can be directly extracted by phase comparison between *I* and *Q* signal parts because of the different phase shift during different data bits [23]–[26]. Alternatively, this $S_{ZIF}(t)$ can be passed on to two complex filters with their center frequencies at $+\omega_1$ and $-\omega_0$, where the data bits can be recovered by amplitude comparison since the complex filter would only pass a complex signal on one side of 0 Hz [27], [28]. In this work both bit extraction techniques are employed and compared under deliberate in-band interference injection. The 27 MHz FSK wireless radio transmission architecture is illustrated in Figure 2 where Figures 2(a) and 2(b) illustrates the transmitter and the receiver, respectively.

2.1. Transmitter

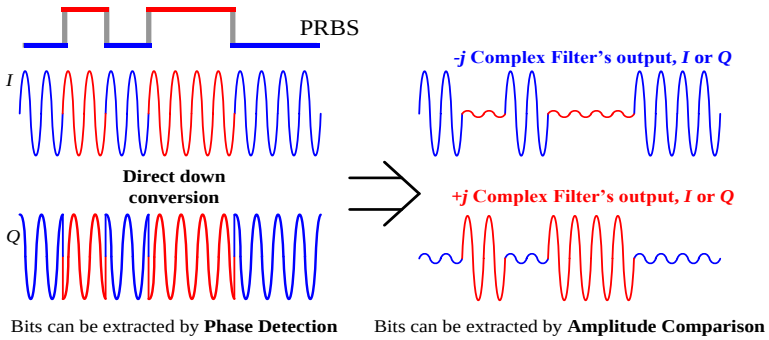
The 1-bit binary pseudo-random binary sequence (PRBS) signal modulates a 400-kHz carrier signal with a voltage-controlled oscillator before being up-converted by 27-MHz with a Gilbert mixer. The RF signal power (centered at 27.4 MHz) is boosted using a power amplifier to drive an antenna for RF electromagnetic radiation. A wideband Gaussian noise can be deliberately added to the FSK signal as interference for system evaluation.

2.2. Receiver

An in-coming RF signal from an antenna is voltage amplified by a low-noise amplifier (LNA) before feeding into a down-conversion mixer to perform a direct down conversion with a complex local oscillator (LO) signal (27.4 MHz) to obtain the complex signal $S_{ZIF}(t)$ as in Figure 1(a). This $S_{ZIF}(t)$ is then channeled into two different paths: i) being filtered by two complex filters (+*j*/-*j* complex filters) whose center frequencies sit at +/-ω rad/s on the opposite side of 0 Hz prior to detecting the signal amplitudes and recovering data bits by amplitude comparison [also known as a frequency-to-energy conversion technique], and ii) being filtered by real lowpass filters before performing bit recovery by phase detection using a D flip-flop. The phase comparison technique looks simpler than its amplitude comparison counterpart due to less circuit complexity. However, with a high level of in-band interference in the system, phase detection technique can be much more severely disturbed and rendering incorrect data recovery. The reason behind this comes from the fact that the amplitude comparison technique takes signals from two complex filters where the impact from any interference appearing at both complex filters can be greatly reduced by comparison process. But in the case of phase detection, the signal has to be amplified and limited before entering a phase detector such as a D flip-flop, this limiting step can be highly erroneous when interference is significant-especially, with an *in-band* random interference where no simple kind of analog filter can be employed to remove it.



(a)



(b)

Figure 1. Conceptual signal diagram for direct-conversion (zero-IF) receiver and two data extraction methods (a) spectrum diagram for direct down conversion by a complex *LO* signal and (b) the time-domain complex $S_{ZIF}(t)$ signals in (a) after direct down conversion (left) and after complex filtering (right)

2.3. Bit-error-rate analysis and comparison for the two detection methods

A simplified BER analysis comparing between the two techniques in the subsequent section will be carried out to verify the aforementioned assumption. In this simple analysis it is assumed that the in-band interference gets through the complex filters and the lowpass filters in both types of bit detection methods. Due to a number of circuit building blocks inside the presented receiver/demodulator architectures, the following BER analysis only serves for a comparison purpose between two-bit recovery techniques and it does not precisely represent the actual BER of the really complicated demodulator structures or the actual wireless channel.

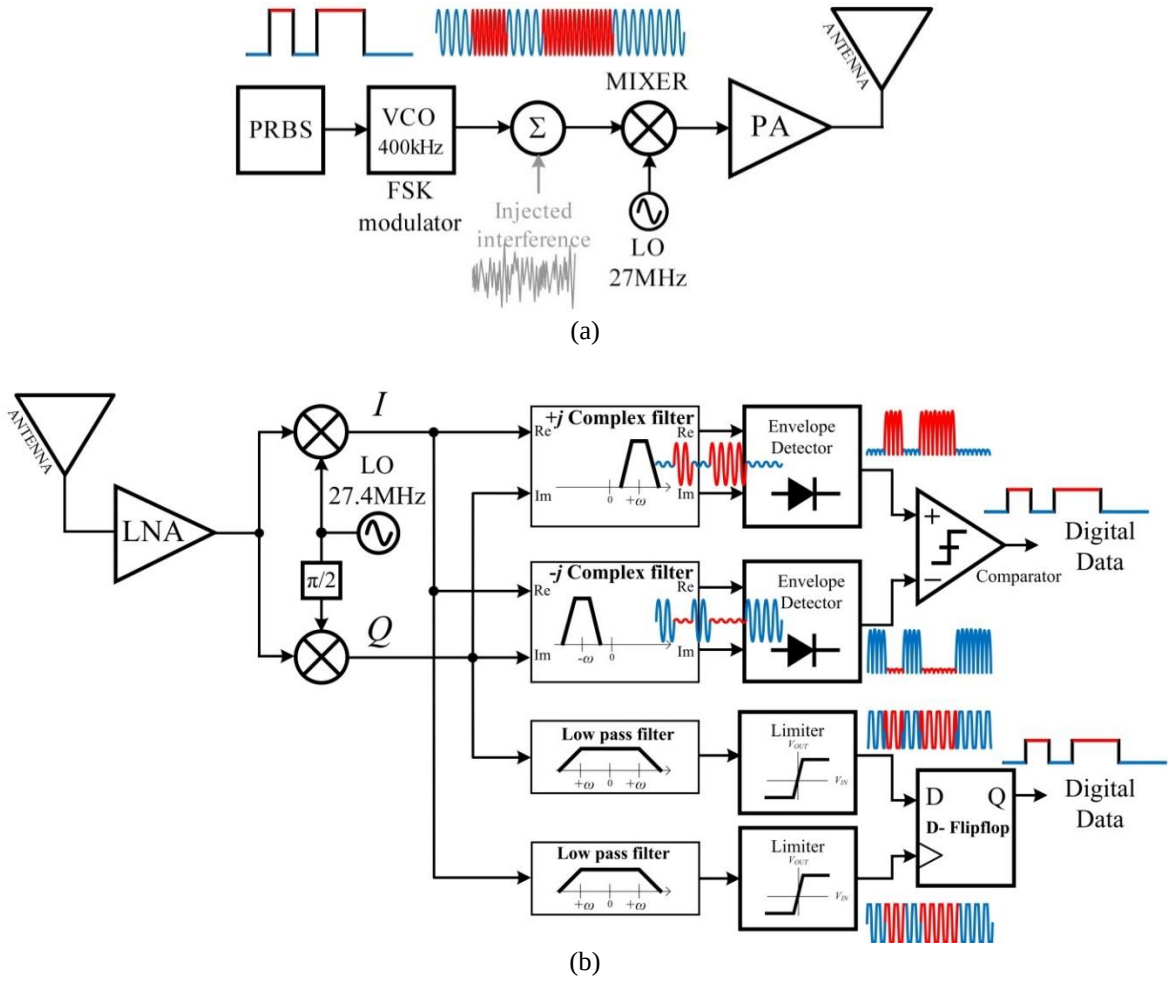


Figure 2. The FSK wireless system architecture under investigation, (a) transmitter and (b) receiver with two types of data extraction for comparison

2.3.1. Phase detection with a D flip-flop (DFF) after lowpass filtering

To simplify the BER analysis, as illustrated in Figure 3 it is assumed that the Gaussian interference disturbs only the signal received from the *I* path at DFF's data terminal, SI_D as in Figures 3(a) and 3(b). While the signal from the *Q* path entering the DFF's clock node, SQ_{CLK} is clean, i.e., the source of bit error comes from SI_D only. Thus this *optimistic* BER analysis of the phase detection technique is simply an issue of detecting error bits from the signal SI_D which is a fairly standard BER calculation [29]. For a single supply system, the logic signal switches between 0 and V_A, the probability density function (*pdf*) of the Gaussian-interfered S_{ID} is as depicted in Figure 4 and the BER of the phase detection technique, BER_{PD} can be expressed as [29].

$$\begin{aligned} BER_{PD} &= P_{0\to1} + P_{1\to0} = 2P_{0\to1} = 2\int_{V_{th}}^{\infty} P_{SI_D@"0"}(u)du \\ &= 2\int_{V_{Th}=0.5V_A}^{\infty} \frac{1}{2\sigma_n\sqrt{2\pi}} exp\left(\frac{-(u)^2}{2\sigma_n^2}\right) du \\ &= \int_{V_{Th}/\sigma_n}^{\infty} \frac{1}{\sqrt{2\pi}} exp\left(\frac{-z^2}{2}\right) dz = Q\left(\frac{V_{Th}}{\sigma_n}\right) = Q\left(\frac{0.5V_A}{\sigma_n}\right) \end{aligned} \quad (2)$$

Where σ_n is the interference's *rms* voltage where V_{Th} (=V_A/2) is the threshold voltage level for logic decision. $Q(x)$ is widely known as a *Q* function and its value can only be found by approximation [30].

2.3.2. Amplitude comparison after complex filtering

For simplification, it is again assumed that the uncorrelated Gaussian interferences are present at both inputs of the comparator S_{CP} and S_{CN} after complex filtering and amplitude detection process as in

Figure 5. Figure 5(a) shows how interferences enter the comparator while Figure 5(b) displays disturbed time-domain signals. The first two graphs in Figure 6 show the probability density functions (*pdf*), $P_{SCP}(x)$ and $P_{SCN}(x)$ of the signals S_{CP} and S_{CN} at the comparator's inputs. For a single supply system, it is assumed that the pre-amplitude-detected signal swings between V_A and 0 rendering the ideal amplitude-detected/rectified voltage level at αV_A and 0, where α is a rectification factor with $0<\alpha\leq 1$. The comparator mathematically performs a subtracting task between S_{CP} and S_{CN} before limiting the difference, and if the difference (S_{CP}-S_{CN}) is greater (or lower) than zero, this implies that bit "1" (or "0") would be detected. Therefore, the BER can be computed from the *pdf* of S_{CP}-S_{CN}, i.e., $P_{(S_{CP}-S_{CN})}$ which can be seen as the convolution of $P_{S_{CP}}(x)$ and $P_{(-S_{CN})}(x)$) (the *pdf* of the $-S_{CN}$ signal). Using the proof developed in [31], [32] if $P_{S_{CP}}(x)$ and $P_{S_{CN}}(x)$ are

$$P_{S_{CP}@"1"}(x) = \frac{1}{2\sigma_{nCP}\sqrt{2\pi}} exp\left(\frac{-(x-\alpha V_A)^2}{2\sigma_{nCP}^2}\right) \tag{3}$$

and

$$P_{S_{CN}@"1"}(x) = \frac{1}{2\sigma_{nCN}\sqrt{2\pi}} exp\left(\frac{-(x)^2}{2\sigma_{nCN}^2}\right) \tag{4}$$

when bit "1" is sent, $P_{(SCP-SCN)}$ can be expressed as

$$P_{(S_{CP}-S_{CN})@"1"}(x) = \frac{1}{4\sqrt{2\pi(\sigma_{nCP}^2+\sigma_{nCN}^2)}} exp\left(\frac{-(x-\alpha V_A)^2}{2(\sigma_{nCP}^2+\sigma_{nCN}^2)}\right) \tag{5a}$$

Similarly, when bit "0" is sent, $P_{(SCP-SCN)}$ can be expressed as

$$P_{(S_{CP}-S_{CN})@"0"}(x) = \frac{1}{4\sqrt{2\pi(\sigma_{nCP}^2+\sigma_{nCN}^2)}} exp\left(\frac{-(x-(-\alpha V_A))^2}{2(\sigma_{nCP}^2+\sigma_{nCN}^2)}\right) \tag{5b}$$

These $P_{(S_{CP}-S_{CN})@"1"}(x)$ and $P_{(S_{CP}-S_{CN})@"1"}(x)$ are also shown as the last graph in Figure 6. The BER is the total probability of the error bit detection, i.e.,

$$\begin{aligned} BER &= P_{0\to1} + P_{1\to0} = 2P_{1\to0} = 2P_{0\to1} = 2\int_{-\infty}^{0} P_{(S_{CP}-S_{CN})@"1"}(u)du \\ &= 2\int_{0}^{-\infty} P_{(S_{CP}-S_{CN})@"0"}(u)du \\ &= 2\int_{0}^{-\infty} \frac{1}{4\sqrt{2\pi(\sigma_{nCP}^2+\sigma_{nCN}^2)}} exp\left(\frac{-(u+\alpha V_A)^2}{2(\sigma_{nCP}^2+\sigma_{nCN}^2)}\right) du \end{aligned} \tag{6}$$

For simplicity, $\sigma_{nCP} = \sigma_{nCN} = \sigma_n$ and the BER of the amplitude detection technique, BER_{AD} is reduced to

$$BER_{AD} = \frac{1}{2}\int_{0}^{-\infty} \frac{1}{\sqrt{2}\sigma_n\sqrt{2\pi}} exp\left(\frac{-(u+\alpha V_A)^2}{2(2\sigma_n^2)}\right) du = \frac{1}{2}\int_{\alpha V_A/\sqrt{2}\sigma_n}^{-\infty} \frac{1}{\sqrt{2\pi}} exp\left(\frac{-(z)^2}{2}\right) dz = \frac{1}{2}Q\left(\frac{\alpha V_A}{\sqrt{2}\sigma_n}\right) \tag{7}$$

Specifically, if the amplitude detection process can manage $1/\sqrt{2}$ of V_A, i.e. $\alpha=1/\sqrt{2}$, then $BER_{AD}=0.5Q(0.5V_A/\sigma_n)$ which is still an improvement by a factor of two as compared to the phase detection technique. Noting that under a single supply system with *square*-wave signaling, the ratio $(0.5V_A/\sigma_n)$ is technically a signal to noise ratio (SNR), but if the signal under consideration is *sinusoidal*, the $(0.5V_A/\sigma_n)$ is instead equal to $\sqrt{2}SNR$. Comparison plot of BER as a function of SNR between BER_{PD} and BER_{AD} for a square-wave signaling scenario with $\alpha=1$ are illustrated in Figure 7. It is important to note that the SNR under consideration in these analyses is at the inputs of bit extraction circuitries (a comparator or a phase detector) and not at the actual input of the demodulator. Moreover, in the presented BER analysis, correlation of the noise/interference signals at the comparator's and the phase detector's inputs have not been taken into account. However, these simple BER graphs can be used to serve for a comparison purpose between the two-bit extraction techniques. If the interferences at the comparator's inputs are correlated (they actually are, to a certain extent), the BER graphs would definitely be better than those in Figure 7.

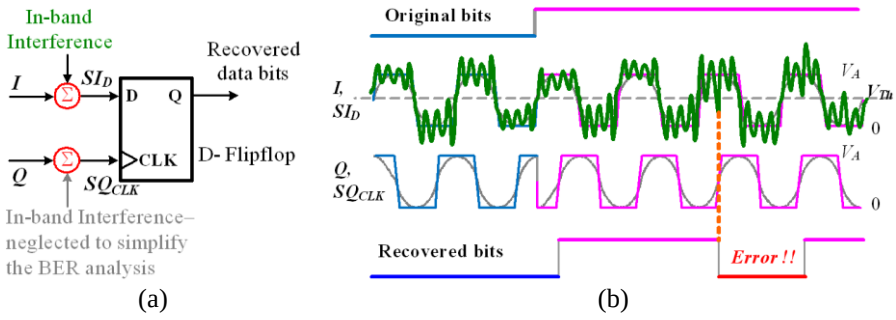


Figure 3. In-band interference scenario for BER calculation in the BFSK demodulation with a phase-detection technique with a *D* flip-flop as a phase detector, (a) interference is present only at DFF's data terminal and (b) occurrence of the error

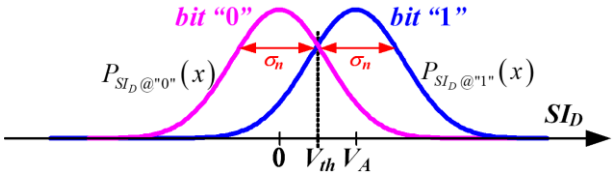


Figure 4. *Pdf* of the signal at the DFF's data terminal, P_{SID} for BER calculation in the BFSK phase-detection system

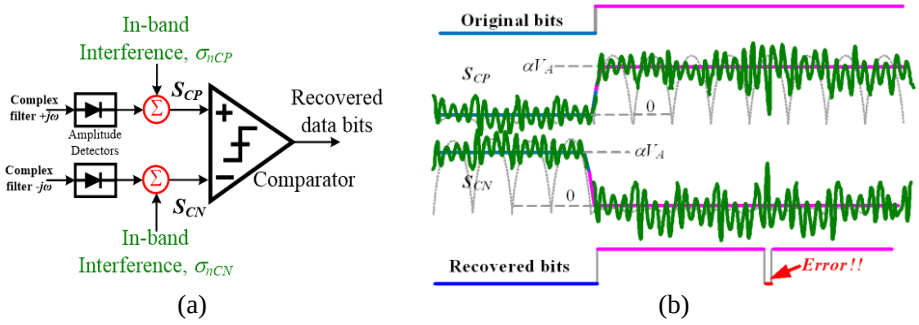


Figure 5. In-band interference scenario for BER calculation in the BFSK demodulation with amplitude comparison, (a) the uncorrelated interference is present at both of the comparator's input terminals, (b) occurrence of the error

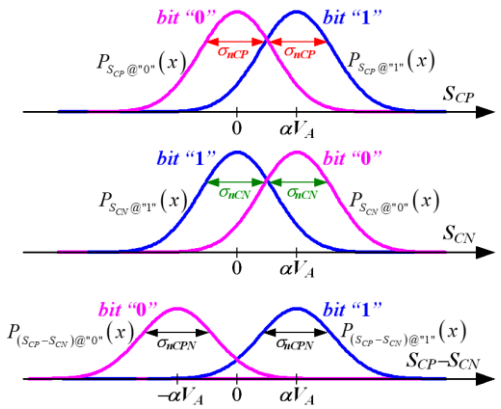


Figure 6. *Pdf*'s of the signals at the comparator's inputs, P_{SCP} and P_{SCN} and that of the corresponding difference, $P_{(SCP–SCN)}$

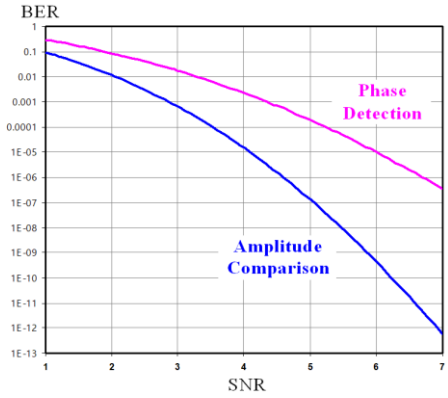


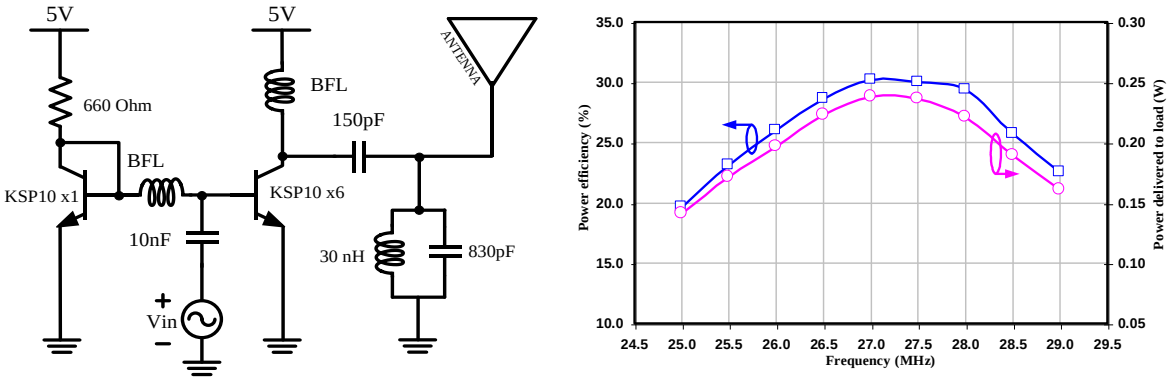
Figure 7. Calculated BER comparison between the two bit extraction techniques in the BFSK demodulator

3. CIRCUIT BUILDING BLOCKS

Various low-cost, off-the-shelf integrated circuits have been employed for implementing the wireless system namely, mixer (MC1496), voltage comparator (LM339), limiter (74HC04), D flip-flop (74LS74). The VCO from 74HCT4046 is employed to generate a BFSK signal around 400-kHz carrier frequency with deviation of +/-50kHz for "1"/"0" bits, i.e. $|\omega_1|=|-\omega_0|=\omega$=50 kHz in Figures 1 and 2. Important circuit schematics with their performances are illustrated in Figures 8 and 9.

3.1. A power amplifier (PA)

For simplicity, a class-A PA in Figure 8(a) is employed [15]. The main bipolar junction transistors (BJT) is biased with a current mirror to allow a large V_{ce} voltage swing with the cost of PA's power efficiency (PE) wasted in the current mirror. In this work, a discrete KSP10 is used for the BJT. The antenna impedance is transformed to 25 Ω (instead of 50 Ω) for the PA's output load so that more power can be delivered to the antenna due to a limited voltage swing (ideally at $2V_{CC}$ peak-to-peak). Assuming a sinusoidal voltage swing at the load, the ideal maximum power delivered to the load R_L is $V^2_{CC}/2R_L$. The PA's efficiency and maximum output power is plot against input frequency in Figure 8(b). At mid-band, the maximum power of 240 mW has been obtained with the corresponding PE of 30%. The PA drives a spiral antenna which has been implemented on the FR-4 printed circuit board (PCB) and optimized for 27.4 MHz narrow-band operation.



(a) (b)

Figure 8. A 27-MHz class-A power amplifier, (a) schematic and (b) performance

3.2. Low-noise amplifier (LNA)

A class-A inductive degenerated low-noise amplifier of Figure 9(a) is employed with KSP10 [15], [16]. The LNA's s-parameters s_{11} and s_{21} with respect to a 50 Ω reference system is shown in Figures 9(b) and 9(c), respectively. The s_{11} of -10 dB widely extends from 15 to 40 MHz well covering the operation for this wireless transmission system. The voltage gain is also measured as depicted in Figure 9(d)

with the quadrature down-conversion mixer's input attached as a load. The peak voltage gain of over 33 dB has been achieved.

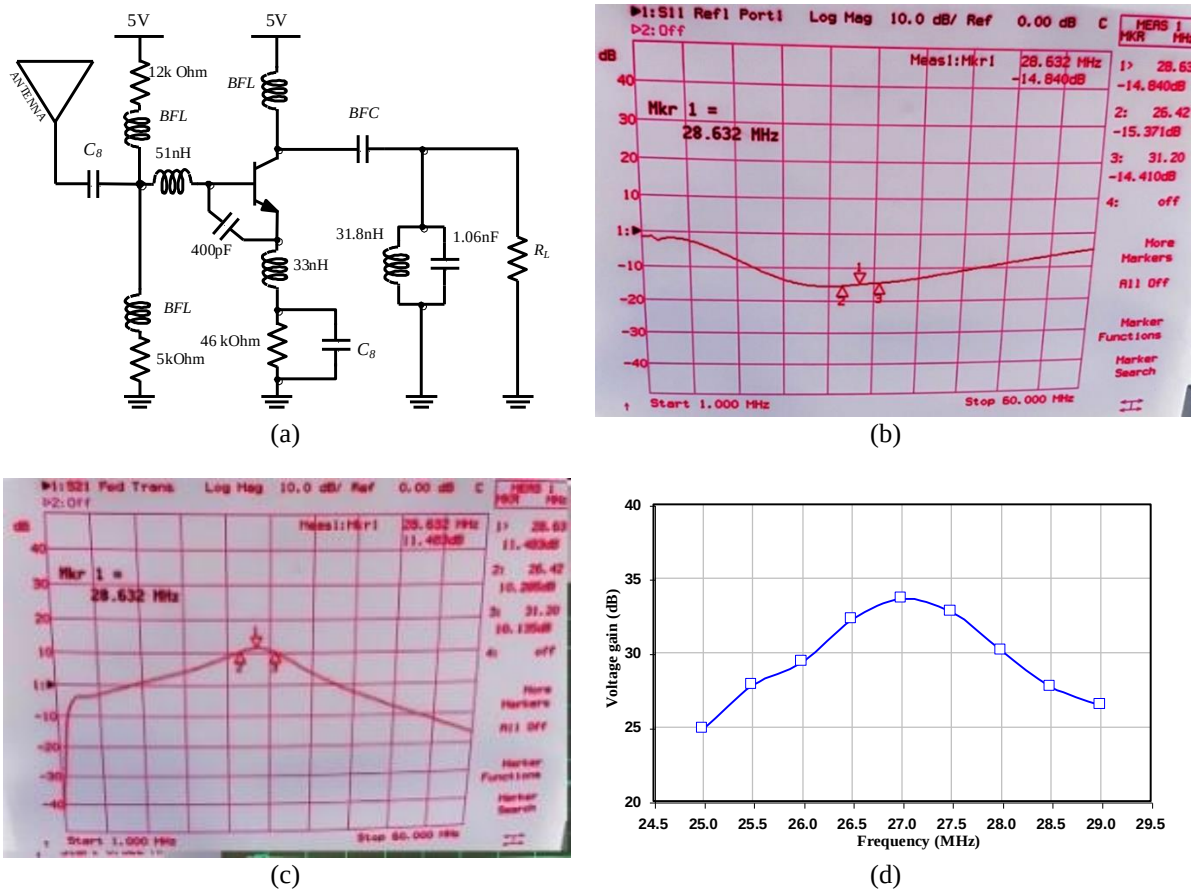


Figure 9. A 27-MHz low-noise amplifier, (a) schematic, (b) s_{11}, (c) s_{21}, (d) LNA's voltage gain

3.3. A polyphase filter and an envelope detector

A 3rd-order *RC* polyphase filters as shown in Figure 10 [33], [34] has been used for complex filtering followed by a simple 2nd-order *RC* lowpass filter in the receiver as part of the amplitude comparison technique for data bit extraction. Note also that a differential 5th-order *RC* passive lowpass filter has been used for the phase detection method. A BJT-based amplitude detector circuit in Figure 11 (developed from [35], [36]) has been used for amplitude detection with a single supply of 5 V. Discrete transistors BC547 and BC558 have been employed in this work.

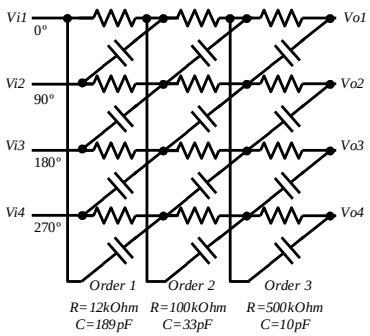


Figure 10. A 3rd-order *RC* polyphase filter as a complex filter

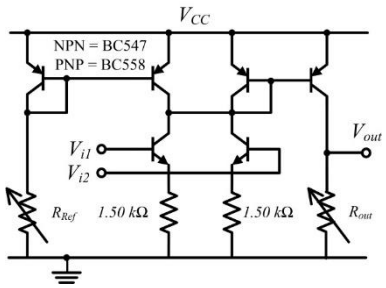


Figure 11. A BJT-based amplitude detector circuit

4. EXPERIMENTATION, RESULTS AND DISCUSSION

The complete system has been tested for both wire-line and wireless setups. The two aforementioned bit recovery techniques have been extensively compared. Measured results are described here.

4.1. Wire-line system test

Without the PA and the LNA involved, the output of the Tx's up-conversion mixer has been directly connected to the input of the Rx's down-conversion mixer. The results in time-domain are shown in Figures 12(a) and (b) and 13(a) and (b). In Figure 12, with no interference added to the modulated signal, both bit extraction techniques are working correctly where the phase detection technique does win on the basis of system simplicity and slightly lower power consumption.

To test interference resilience of the system, Gaussian noise has been deliberately added to the BFSK signal in front of the up-conversion mixer as indicated in Figure 12(a). This interference (together with the BFSK carrier) is also translated to be well inside the RF transmission band around 27.4 MHz. The results are as illustrated in Figure 13 with *in-band* interference at a significant level, the amplitude comparison technique with two complex filters can still operate correctly while its phase detection counterpart fails and continuously produced erroneous recovered bits. On the right side of Figure 13(a), we can see that the phase shift between the *I*/*Q* signals have been severely disturbed and this leads to incorrect bit recovery. It is important to note that the injected interference with frequency around 400±50 kHz (in-band) severely degrades bit extraction functionality by the phase detection method.

4.2. Wireless system test

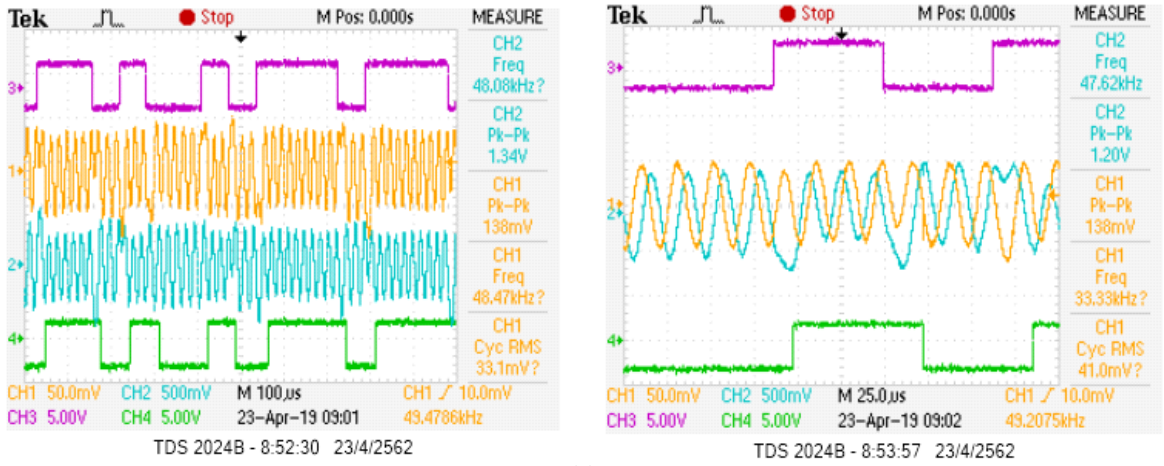
The transmitter, T_x and the receiver, R_x are separated by some physical distance with a clear line of sight as shown in Figure 14(a). The double-sideband spectrum at the power amplifier's input is depicted in Figure 14(b). The lower sideband signal and the 27-MHz *LO* leakage are clearly visible. These unwanted signals will not be strongly suppressed by the PA and LNA due to their rather low-quality factors. However, this will not be a serious issue owing to the direct-conversion receiver architecture where these undesired out-of-band interference can be easily removed by the baseband real lowpass filters or the complex filters.

Figure 15 demonstrates the operation at a distance of 10 meters with and without interference as shown in Figures 15(a) and (b) are from phase and amplitude detections, respectively. Both bit recovery techniques can perform correctly under low interference level as shown on the left side of Figures 15(a) and 15(b). On the right-hand side, the figures show how the high in-band interference level can severely corrupt the data extraction process using phase detection while the amplitude comparison method after the two complex filters can still function correctly. The result suggests that a smart receiver could alternately select an appropriate bit recovery method according to the present interference level so that trade-off between bit-error rate (BER) and power consumption can be well balanced.

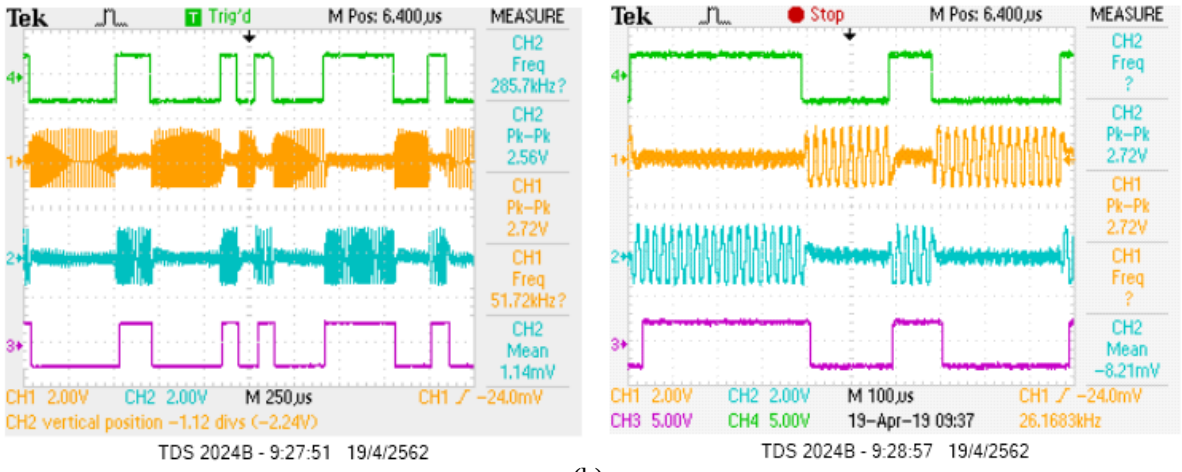
The minimum *Corrupted* signal-to-in-band *interference+noise* ratio (*c*S*ib*INR)-measured at the outputs of the complex filters, is the smallest ratio between power of the modulated signal corrupted by the *interference+noise*, $P_{Sig\pm inf\_noi}$ and power of the in-band *interference+noise* without the modulated signal, P_{ibinf_noi}, that allows the receiver with the complex-signal amplitude-comparison technique still perform correctly at a 20-kbps data rate while its phase detection counterpart practically fails, i.e., this *c*S*ib*INR can be expressed by (18).

$$cSibINR = \frac{P_{S\pm inf\_noi}}{P_{ibinf\_noi}} \quad (8)$$

Figure 13(b) indicates how *c*S*ib*INR of the complex-signal amplitude-comparison technique can be measured for a wire-line test. From the experiment, the phase detection technique always fails at these minimum *c*S*ib*INR levels recorded for the amplitude comparison technique. This result confirms its inferiority under a highly interfered environment. Plots of the received power level measured at the LNA's input and the minimum *c*S*ib*INR against the transmission distance is shown in Figure 16. Figure 16(a) shows the LNA's input power while Figure 16(b) illustrates the minimum *c*S*ib*INR figures.



(a)

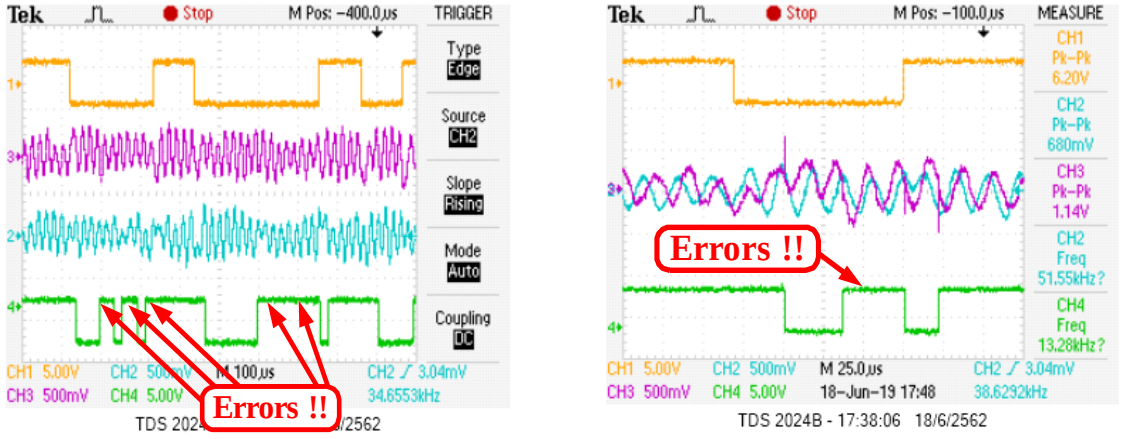


(b)

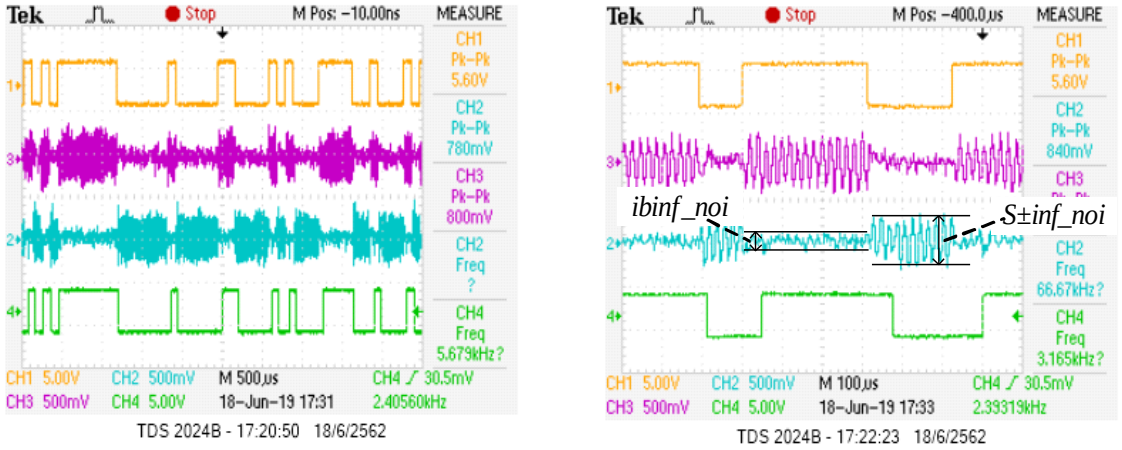
Figure 12. Wire-line system test without any interference, (*I*/*Q* phase detection using D flipflop (Ch2=*Q*, Ch1=*I*, Ch3=original data, Ch4=recovered data), (b) amplitude comparison (Ch1=-*j*CmplxFltr, Ch2=+*j*CmplxFltr, Ch4=original data, Ch3=recovered data)

4.3. Bit-error rate measurement

The BER has been measured with a wire-line connection setup where the transmitter is directly connected to the receiver i.e., the power amplifier, low-noise amplifier and antennae have been omitted. The received data bits have been retimed, digitized and compared with its transmitted counterpart by mean of digital logic processing on a field-programmable gate array (FPGA) (Xilinx Zybo zynq 7000 [37]). The results are as depicted in Figure 17 for both methods of bit extraction at 5 k, 10 k, 20 kbps. Noting that the signal-to-noise ratio (SNR) in this graph has been measured at the input of the receiver/demodulator (the receiver mixer's input)-not at the comparator or the phase detector's inputs as considered for the BER analysis in section 2.3. It is obvious that the amplitude-detection method offers much superior performance over its phase-detection counterpart (as theoretically predicted by the calculations in Figure 7) where the SNR is at 1 dB for BER=10^{-3} at 10 kbps (10 dB better than the phase detection counterpart).

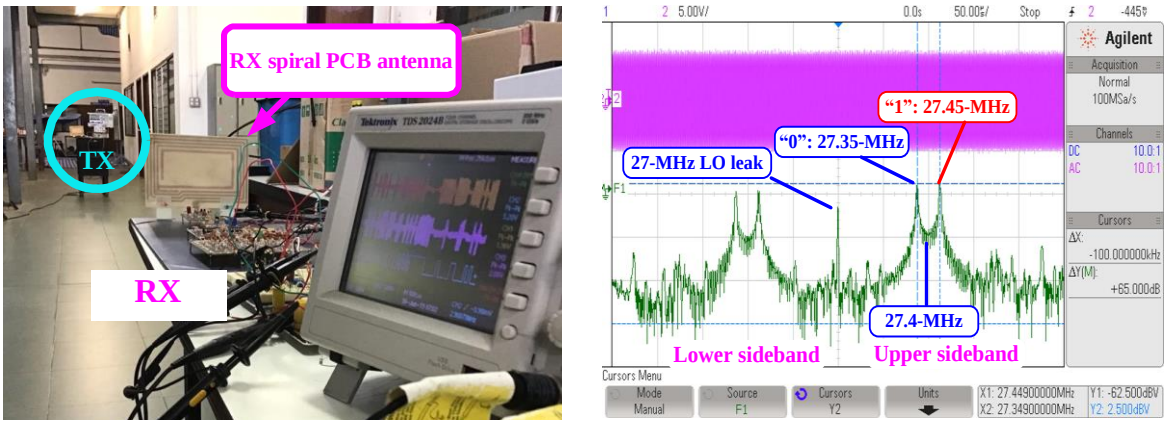


(a)



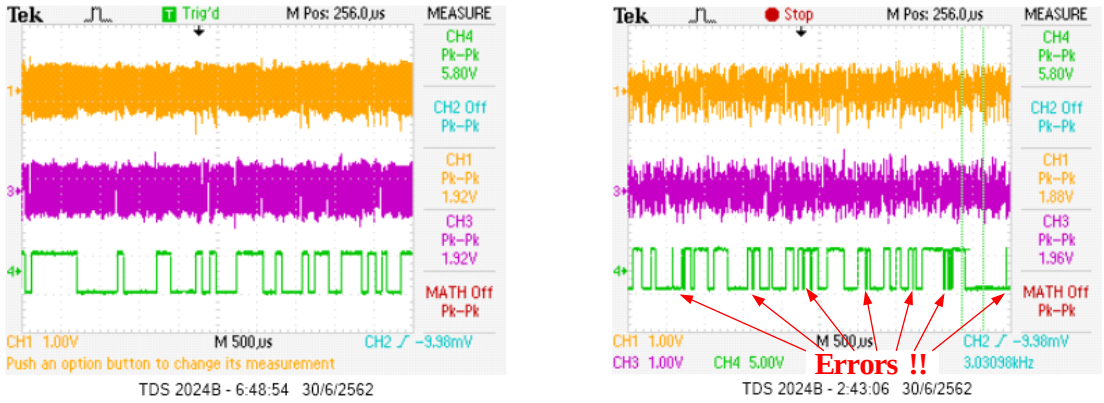
(b)

Figure 13. Wire-line system test with in-band interference deliberately added to the BFSK signal, (a) phase detection: error bits can be easily observed (Ch2=*Q*, Ch3=*I*, Ch1=original data, Ch4=recovered data), (b) amplitude comparison: no error bits (Ch2= -*j*CmplxFltr o/p, Ch3=+*j*CmplxFltr o/p, Ch1=original data, Ch4=recovered data)

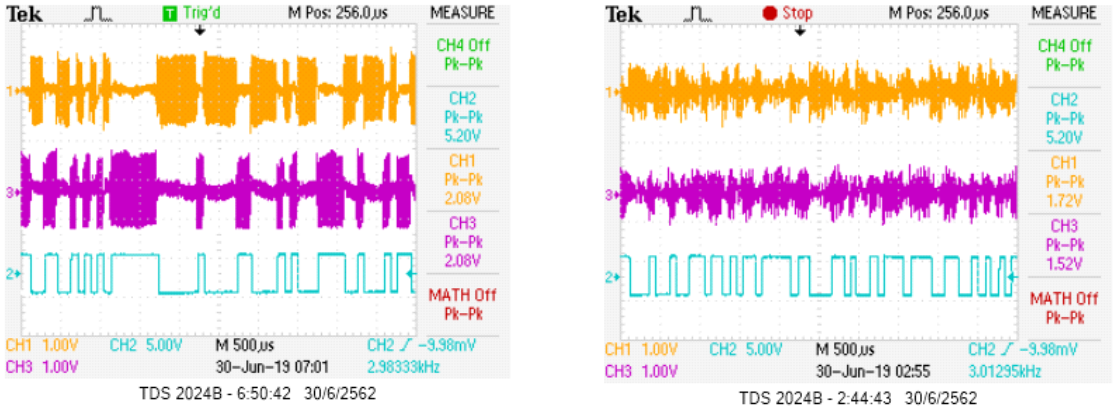


(a) (b)

Figure 14. Wireless system testing, (a) distance at 10 meters and (b) spectrum at PA's input

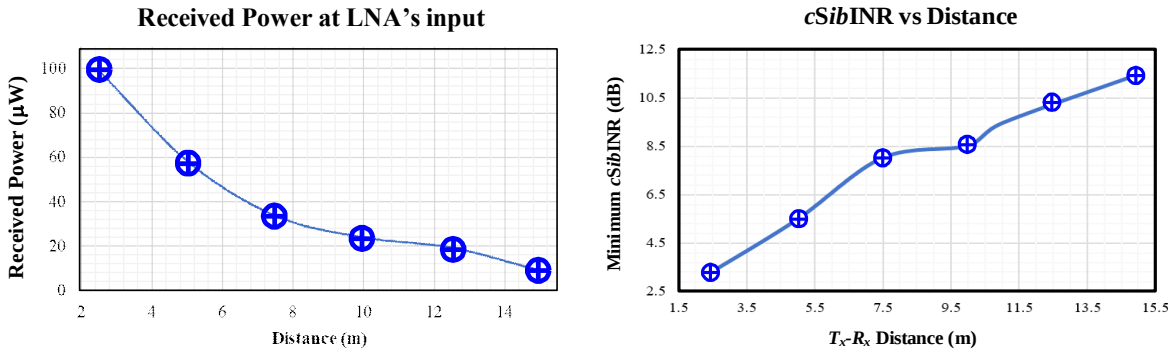


(a)



(b)

Figure 15. Wireless system test at 10-m distance for two data recovering techniques with the same level of interference, (a) phase detection by D-FF without (left) and with (right) interference: *I* (Ch1), *Q* (Ch3), recovered bits (Ch4), (b) amplitude comparison without (left) and with (right) interference: -*j*CmplxFltr o/p (Ch1), +*j*CmplxFltr o/p (Ch3), recovered bits (Ch2)



(a) (b)

Figure 16. The system performance *vs* distance, (a) the LNA's input power and (b) the minimum *c*S*ib*INR using the amplitude comparison

Similar to [26], the tolerance to in-band interference has also been tested with the system being subjected to single-tone and two-tone in-band interferences around the modulating frequency of 400 kHz as shown in Figure 2(a). The sensitivity results are plotted in Figure 18 where the signal-to-interference ratio

(SIR) has been measured at BER=10^{-3} at 10 kbps. The *frequency offset* is a frequency deviation from the modulating frequency (=400 kHz) of a single-tone interference as shown in Figure 18(a) or of a common frequency of the two-tone interferences as shown in Figure 18(b), the two-tone frequency difference was fixed at 100 kHz. The SIR sensitivity level in Figure 18(c) is plotted against a *frequency span* from the two-tone common frequency (fixed at 400 kHz). From the measured results in Figure 18, a smaller SIR level at BER=10^{-3} strongly suggests that the amplitude detection technique outperforms its phase comparison counterpart. Table 1 summarizes the performance of the transmission system.

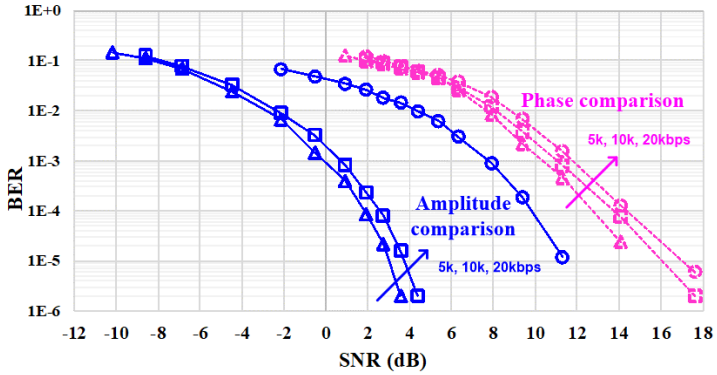


Figure 17. Measured BER *vs* SNR comparison between the two receiver techniques at 5, 10, 20 kbps

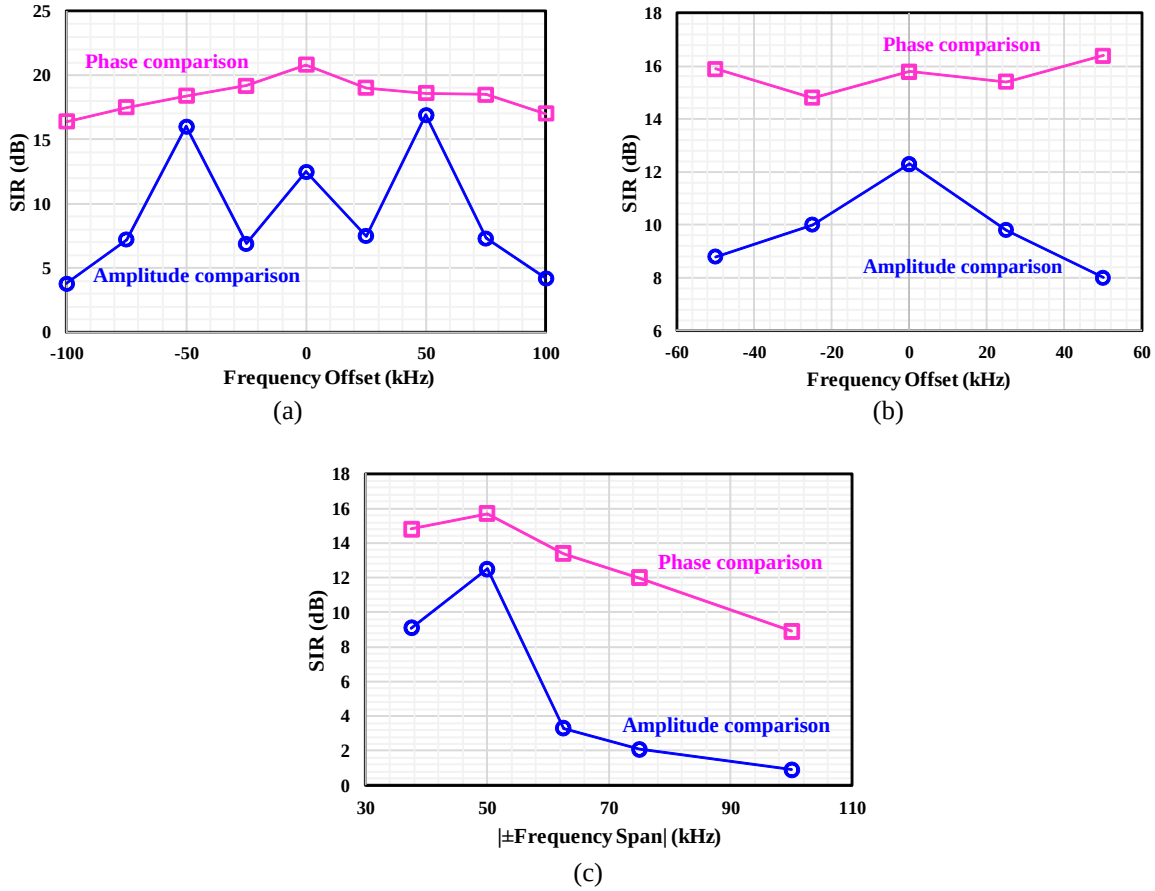


Figure 18. Compared sensitivity at BER=10^{-3} at 10 kbps: (a) single-tone interference, the offset is measured from 400-kHz, (b) the two-tone common frequency as offset from 400-kHz, and (c) with a fixed two-tone common frequency and a symmetrical frequency span

Table 1. Summary of the wireless system performance

V_{CC} (single supply)	5 V
Modulation technique	BFSK
FSK carrier frequency, $f_c \pm \Delta f$	400 kHz±50 kHz
RF frequency	27.4 MHz
Peak power delivered to antenna	240 mW
PA's max. efficiency	30%
Maximum data rate	40 kbps at max. distance of 15 m (no interference added)
Minimum *cSib*INR (at the complex filters' outputs) at 20 kbps	3.3 dB (at 2.5 m)
	11.5 dB (at 15.0 m)
SNR at BER=10^{-3}	1 dB (amplitude detection)
for data rate=10 kbps	11 dB (phase detection)
for data rate=20 kbps	7.9 dB (amplitude detection)
	11.8 dB (phase detection)

5. CONCLUSION

A 27-MHz BFSK wireless radio system has been reported. The receiver employs a direct conversion with complex filtering and amplitude comparison for recovering digital data. This helps make the receiver more tolerant to any in-band or out-of-band interference as compared to a well-established phase comparison technique. The system has been successfully verified with measurements using off-the-shelf discrete components. In the future study, number of components and power consumption can be further reduced by employing a single complex filter. This will be integrated in a standard complementary metal oxide semiconductor field effect transistor (CMOS) technology and reported in another literature.

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