

Strategy to reduce transient current of inverter-side on an average value model high voltage direct current using adaptive neuro-fuzzy inference system controller

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ABSTRACT

Growing-up of high voltage direct current (HVDC) penetration into modern power systems (PS) makes difficulty on the PS operation. The HVDC produces high and slow transient current (TC) at start-time, especially for higher up-ramp rate ($U_{rr} > 20$ pu/s). Its condition makes the HVDC cannot be linked and synchronized into the PS rapidly. A strategy to reduce the TC is proposed by an adaptive network based fuzzy inference system (ANFIS) control on inverter HVDC-link to cope up this problem. The ANFIS control is tuned with the help of conventional control in various train-data by using offline mode. Response of ANFIS scheme is improved by suppressing TC at the values of 3.75% for the both phases (A and C), and 3.95% for phase B, for the $U_{rr} = 30$ pu/s. While the conventional control achieved at 9.1% for the both phases (A and B), and 9.2% for the phase C. The ANFIS control gives shorter settling time (0.553 s) than the conventional control (0.584 s) for all phases. The proposed control is more effective than the conventional control at all the scenario.

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1. INTRODUCTION

Transmission networks have played a prominent role to transmit amount of power through high voltage direct current (HVDC) circuits in modern power systems. The HVDC is not applied on flat-land only, but commonly installed on over-terrain areas also, and operated on extremely environment temperature. These conditions make the HVDC lead to high-rate faults on its line, such as: 3-phase or/and phase-to-ground short-circuit faults. Some protection schemes have conducted to cove these problems, likes: Smoothing-reactor voltage method is used on pilot protection to protect LCC-HVDC [1], wide-area protection for transmission-link using fault-component complex power [2]. Transient response maintenance of LCC-HVDC model is done by controlling both on the voltage and current of rectifier and inverter-sides, respectively [3].

Indonesia has around 290 million people, to develop the HVDC-link is one of economy aspect considered to grow-up income of domestic residents [4] occupy and live on main-islands [5] and other small-islands, that the total number of islands in Indonesia archipelago is 16,771 islands in 2020 [6]. So, to build transmission of electric power systems (EPS) in this country should be considerate to use high voltage alternating current (HVAC) and HVDC lines. Due to geographically constraint, the EPS(s) of Indonesia are developed in main-islands and each EPS(s) are operated to service local load demand. Moreover, the EPS(s) are separated by strait or sea, except for Java-Madura-Bali EPS. The HVDC-link has been considered to develop in order to merge the existing EPS, and to meet the increasing of energy demand. Pre-study and

feasibility analysis of HVDC-transmission to connect the Java-Sumatra EPS are done in [7], [8]. In power systems perspective, the HVDC-link is used to avoid line-outage-cascade by preserving a load-margin of some selected critical AC-lines at an acceptable-level during disturbance period [9]. Small-signal model is built using transfer-function matrix to control hybrid multi-terminal HVDC on different mode operation [10]. Accurate small-signal stability is implemented on an appropriate level HVDC-model to match with EPS model, and a simple HVDC-model is able to reduce complexity of model and simulation time [11]. Protection and control schemes are done as follow: Rapid fault-detector scheme developed by low-freq voltage-part and fast-filter to protect both the pole and line of HVDC transmission [12], a module to prevent commutation-failure to reduce extinction-angle in HVDC by adjusting of resistance proportionally [13], supplementary control is implemented to suppress transient response in HVDC-side [6], supplementary damping control is used to mitigate inter-area oscillation in EPS-side [14], and a novel supplementary damping control based on response-frequency is applied to improve the stability margin of weak HVAC grid [15]. Application of artificial intelligent expands to electrical engineering such as: Artificial neural network is applied for protection current source converter- high voltage direct current (CSC-HVDC) line in [16] to improve transient stability under variation operating of HVDC-link [17] and robust stability power on transmission-line [18].

Optimization method (OM) is develop also, like: Chaotic brain-storm and teaching-learning OMs are used to minimize power loss on 14/30 and 57 IEEE standards [19], [20], particle swarm optimization (PSO) and the PSO combine by adaptive network based fuzzy inference system (ANFIS) are applied on wind farm-HVDC [21] and on photovoltaic (PV) tracking [22]. Genetic algorithm OM based on sliding mode control is used to improve dynamic stability system of source voltage converter HVDC in considering wide range operating conditions [23]. Bacterial foraging and grey wolf OMs are applied in capacitor-run motor [24] and to estimate input-output parameters power plant, respectively [25]. Fuzzy and fuzzy type-2 controls are used to improve maximum performance point tracker (MPPT) of solar panel dynamic performance under variation weather conditions [26] and drive control of permanent magnet synchronous machine [27]. Moreover, ANFIS control has been applied to enhance the performance of wind-farm induction generator [28], to regulate vector control of induction motor [29], to control the MPPT under rule numbers reduce in terms of tracking speed and static error [30]. Also, the ANFIS control is used on inverter HVDC [31], on stability enhanced of three-bus EPS [32], combined by fuzzy type-2 method applied on large-scale EPS [33], and collaborated by proportional-integral-derivative (PID) loop control to improve transient voltage on EPS [34]. Simulation of the HVDC produces high and slow transient current (TC) at starting-time, especially for higher up-ramp rate. So, this issue makes the HVDC too slow to be linked and synchronized to the EPS. Some efforts have done to reduce transient responses such as: on AC-DC power converter using feedforward compensation system [35], on inverter using neural network with embedded machine learning [36], on DC-DC buck converter to improve transient response by using source in triangular wave shape signal [37], on DC-DC converter to improve transient responses by implementing internal [38] and feedforward compensations [39], respectively. But, how to reduce transient current of starting-time in inverter-side of average value model-high voltage direct current (AVM-HVDC) is very important to make the linking and synchronizing the HVDC to the EPS networks faster and secure. To cope up this problem, a strategy to reduce the TC is proposed by an ANFIS-based control on inverter HVDC-link. The rests of this article are organized as follows: Concept of average value model and its application for HVDC are explained on section 2. Moreover, in section 3 is described procedure to design ANFIS control. Next, simulation results of ANFIS control in reducing the current transient analysis and discussion are given in section 4. Finally, effectiveness of the proposed control to reduce the transient response is concluded in section 5.

2. AVERAGE VALUE MODEL OF HVDC

A popular method that can be applied to build supplement model of a physical complex system by using differential and/or algebra equations is an average value model (AVM). The AVM of the HVDC is emerged on [40]–[42], this model is developed to replace detailed model function and to analyses HVDC behavior when it connected to the power system. The AVM-HVDC model that we used is provided by [43]. The model is structured by: An ideal source, filter and rectifier at sending-end, 300 km long-distance DC-line, inverter, filter and an ideal source at receiving-end. By assuming, the HVDC is operated on normal mode that power direction is flowed from sending-end to receiving-end. The AVM on inverter HVDC can be realized according to block diagram depicted on Figure 1(a). Signal guide of current reference on Master control is shown in Figure 1(b). Figure 2(a) shows the equivalent model of AVM-HVDC inverter-side that constructed by DC system, inverter and AC system. For the AVM model, all high-frequency switching in detailed-models such as: The DC, inverter and AC systems are substituted by differential and algebra modules. So, interfacing and implementing scheme of inverter-side are done to convert the detailed-model into the AVM at receiving-end of HVDC. There are two methods can be used such as: A 3-phase original and

a direct-quadrature axis transformation methods [40]. Block diagram of original method is shown in Figure 2(b). While, transformation method block diagram is shown in Figure 2(c).

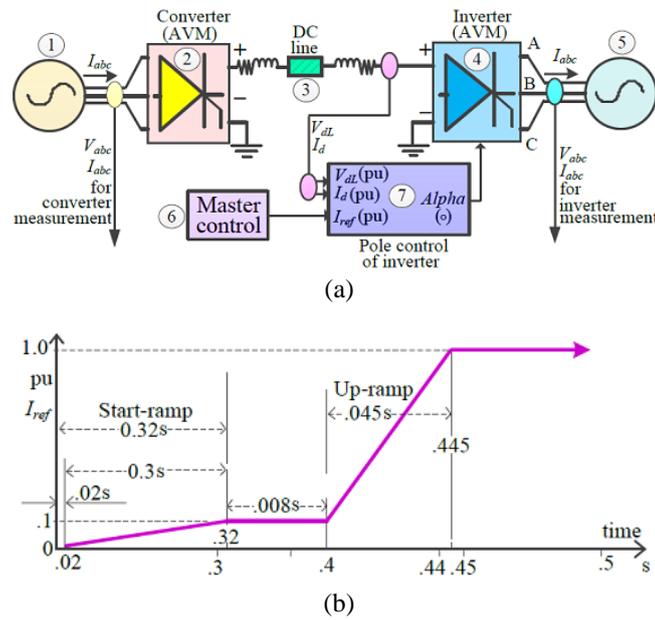


Figure 1. HVDC transmission based on AVM for (a) inverter-side of HVDC, its control and (b) pattern of I_{ref} signal to guide the inverter pole control (Block 7)

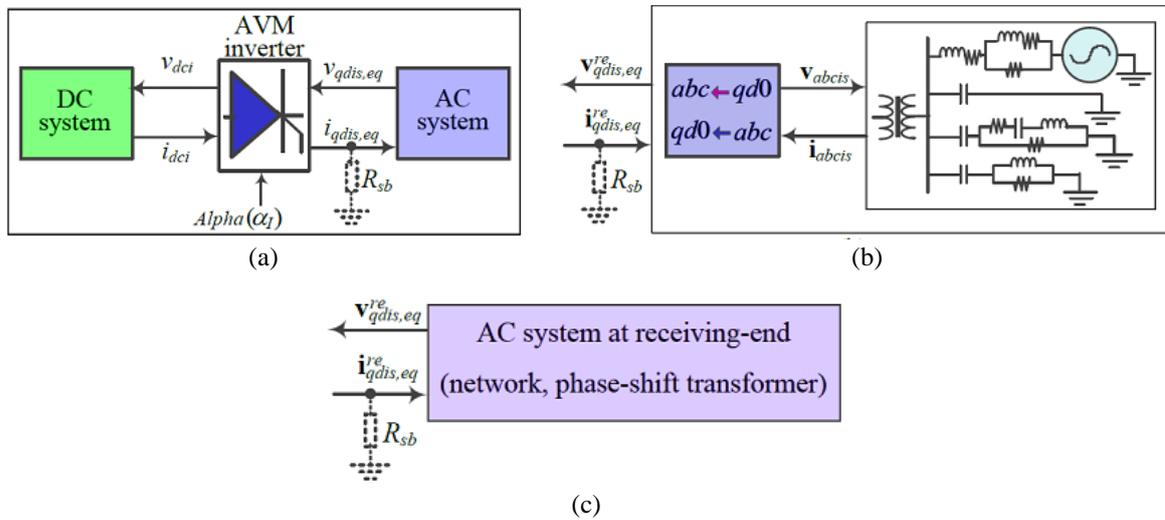


Figure 2. Implementing and interfacing of AVM on inverter-side HVDC-link at (a) AVM of inverter-side HVDC, (b) on abc original circuit and (c) on $qd0$ transformation circuit

3. PROCEDURE TO OBTAIN ANFIS CONTROL

To obtain ANFIS parameter controller some procedure was done: Running the system under start-time equipped by conventional (PI) controller as shown in Figure 3(a). The up-ramp rate was varied from 20 until 30 pu/s, data were collected and stored on mat file format. Fuzzy model Sugeno [44], [45] was used to realize the ANFIS control because this model can be trained by using data that has collected before. Next, the ANFIS control was developed by training processes to adjust ANFIS parameters. At training stage, three matrix-data such as: Training-data, testing-data and checking-data are loaded from workspace. In this initiated, 2 Gaussian membership functions (MFs) and linear MF were set on inputs and output, respectively. Fuzzy inference system was generated and set by grid-partition algorithm. Hybrid optimization method was

set to optimize the ANFIS parameters. Inputs of the ANFIS are the current error (I_{err}) and its derivative (dI_{err}). Figure 3(b) depicts membership functions for the I_{err} input. Linear function type is applied to present output membership function in this learning. Relationship of the both inputs and output of ANFIS control can be represented by input-output control surface that shown in Figure 3(c). Conventional combined by ANFIS control diagram block is shown in Figure 3(d).

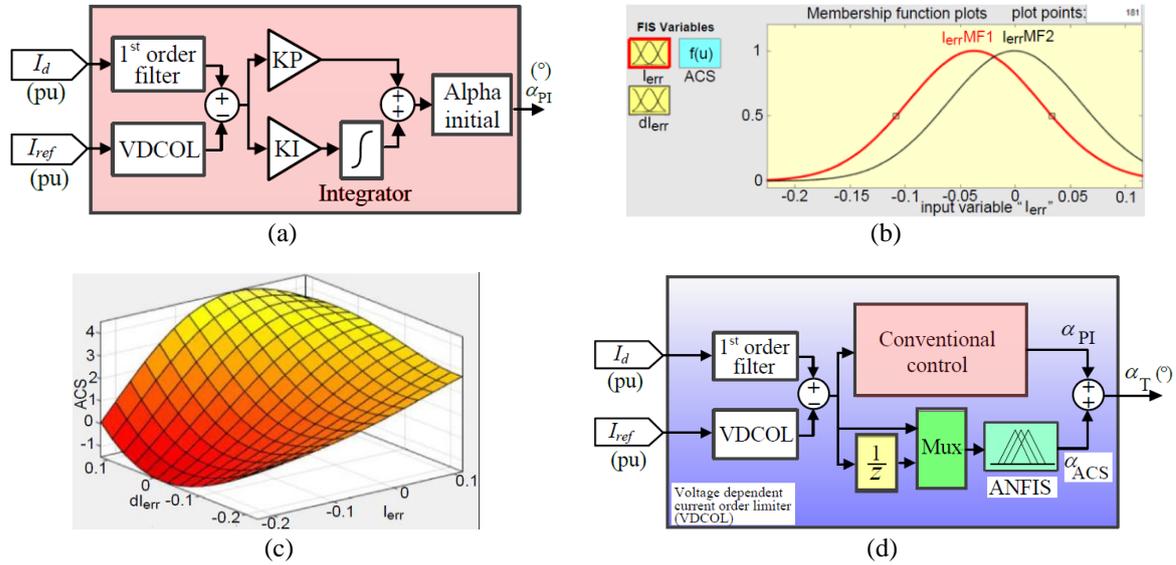


Figure 3. Inverter control, (a) conventional, (b) MF for I_{err} input, (c) I-O surface, and (d) conventional plus ANFIS

4. RESULTS AND DISCUSSION

To assess proposed control performance, the controller is tested by changing parameters at Master control such as: Up-ramp final-value and up-ramp rate. Simulation is performing on Intel Core i5-7400 PC and MATLAB/Simulink software [46]. In this research, the up-ramp final-value was set at: 1.0 (default), .98 (decreased), and 1.02 pu (increased) scenarios. The proposed control was run on respective scenarios and compared to conventional controller (PI) on default setting ($K_p = 45$; $K_I = 4500$) [43].

4.1. Testing ANFIS scheme control for default value (1.0 pu)

At first time, the AVM-HVDC system was tested by default of up-ramp final value (U_{rfv}) at 1.0 pu. Up-ramp time was taken at .4 s. Simulation results are observed on maximum peak overshoot (M_p) and settling time (t_s) for respective effective phase currents (or phase currents for simplification) (I_{a_eff} , I_{b_eff} and I_{c_eff}) at start time. In order to simplify peak overshoot of current reference and phase current comparison, the value of I_{eff} was added by .206 pu for I_{ref} 1.0 pu. These results are illustrated in Figure 4. Quantitive results are listed on Table 1. When the system was run on up-ramp 20 pu/s, the conventional controller gives the results as follows: Peak overshoot (M_p) was achieved at the values of 1.0432 (4.32), 1.0431 (4.31) and 1.0442 (4.42) pu (%) for I_{a_eff} , I_{b_eff} and I_{c_eff} . The response was settled at time .599 s for all phase currents.

When up-ramp rate (U_{rr}) was set on 22 pu/s, peak (maximum) overshoot (M_p) increased also to the values of 1.0568 (5.68), 1.0562 (5.62) and 1.0561 (5.61) pu (%). The settling time (t_{st}) obtained slightly shorter at time of .569 s for all phase currents. For the U_{rr} regularly increased the response for the M_p was also increased again proportionally. The highest of peak overshoot was observed at 1.092 (9.2) pu (%) for the phase C current (I_{c_eff}) for the U_{rr} at the values of 30 pu/s. At this operation, the HVDC gives settle time at 0.569 s. Next, the ($U_{rr} = 20$ pu/s), the ANFIS controller gives results as follows: The M_p response was obtained at 1.0095 (0.95), 1.0085 (0.85) and 1.0084 (0.84) pu (%) for I_{a_eff} , I_{b_eff} and I_{c_eff} , respectively. The response was settled at time 0.569 s for all phase currents. The testing signal increased to 22 pu/s, it is obtained that peak overshoot at 1.0134 (1.34), 1.0152 (1.52) and 1.0145 (1.45) pu (%). The settling time is slightly shorter at time of .567 s for all phase currents. The highest of peak overshoot was obtained at the value of 1.0395 (3.95) pu (%) for the phase B current for the U_{rr} at 30 pu/s. At this condition, response for the t_s was at time .553 s. These detail responses are given in Figure 5 and Table 1 for the both controllers. From this scenario we show that the peak overshoot of the ANFIS controller is less than the peak overshoot of the PI controller. The performance of the ANFIS controller is better than the competing controller for both the peak overshoot and settling time criterions.

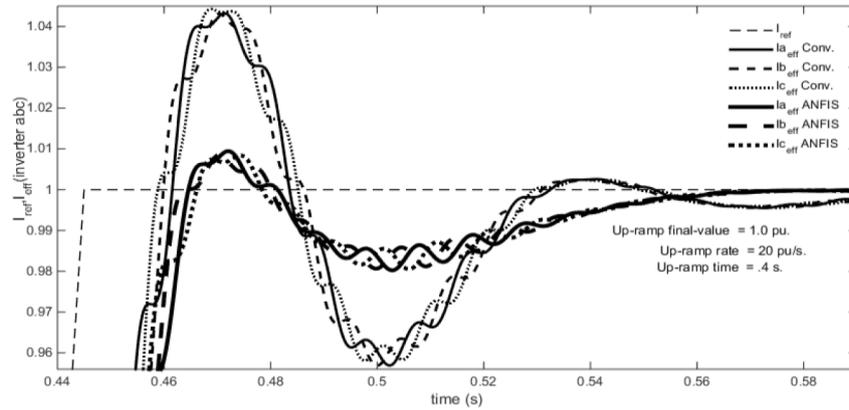


Figure 4. Comparison of I_{abc} peak overshoot of inverter for PI and ANFIS controllers at start-time

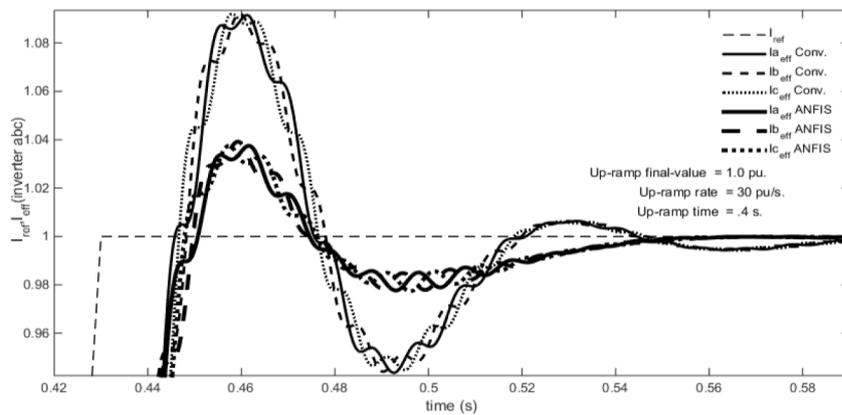


Figure 5. Reducing of I_{abc} peak overshoot of inverter by ANFIS controller

Table 1. The reduce of transient current responses at default up-ramp final-value

Up-ramp rate (pu/s)	Conventional control						ANFIS control								
	M_p (pu)	I_{a_eff} (%)	t_s (s)	M_p (pu)	I_{b_eff} (%)	t_s (s)	M_p (pu)	I_{c_eff} (%)	t_s (s)	M_p (pu)	I_{a_eff} (%)	t_s (s)	M_p (pu)	I_{b_eff} (%)	t_s (s)
20	1.0432		.599	1.0431		.599	1.0442		.599	1.0095		.569	1.0085		.569
	4.32			4.31			4.42			.95			.85		
22	1.0568		.598	1.0562		.598	1.0561		.598	1.0134		.567	1.0152		.567
	5.68			5.62			5.61			1.34			1.52		1.45
24	1.0674		.596	1.067		.596	1.0671		.596	1.0198		.564	1.0191		.564
	6.74			6.7			6.71			1.98			1.91		2.1
26	1.0765		.593	1.0768		.593	1.0763		.593	1.0265		.558	1.0248		.558
	7.65			7.68			7.63			2.65			2.48		2.54
28	1.0845		.589	1.085		.589	1.084		.589	1.032		.556	1.032		.556
	8.45			8.5			8.4			3.2			3.2		2.98
30	1.091		.584	1.091		.584	1.092		.584	1.0375		.553	1.0395		.553
	9.1			9.1			9.2			3.75			3.95		3.75

4.2. Testing on the current reference decrease to 0.98 pu (2%)

In this scenario, the up-ramp final value ($Urfv$) was given on .98 pu. Performance of conventional control is depicted in Figure 6 and listed in Table 2. At the Urr was taken at 20 pu/s, the M_p obtained at the values of 1.0258 (4.0392), 1.0251 (4.602) and 1.0264 (4.7347) pu (%) for I_{a_eff} , I_{b_eff} and I_{c_eff} , respectively. HVDC response for the t_s was settled at time .617 s for all phase currents. The HVDC system was test under the Urr set on 22 pu/s, in this scenario the M_p was obtained at 1.0386 (5.9796), 1.0382 (5.9388) and 1.0378 (5.898) pu (%) for I_{a_eff} , I_{b_eff} and I_{c_eff} , respectively. The settling time was achieved at time .611 s for all phase current effective. Furthermore, the up-ramp rate is increased step-by-step until at maximum value: 30 pu/s. At maximum value, the peak overshoot was increased to 1.0713 (9.3163), 1.0721 (9.398) and 1.0722

(9.4082) pu (%) for I_{a_eff} , I_{b_eff} and I_{c_eff} , respectively. The settling time was achieved at time .604 s for all phase currents. On the other hand, ANFIS controller gives results as follows: Peak overshoot (M_p) at the values of .9908 (1.102), 0.9903 (1.051) and .9891 (.9286) pu (%) for I_{a_eff} , I_{b_eff} and I_{c_eff} , respectively. So, the HVDC response was rapidly to settle on time 0.572 s for all phase currents for ($Urr=20$ pu/s). Simulation for (the $Urr=22$ pu/s), the system gives results as follows: The M_p was gradually uphill to 0.9945 (1.4796), .9964 (1.6735) and .9962 (1.6531) pu (%) for I_{a_eff} , I_{b_eff} and I_{c_eff} , respectively. The settling time was slightly decreased to time 0.567 s for all phase currents. Moreover, the Urr was increased again until to 30 pu/s. In this maximum value, simulation results as follows: The M_p obtained at 1.0713 (9.3163), 1.0721 (9.398) and 1.0722 (9.4082) pu (%) for I_{a_eff} , I_{b_eff} and I_{c_eff} , respectively. Also, the settling time was slightly decreased to time .604 s for all phase currents at this setting. The complete results of ANFIS controller in this scenario are illustrated in Figure 7 and Table 2.

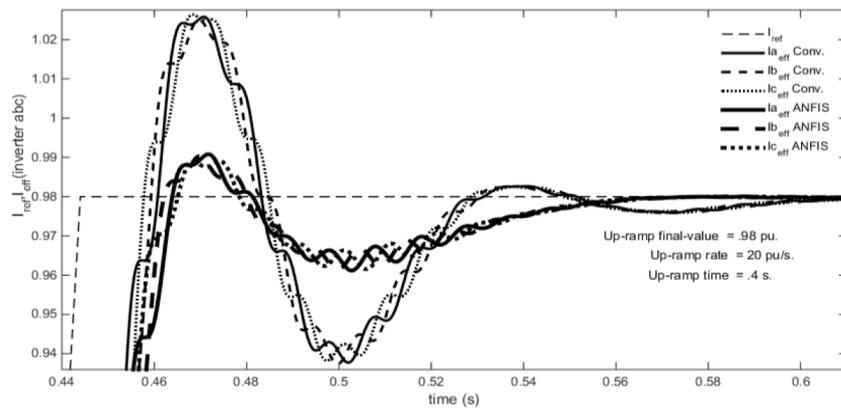


Figure 6. Comparison of phase current inverter for up-ramp rate final-value at .98 pu

Table 2. The improvement of transient current responses at up-ramp final-value .98 pu

Up-ramp rate (pu/s)	Conventional control						ANFIS control					
	I_{a_eff} M_p (pu) (%)	t_s (s)	I_{b_eff} M_p (pu) (%)	t_s (s)	I_{c_eff} M_p (pu) (%)	t_s (s)	I_{a_eff} M_p (pu) (%)	t_s (s)	I_{b_eff} M_p (pu) (%)	t_s (s)	I_{c_eff} M_p (pu) (%)	t_s (s)
20	1.0612 4.0392	.615	1.0619 4.1078	.615	1.0623 4.1471	.615	1.0284 .8235	.575	1.0271 .6961	.575	1.028 .7843	.575
22	1.0752 5.4118	.598	1.0745 5.3431	.598	1.0751 5.402	.598	1.0333 1.3039	.567	1.0344 1.4118	.567	1.0331 1.2843	.567
24	1.0868 6.549	.596	1.0864 6.5098	.596	1.0862 6.4902	.596	1.0385 1.8137	.564	1.039 1.8627	.564	1.0402 1.9804	.564
26	1.0962 6.549	.593	1.0964 7.4902	.593	1.0961 7.4608	.593	1.046 2.549	.562	1.0436 2.3137	.562	1.0454 2.4902	.562
28	1.1047 8.3039	.589	1.1051 8.3431	.589	1.1039 8.2255	.589	1.0523 3.1667	.558	1.0516 3.098	.558	1.0498 2.9216	.558
30	1.1121 9.0294	.585	1.1127 9.0882	.585	1.1121 9.0294	.585	1.0579 3.7157	.555	1.0591 3.8333	.555	1.0567 3.598	.555

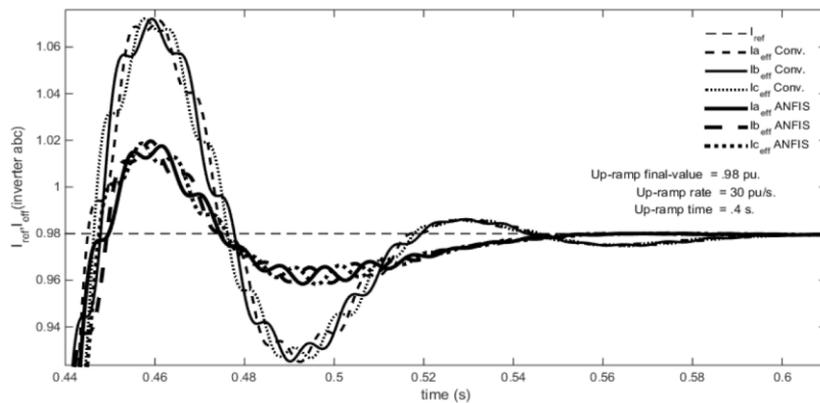


Figure 7. Comparison of phase current inverter for PI and ANFIS controllers at up-ramp rate 30 pu/s

4.3. Transient response reducing for final-value increased to 1.02 pu (2%)

To completeness performance of both the controllers (conventional and ANFIS), these controllers are also tested on 1.02 pu (2% increased). The simulation results as follows: At up-ramp rate was given at 20 pu/s, the peak overshoot (M_p) was obtained at the values of 1.0612 (4.0392), 1.0619 (4.1078) and 1.0623 (4.1471) pu (%) for I_{a_eff} , I_{b_eff} and I_{c_eff} , respectively. The results for up-ramp rate at 20 pu/s are shown in Figure 8 and listed in Table 3. The settling time was achieved at time .615 s for all phase currents. Next, the up-ramp rate was increased to 22 pu/s, the peak overshoot was achieved at the values of 1.0752 (5.4118), 1.0745 (5.3431) and 1.0751 (5.402) pu (%) for I_{a_eff} , I_{b_eff} and I_{c_eff} , respectively. The settling time was slightly decreased to .598 s for all phase currents. Furthermore, the up-ramp rate was increased again until reach maximum value at 30 pu/s. For the maximum Urr , the HVDC response of Pi control achieved on 1.1121 (9.2094), 1.1127 (9.0882) and 1.1121 (9.0294) pu (%) for I_{a_eff} , I_{b_eff} and I_{c_eff} , respectively. The settling time was achieved at time .585 s for all phase currents.

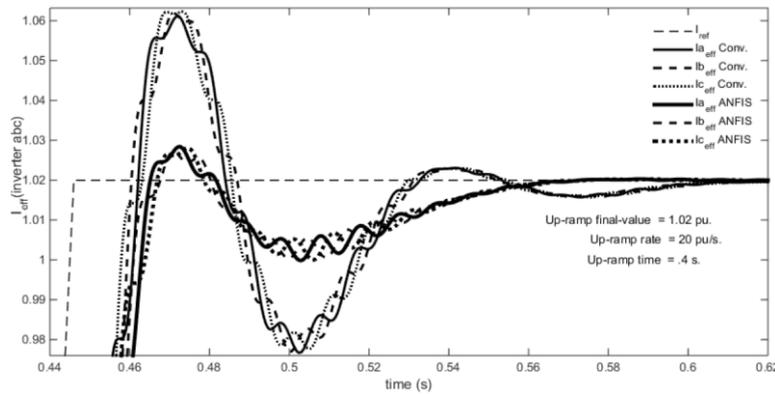


Figure 8. Reducing of I_{abc} peak overshoot by ANFIS controller at up-ramp rate final-value 1.02 pu

Table 3. Simulation results when up-ramp final-value increased to 1.02 pu

Up-ramp rate (pu/s)	Conventional control						ANFIS control					
	I_{a_eff} (M_p (pu) (%)	I_{a_eff} (t_s (s)	I_{b_eff} (M_p (pu) (%)	I_{b_eff} (t_s (s)	I_{c_eff} (M_p (pu) (%)	I_{c_eff} (t_s (s)	I_{a_eff} (M_p (pu) (%)	I_{a_eff} (t_s (s)	I_{b_eff} (M_p (pu) (%)	I_{b_eff} (t_s (s)	I_{c_eff} (M_p (pu) (%)	I_{c_eff} (t_s (s)
20	1.0258	.617	1.0251	.617	1.0264	.617	.9908	.572	.9903	.572	.9891	.572
	4.6735		4.602		4.7347		1.102		1.051		.9286	
22	1.0386	.611	1.0382	.611	1.0378	.611	.9945	.568	.9964	.568	.9962	.568
	5.9796		5.9388		5.898		1.4796		1.6735		1.6531	
24	1.0486	.609	1.0488	.609	1.0486	.609	1.0016	.564	.9996	.564	1.0019	.564
	7.0		7.0204		7.0		2.2041		2.0		1.9804	
26	1.0573	.607	1.0577	.607	1.0569	.607	1.0077	.563	1.0064	.563	1.0059	.563
	7.8878		7.9286		7.8496		2.8265		2.6934		2.6469	
28	1.0649	.606	1.0655	.606	1.0648	.606	1.0128	.562	1.1034	.562	1.011	.562
	8.6633		7.9286		8.6531		3.3469		3.4082		3.1633	
30	1.0713	.604	1.0721	.604	1.0722	.604	1.0175	.561	1.0197	.561	1.0187	.561
	9.3163		9.398		9.4082		3.8265		4.051		3.949	

Meanwhile, results of ANFIS controller are as follows: Peak overshoot was achieved at the values of 1.0284 (0.8235), 1.0271 (0.6961) and 1.028 (0.7843) pu (%) for I_{a_eff} , I_{b_eff} and I_{c_eff} , respectively. The settling time was achieved at time .615 s for all phase currents, for the ($Urr=20$ pu/s). Moreover, the up-ramp rate was increased to 22 pu/s, the results as follows: Peak overshoot was increased to 1.0333 (1.3039), 1.0344 (1.4118) and 1.0331 (1.2843) pu (%) for I_{a_eff} , I_{b_eff} and I_{c_eff} , respectively. The settling time was slightly decreased to time .567 s for all phase currents. Finally, the up-ramp rate was taken at 30 pu/s, the peak overshoot was obtained at 1.0579 (3.7157), 1.0591 (3.8333) and 1.0567 (3.598) pu (%) for I_{a_eff} , I_{b_eff} and I_{c_eff} , respectively. Also, the settling time was slightly decreased to time 0.555 s for all phase currents at this setting. The complete simulation results of ANFIS controller in this scenario are illustrated in Figure 9 and Table 3. We can proof our proposed control is effective to reduce the HVDC response on significant value at around 3%, while result of competing control is around 9%. In addition, the ANFIS control gives the HVDC response is shorten to settle for all scenarios. The proposed control gives good results in the scenarios. But the proposed control gives not a significant improvement on low up-ramp rate. The other scenario, except that explained in this research is not conducted yet.

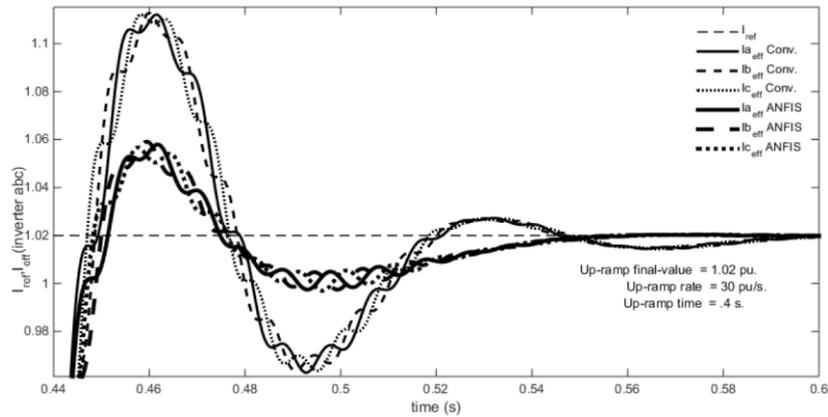


Figure 9. Reducing of I (abc) of inverter by ANFIS controller at up-ramp rate 30 pu/s

5. CONCLUSION

A strategy to reduce the peak overshoot of HVDC by using ANFIS controller is proposed, designed and simulated in this research. The ANFIS algorithm is built by training data procedure that find out from running up the HVDC-link and regulated by PI control on its firing angle. During the development period, the HVDC model is run under variable and parameter values are changed in various ways. First, at up-ramp final-value 1.0 pu, ($U_{rr}=30$ pu/s) the PI control gives results: The maximum peak overshoot (Mp) of phase current was at the values of 9.1% for the both phases (A and B), and 9.2% for the phase C. Meanwhile, the proposed control gives results as follows: The Mp of phase current is observed at the values of 3.75% for the both phases (A and C), and 3.95% for the phase B. At this operation, the settling time is achieved at the time of 0.584, and 0.533 s, for the conventional and proposed controls, respectively. Second, result of the conventional control with the up-ramp final-value set at .98 pu, the peak overshoot of phase was at the values of 9.0294% for the both phases (A and C), and 9.0882% for the phase B. For the proposed control, the peak overshoot of phase current was at the values of 3.7157, 3.8333 and 3.598% for the phases A, B and C. The settling time is achieved at the time of .585, and .555 s, for the conventional and proposed controls. Third, the result of conventional control with the up-ramp final-value increased to 1.02 pu, the peak overshoot of phase current was at the values of 9.3163, 9.398 and 9.4082% for the phases A, B and C, respectively. The proposed control was as follows: 3.8265, 4.051 and 3.949% for the phases A, B and C. The settling time was at the time of .604, and .561 s, for the conventional and proposed controls. So, the ANFIS control makes the Mp decrease and the settling time shorter. Where, the results of the proposed control are compared to results of PI control for validity procedure is properly done. In the next research, it is potential to investigate other schemes of control of HVDC in simulation as well as laboratory scale using real-time digital system (RTDS) or side-field.

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