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Design and performance analysis of human body communication digital transceiver for wireless body area network applications

Sujaya Bangalore Lokanatha[1], Sompura Basavaraju Bhanu Prashanth[2]
[1]Department of Electronics and Communication Engineering, B.N.M. Institute of Technology, Bengaluru, India
[2]Department of Medical Electronics Engineering, B.M.S. College of Engineering, Bengaluru, India

Article Info

ABSTRACT

Wireless body area network (WBAN) is a prominent technology for resolving health-care concerns and providing high-speed continuous monitoring and real-time help. Human body communication (HBC) is an IEEE 802.15.6 physical layer standard for short-range communications that is not reliant on radio frequency (RF). Most WBAN applications can benefit from the HBC's low-latency and low-power architectural features. In this manuscript, an efficient digital HBC transceiver (TR) hardware architecture is designed as per IEEE 802.15.6 standard to overcome the drawbacks of the RF-wireless communication standards like signal leakage, on body antenna and power consumption. The design is created using a frequency selective digital transmission scheme for transmitter and receiver modules. The design resources are analyzed using different field programmable gate array (FPGA) families. The HBC TR utilizes <1% slices, consumes 101 mW power, and provides a throughput of 24.31 Mbps on Artix-7 FPGA with a latency of 10.5 clock cycles. In addition, the less than 10-4bit error rate of HBC is achieved with a 9.52 Mbps data rate. The proposed work is compared with existing architectures with significant improvement in performance parameters like chip area, power, and data rate.

Corresponding Author:

Sujaya Bangalore Lokanatha
Department of Electronics and Communication Engineering, B.N.M. Institute of Technology
12th Main Road, 27th Cross, Banashankari Stage II, Banashankari, Bengaluru, Karnataka 560070, India
Email: sujayabl@bnmit.in

1.   INTRODUCTION

The wireless body area network (WBAN) is a new technology that may be used to track and monitor the human body. In most application disciplines, such as intelligence, entertainment, and medicine, this technology creates a new paradigm. The WBAN is a network of sensors that operate on the human body and measure a variety of essential data. The WBAN's mobility, dependability, and adaptability are its distinguishing qualities. Intra-body communication (IBC) is a wireless technology alternative that solves the majority of the flaws of radio frequency (RF) based wireless technologies. The physical layer (PHY) standard for WBAN is IEEE 802.15.6, which is divided into three categories: narrow-band (NB), ultra-wide-band (UWB), and human body communication (HBC). The RF wireless technologies include NB and UWB, whereas HBC uses non-RF technology. The RF wireless technology runs in the frequency range of 402 MHz to 10 GHz, with data speeds of up to 13 Mbps, a distance coverage of up to 10 meters, and an on-body antenna that saves energy. Similarly, HBC uses a central frequency of 21 MHz, transmits data up to 2 Mbps, has a range of 2 meters, does not require an on-body antenna, and has a greater energy efficiency in the human body [1]–[3].

The HBC with galvanic and capacitive coupling has to meet a few main characteristics: lower carrier frequency, low signal attenuation, lower transmission power, higher security, and small-signal leakage. There are many HBC signal propagation models like the finite difference time domain (FDTD) method, analytical electromagnetic model, finite element method (FEM), and general circuit model that are selected for data transmission in the human body [4]. The HBC is designed for wearable computing, sensing, medical, and other portable wireless networking applications [5]. The WBAN is used in most medical applications like disease monitoring [6], handling medical emergencies using a Software-defined network [7], hearing aids [8], and real-time patient monitoring at high throughput [9].

HBC is a popular communication method to exchange the data/power transmission between two or more electronic devices in a body area network (BAN). Most of the HBC use coupling (capacitive) as a transmission channel. The electrical signals are passed via the Human body in both HBC transmitter (HBC TX) and HBC receiver (HBC RX) using capacitive coupling. Both the HBC TX and HBC RX uses electrode by replacing the antenna. The Human body with an electrode provides the modulating electric signals at the HBC TX side, and it demodulates electric signals at the HBC RX side. IEEE 802.15.6 has acknowledged the PHY-based HBC as a short-range communication standard, particularly for WBAN applications [10]. HBC has a lower level of complexity and uses less energy. The data is received by the human body and distributed throughout the frequency selective (FS) domain utilizing digital codes.

The overview of the complete HBC modem is represented in Figure 1. The data information is provided by the medium access control (MAC) controller to the first in first out (FIFO) module of the HBC TX interface. The HBC TX Module gets data from the FIFO and sends it to the analog frontend (AFE). The electrode transmits the AFE data to the human body as electric impulses. The electrode transfers the detected data to the HBC AFE from the human body. The HBC RX module delivers the human body data to the HBC RX interface, which then transfers it to the MAC controller. The MAC controller offers the human body and other linked devices with a full data control mechanism.
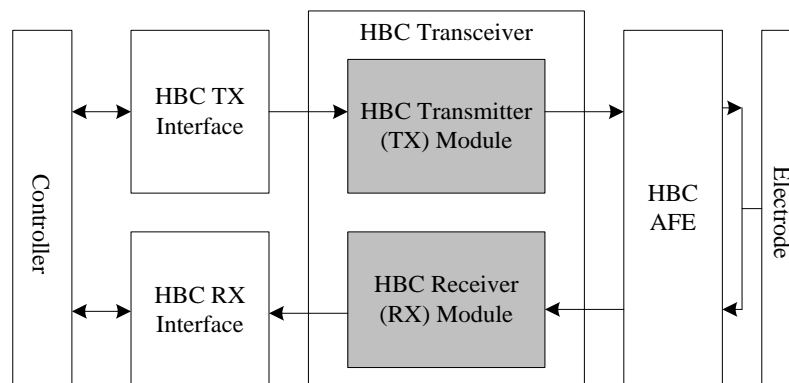

Figure 1. Overview of complete HBC modem

Most BAN applications employ RF-based wireless technology, which uses greater chip space, uses more battery power, has numerous security concerns, and is impacted by electromagnetic interference. As a result, non-RF wireless technology is required to track BAN applications. Most of the existing HBC systems are designed using a software environment, and very few are adopted in the hardware platform. Most of the HBC system's existing HBC system is concentrated more on the HBC analog front end (AFE) rather than the HBC transceiver using the field programmable gate array (FPGA) platform. Several HBC TR designs have been built on the FPGA platform, however performance parameters such as chip area, power, data rate, and bit error rate (BER) have been found to be lacking. As a result, efficient HBC TR for WBAN applications is required to address the aforementioned issues while also improving performance metrics.

In this manuscript, an efficient HBC transceiver architecture is proposed for wireless BAN applications using the IEEE 802.15.6 PHY standard. The proposed architecture provides low-latency, high throughput and utilizes lesser chip resources on hardware. As a result, the hardware module obtains a better BER and is suitable for BAN applications. Section 1 describes the existing body-communication system review and its performance analysis. Section 2 explains the detailed hardware architecture of the HBC transceiver. The results and discussion with simulation, synthesized, and comparative results for HBC-TR in section 3. Finally, in section 4 it finishes the whole work with a futuristic viewpoint.

This section gives an overview of the review of the existing HBC system methods and their analysis. Shimizu *et al.* [11] present the FPGA-based ultra-wideband (UWB) based impulse radio (IR) receiver module for in-out body communication. The UWB-IR RX module contains a synchronization unit, frequency down-converter with a filtering and detection module. The module supports good communication performance in real-time scenarios and achieves the BER up to 10^{-3} with a data rate of 2 Mbps. In the paper, Lee *et al.* [12] describe the HBC TR for an energy-efficient BAN system. The work is analyzed with concepts, practical applications, channel enhancement, network protocol features, and standards compatibility. In the paper, Manchi *et al.* [13] present the digital base-band TR modules for IEEE 802.15.6 standards with low power consumption. The narrowband –TR and HBC TR architectures are designed and work with a data rate of 455 Kbps and 1.3125 Mbps, respectively, with better energy efficiency. Finally, Eddabbah *et al.* [14] present the performance analysis of the IEEE 802.15.6 PHY-based HBC system. The module discusses the BER for hamming, cosine, and Jaccard distance. The hamming distance provides better BER than the other two approaches and proves better message integrity.

Ali *et al.* [15] present the PHY based HBC TR for WBAN on MATLAB and ASIC platforms, including HBC TX, HBC RX with synchronization module. The HBC supports up to 1.325 Mbps and consumes 0.63 mW power. Park *et al.* [16] elaborate on the frequency selective digital transmission (FSDT) based HBC module with BER measurements on software environments. The work analyzes the BER performance of HBC in-and out-of-band interference, BER v/s interference frequency, BER concerning signal to interference ratio (SIR) with existing HBC system with improvements. In the paper, Chung *et al.* [17] present the body channel communication TR using Walsh code on the FPGA platform. The design improved the code rate and enhanced jitter tolerance. The chip rate was achieved up to 12.5 Mcps with a BER of $< 10^{-5}$.

In a software context, Yuan *et al.* [18] described the IEEE 802.15.6 module with the MAC protocol for WBAN applications. Priority allocation, super-frame network, protocol functioning operation, and channel access are all included in the adaptive MAC (A-MAC) protocol. The results are analyzed for average delay comparison concerning nodes, throughput by nodes, and average energy consumption concerning node number. The A-MAC-based IEEE 802.15.6 provides better performance results than normal–MAC and CA-based MAC protocols. The low-power TR for body-channel communication (BCC) utilizing the application specific integrated circuits (ASIC) platform with 65 nm complementary metal-oxide-semiconductor (CMOS) technology is presented by Vijayalakshmi and Nagarajan [19]. BCC incorporates the hamming coding method to enhance data rate. With only 1 mW of power, the BCC reaches a data throughput of 60 Mbps. Intra-body communication (IBC) based on TR utilizing differential-phase shift keying (DPSK) with galvanic coupling is described by Wei *et al.* [20]. The IBC TR achieves the 1 Mbps data rate with a lower coupling amplitude. The complete IBC-TR is developed on the NI-LabView environment. Ventura *et al.* [10] present the priority-based data transmission for WBAN application to improve service quality (QoS), end-end delay, and reliability features.

2.   PROPOSED HBC DIGITAL TRANSCEIVER MODULE

According to the IEEE 802.15.6 PHY standard, this work created the digital baseband HBC transceiver (TR) architecture. Figure 2 depicts the hardware architecture of the HBC TR. HBC TX, the human body as a channel, and HBC RX modules are the primary components of the design. The complete architecture is designed based on the FSDT modulation scheme. The detailed HBC transceiver is explained in the following subsections.

2.1. HBC transmitter

The HBC TX mainly contains preamble/start of frame delimiter (SFD) and physical layer convergence protocol (PLCP) header generator, data generator, serial to parallel (S2P) converter, frequency selective (FS) spreader module, and multiplexer (MUX) module. The preamble generator is used to synchronize the PHY with packet timing. The 64-bit gold code sequences generate the Preamble sequence via frequency shift code (FSC). To achieve packet synchronization on the HBC RX side, the preamble sequences are repeated four times. To frame the 64-bit gold code sequence, the two independent 32-bit gold codes are concatenated. For gold code values '0' and '1', the FSC is specified as "AA" and "55". To create the preamble generator output, multiply the FSC "AA" value with a 64-bit gold code sequence if the LSB bit is zero in the gold code sequence. To create the preamble generator output, multiply the FSC (55) value with a 64-bit gold code sequence if the LSB bit of the gold code sequence is one. The spread factor is set to 8 for FSC and used in HBC-TR. The SFD generator is used to detect the preamble sequence and consider it a start of the packet and a starting point of the SFD frame. In this design, burst mode is set to zero and considers only SFD and not rate indicator. The SFD is the same as the Preamble sequence, but the frame sequence is sent only once for transmission.

Figure 3 shows the PLCP header with payload data formation. The PLCP header [0:15] is defined as per the frame format. The 3-bit data rate is set to "011" and works at 1.3125 Mbps. The pilot insert period is set to "000"; Burst mode is not activated and used only the SFD frame. The scrambler seed is not used in HBC-TR. The 8-bit MAC frame acts as payload data to the HBC TX, and the 8-bit cyclic redundancy check (CRC8) is implemented over PHY based PLCP header. The CRC8 is generated using $1+ x^2+x^3+x^7+x^8$ polynomial. Where 'x' is the polynomial register is used to shift the data, bits based on the polynomial.
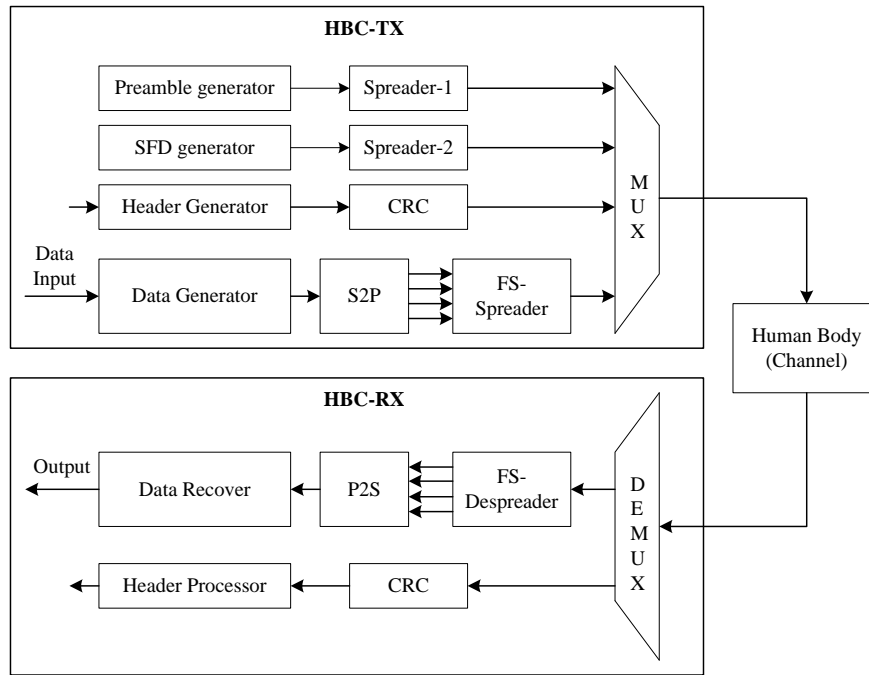

Figure 2. Hardware architecture of HBC transceiver

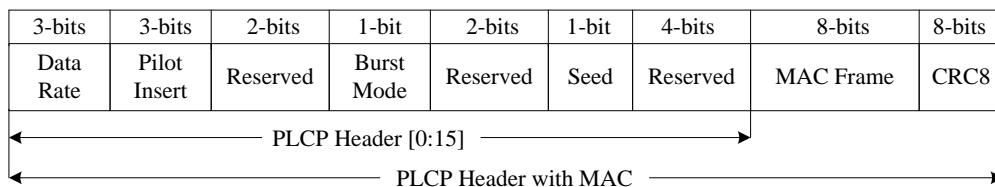| 3-bits	3-bits	2-bits	1-bit	2-bits	1-bit	4-bits	8-bits	8-bits
Data Rate	Pilot Insert	Reserved	Burst Mode	Reserved	Seed	Reserved	MAC Frame	CRC8

PLCP Header [0:15]

PLCP Header with MAC

Figure 3. PLCP header with payload data formation

The PHY service data unit (PSDU) provides the MAC unit's data information via FIFO interface and is designed using the FSDT scheme. It mainly consists of a data generator, an S2P converter, and FS-spreader. The data generator receives 1-bit from FIFO in a sequence at 1.3125 Mbps and frame it to the 4-bit (symbol) using an S2P converter at 328 Ksps. The FS-Spreader is designed using 16-bit Walsh code and FSC. The 16-bit Walsh code (chips) is generated based on the S2P converter output at 5.25 Mcps, tabulated in Table 1. By multiplying the 16-bit Walsh code with an 8-bit FSC, the FS-Spreader module creates the result at 42 Mcps. The multiplexer takes in preamble, SFD, header, and PSDU outputs and creates a single output based on the user's selection line. The additive white Gaussian noise (AWGN) noise in channel is added to the HBC TX multiplexor output before being sent to the HBC receiver.

Table 1. Walsh code generation for mapping

S2P Data	0000	0001	0010	0011	0100	0101	0110	0111
Walsh Code	FFFF	AAAA	CCCC	9999	F0F0	A5A5	C3C3	9696
S2P Data	1000	1001	1010	1011	1100	1101	1110	1111
Walsh Code	FF00	AA55	CC33	9966	F00F	A55A	C33C	9669

2.2. HBC receiver

The HBC RX mainly contains the demultiplexer (DEMUX) module, followed by a PSDU (FS-despreader module, parallel to serial (P2S) converter, and data recovered module) and header processor module. The data recovery procedure is performed by the HBC RX, which receives damaged data from the additive white Gaussian noise (AWGN) channel. Using the same select line, the demultiplexer receives the damaged data and creates the header and PSDU output. The frame synchronizer is used to synchronize the received header and PSDU data with the proper clock mechanism. The FS-Despreader has mainly 16-bit Walsh demodulated code and FSC data. The 16-bit Walsh demodulated code is the same as the 16-bit Walsh code. But the output of the Walsh code acts as an input, and input acts as an output. The 4-bit output is generated by dividing the 16-bit Walsh demodulated code by FSC in the FS-despreader. A shift register is used to produce 1-bit serial data using the P2S converter. The final data sequence is received by the data recovery module. The header information is retrieved by the Header processor and compared to the sent PLCP header information.

2.3. BER calculation

The signal-to-noise (SNR) ratio is used to calculate the bit error rate (BER). The SNR is the energy per bit divided by the spectral noise density (Eb/No) ratio. The AWGN is generated with zero mean and unity variance ($\delta^2=1$). The new variance is generated by performing the inverse and square of scaling factor (s). So $\delta^2=1/s^2$. The SNR is defined based on the scaling factor: $SNR=s^2/4$. Different SNR values are generated based on the scaling factor (s) for the AWGN channel. The BER calculation module is represented in Figure 4. The AWGN channel c(t) generates the random sequence based on a linear feedback shift register (LFSR). The noise data n(t) is generated by dividing the c(t) by scaling factor (s). The corrupted data (n'(t)) is obtained by performing the OR operation of noise data with transmitted data m(t). The HBC RX module receives the damaged data and creates the restored output data r(t). The error signal e(t) is obtained by comparing the recovered data's output with delayed input data i(t). The bit error rate is measured based on the error count divided by the number of data transmitted.
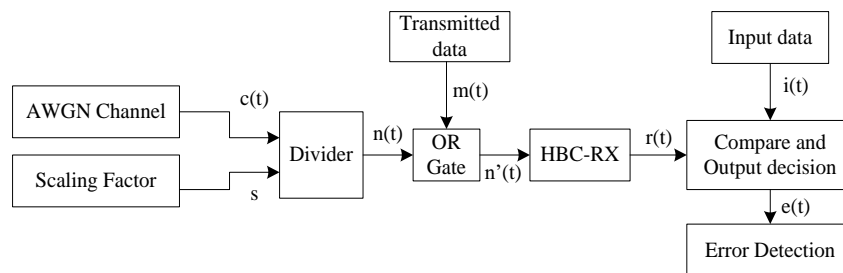

Figure 4. BER calculation module

3. RESULTS AND DISCUSSION

The HBC transceiver (TR) is based on the IEEE 802.15.6 PHY standard and was prototyped using a Xilinx Artix-7 FPGA. The HBC TR is simulated on ModelSim simulator and synthesized using different FPGA families for resource utilization analysis. The comparative and performance analysis are highlighted with existing similar HBC TR modules with better resource improvements. The HBC transceiver simulation results are represented in Figure 5.
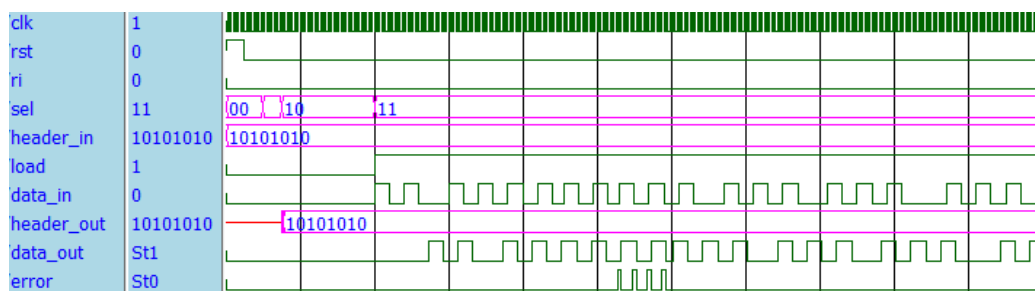

Figure 5. HBC transceiver simulation results

The global clock (clk) is activated with a lower asynchronous reset (rst) and rate indicator (ri). The select line is used in both HBC TX and HBC RX's MUX and DEMUX modules, respectively. If the 2-bit select line is "00", then preamble data is activated; similarly, for "01", SFD data is included with the Preamble generator. For "10", PLCP Header information, and "11", PSDU data is activated. The input data (data_in) sequence is processed when the selective line "11" and the load signal are activated, the input data (data_in) sequence is processed. The HBC TR obtains the receiver data with a latency of 10.5 clock cycles. The error signal indicates the detection of error between the input and received data sequences. The 10188 bits are transmitted with a scaling factor of 4 to the HBC TR and detect the 40 error bits in the ModelSim simulator. The calculated BER is 3.92×10^{-3} at 6 dB SNR. If the transmitted bits are increased, a better BER rate will be achieved.

The HBC transceiver design is implemented using FPGAs from the Spartan-6, Artix-7, and Virtex-7 families. Table 2 lists the design parameters acquired, such as slice, LUTs, maximum operating frequency (MHz), and power. On the Spartan -6 FPGA, the HBC TR uses 197 slices and 1137 LUTs, operates at 170.79 MHz, and costs 84 mW of power. On the Artix-7 FPGA, the HBC TR employs 196 slices and 1137 LUTs, operates at 255.31 MHz, and consumes 101 mW total power. On a Virtex-7 FPGA, the HBC TR utilizes 196 slices and 1133 LUTs, operates at 304.89 MHz, and costs 195 mW of power. Using a ModelSim simulator, the HBC TR gets a delay of 10.5 clock cycles (CC). Spartan -6, Artix-7, and Virtex-7 FPGAs were used to achieve throughputs of 16.26 Mbps, 24.31 Mbps, and 29.03 Mbps for HBC TR module by utilizing maximum frequency and latency. The *Throughput is calculated based on standard frequency 100 MHz, suitable for capacitive coupling-based HBC [4]. The *Throughput of 9.52 Mbps is achieved using different FPGAs and meets the IEEE 802.15.6 PHY Standards. *Throughput per slice (Kbps/Slice) is used to calculate hardware efficiency. Spartan-6, Artix-7, and Virtex-7 FPGAs have hardware efficiency of 48.32 Kbps/Slice, 48.57 Kbps/Slice, and 48.57 Kbps/Slice, respectively.

The comparative analysis of different IEEE 802.15.6 standards on the FPGA platform is tabulated in Table 3. The Table 3 shows that selected PHY based IEEE 802.15.6 standard like NB/HBC, coding scheme, utilized area (Slices, LUT's), and power consumption on various FPGAs. On the other hand, the proposed HBC TR is designed considering Artix-7 using Walsh coding scheme, which utilizes 196 slices, 1137 LUT's, and 101 mW power, which is relatively better than the existing PHY standard approaches [21]–[23]. The performance analysis of proposed HBC with existing HBC transceivers [24]–[27] is compared and tabulated in Table 4. The Table 4 shows the comparative study of different performance parameters like CMOS technology used, carrier frequency selected, modulation scheme, obtained data rate, supply voltage, consumed total power (mW), and obtained BER for existing HBC TR's with proposed HBC TR.

The proposed HBC uses Artix-7 FPGA with a 28 nm CMOS process and selects the carrier frequency of 100 MHz for FSDT modulation. The proposed HBC achieves a 9.52 Mbps data rate with consumes 101 mW power and obtains $< 10^{-4}$ BER for 10188 transmitted bits. The proposed HBC has a higher data rate and power than the current HBC TRs [24], [25], [27]. The current HBC TR's [25]–[27] transmitted more than $>10^{-5}$ bits, and BER is calculated as $< 10^{-6}$ and $< 10^{-8}$, respectively.

Table 2. HBC transceiver design results on different FPGA's

Resources	HBC Transceiver Module on Different FPGA's		
FPGA Family	Spartan-6	Artix-7	Virtex-7
FPGA Device	XC6SLX45T-3CSG324	XC7A100T-3CSG324	XC7V330T-3FFG1157
Technology	45 nm	28 nm	28 nm
Slices	197	196	196
LUT's	1137	1137	1133
Frequency (MHz)	170.799	255.31	304.897
Power (mW)	84	101	195
Latency (CC)	10.5	10.5	10.5
Throughput (Mbps)	16.26	24.31	29.03
*Throughput (Mbps)	9.52	9.52	9.52
*Efficiency (Kbps/Slice)	48.32	48.57	48.57

*100 MHz suitable for capacitive coupling-based HBC [4]

Table 3. Comparative analysis of different IEEE 802.15.6 standards on FPGA platform

Resources	Liang *et al.* [21]	Mathew *et al.* [22]	Mohandes *et al.* [23]	Park *et al.* [24]	Proposed
IEEE 802.15.6 Standard	NB PHY	NB PHY	NB PHY	HBC PHY	HBC PHY
FPGA	Spartan-6	Virtex-6	Virtex-6	Artix-7	Artix-7
Coding Scheme	BCH	BCH	BCH	Walsh	Walsh
Slices	2843	2668	846	NA	196
LUT's	3915	3161	1293	5231	1137
Power (mW)	192	117	NA	114	101

Table 4. The performance analysis of proposed HBC with existing HBC transceivers

Design Parameters	Hyoung et al. [25]	Ali et al. [26]	Park et al. [24]	Chung et al. [27]	Proposed
CMOS process	ASIC (65nm)	ASIC (45 nm)	FPGA (130nm)	FPGA (90nm)	FPGA (28nm)
Carrier frequency (MHz)	32	42	32	100	100
Modulation	FSDT	Auto encoder	FSDT	Wideband Signaling	FSDT
Data rate (Mbps)	2	5.25	6	3.125	9.52
Core voltage (V)	3.3	1.2	3	1	1
Power (mW)	194.7	1.4	114	158	101
BER	$< 10^{-6}$	NA	NA	$< 10^{-8}$	$< 10^{-4}$

4. CONCLUSION AND FUTURE SCOPE

An efficient HBC transceiver architecture is proposed and implemented using FPGA in this manuscript. For real-time WBAN applications, the HBC TR has a reduced chip complexity and a greater data rate. The HBC TR mainly contains HBC TX, HBC RX, and assuming AWGN channel as the human body. Data transmission and reception are achieved with proper synchronization and clocking mechanism in HBC TR. The HBC TR is synthesized on the Xilinx environment for different FPGA families and tabulated resource utilization. The simulation results show that the modeled HBC TR is working efficiently with less error count. The proposed work achieves less than 10^{-4} BER, and it is suitable for digital-based TR in WBAN applications. The FPGA-based comparative results of HBC with existing HBC TR are analyzed to improve Chip area and power. The proposed HBC TR achieves a data rate of 9.52 Mbps, which meets the IEEE 802.15.6 PHY standards for WBAN applications and utilizes the power of 101 mW comparatively less than the existing HBC TR architectures. In the Future, the proposed HBC TR will be integrated with HBC AFE to analyze the human body characteristics.

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BIOGRAPHIES OF AUTHORS

Sujaya Bangalore Lokanatha 🆔 graduated from Bangalore University, presently pursuing her research in VTU, Belagavi. She is currently serving as Assistant Professor in Department of Electronics and Communication, BNMIT, Bengaluru. Her research work is mainly on wireless body area networks and communication. Her area of interest is networking, communication, and signal processing. She can be contacted at email: sujayabl@bnmit.in.

Sompura Basavaraju Bhanu Prashanth 🆔 graduated from Siddaganga Institute of Technology, Tumkur, and pursued M. Tech and Ph.D. at the Indian Institute of Science, Bangalore. He is a member of the ISSS, ISoI, and Chairman of the IEEE Sensors Council, Bangalore section chapter. His special interests are instrumentation techniques, analog circuit design, embedded systems, optical fiber communication, human body area networks, and amorphous semiconductors. He is currently serving B.M.S. College of Engineering, Bangalore, as Professor in the Department of Medical Electronics. He has 30 years of passionate experience in teaching and research. He is a Senior Member of IEEE. He can be contacted at email: bhanu.ml@bmsce.ac.in.