Design methodology for general enhancement of a single-stage self-compensated folded-cascode operational transconductance amplifiers in 65 nm CMOS process

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Article Info

ABSTRACT

The problems resulting from the use of nano-MOSFETs in the design of operational trans-conductance amplifiers (OTAs) lead to an urgent need for new design techniques to produce high-performance metrics OTAs suitable for very high-frequency applications. In this paper, the enhancement techniques and design equations for the proposed single-stage folded-cascode operational trans-conductance amplifiers (FCOTA) are presented for the enhancement of its various performance metrics. The proposed single-stage FCOTA adopts the folded-cascode (FC) current sources with cascode current mirrors (CCMs) load. Using 65 nm complementary metal-oxide semiconductor (CMOS) process from predictive technology model (PTM), the HSPICE2019-based simulation results show that the designed single-stage FCOTA can achieve a high open-loop differential-mode DC voltage gain of 65.64 dB, very high unity-gain bandwidth of 263 MHz, very high stability with phase-margin of 73°, low power dissipation of 0.97 mW, very low DC input-offset voltage of 0.14 uV, high swing-output voltages from −0.97 to 0.91 V, very low equivalent input-referred noise of 15.8 nV/$\sqrt{\text{Hz}}$, very high common-mode rejection ratio of 190.64 dB, very high positive/negative slew-rates of 157.5/58.3 V/us, very fast settling-time of 5.1 ns, high extension input common-mode range voltages from −0.44 to 1 V, and high positive/negative power-supply rejection ratios of 75.5/68.8 dB. The values of the small/large-signal figures-of-merits (*FoMs*) are the highest when compared to other reported FCOTAs in the literature.

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1. INTRODUCTION

Nowadays, high-performance metrics operational trans-conductance amplifier (OTA) circuits play an essential and irreplaceable role in many analog and mixed-signal electronics applications. These OTAs are used by circuit designers in applications of biomedical-signal processing, Internet-of things (IoT), telecommunications, signal converters (A/D and D/A), continuous-time (CT) and switched-capacitor (SC) filters, and low-drop output (LDO) voltage-regulators [1]–[12]. However, the entry of metal–oxide–semiconductor field-effect transistor (MOSFET) transistors into the nano-meter era (100 nm and less) and the accompanying reduction in geometrical sizes (aspect ratios), threshold voltages, trans-conductances and intrinsic-gains of MOSFETs and power-supply voltages (V_{DD}/V_{SS}), led to an urgent need for new design techniques to produce OTAs with high-performance metrics such as high open-loop differential-mode DC

voltage gain ($A_{v,dc}$) and unity-gain bandwidth (GBW), high phase-margin ($\emptyset_M$), high slew-rates ($SR^{\pm}$), low settling-time (T_S), low DC input-offset voltage ($V_{in,os}$), high swing-output voltage ($V_{out,sw}$), and low equivalent input-referred noise ($Noise, ir$), [13]–[17].

Recently, several enhancement techniques have been proposed in the literature to enhance the performance metrics of OTAs, such as double-path bulk-driven (BD) input stage with BD current mirror (CM) load two-stage OTA [4], double-recycling CM-based BD single-stage OTA [8], tailless BD input stage-based two-stage OTA [16], double BD flipped-voltage follower (BDFVF) current source-based two-stage BD OTA [18], and auxiliary common-mode feedback (ACMFB) amplifier in input stage-based fully-differential BD two-stage OTA [19]. These proposed techniques have enhanced some of the performance metrics of the OTAs, such as $A_{v,dc}$ and $SR^{\pm}$, which are useful in the field of low-frequncy applications such as biomedical applications. However, these techniques have led to an increase in the OTAs architecture complexity as they use large compensation/load capacitors, due to extra pairs of the pole and zero at the internal/output nodes, these are not useful in terms of silicon area on the chip, as well as have increased the $Noise, ir$ because of the use of pMOSFETs in the input-stage [2], [5], [6], [20], [21].

Furthermore, other enhancement techniques have been proposed to enhance the performance metrics of the OTAs used in high $A_{v,dc}$ and GBW applications, such as high-swing ($V_{out,sw}$) CM-based single-stage folded cascode OTA (FCOTA) [22], high $V_{out,sw}$ CM-based two-stage FCOTA [23], quadruple-recycling (QR) single-stage FCOTA [24], and self-biasing CM-based improved nonlinear (INL) two-stage recycling folded cascode (RFC) OTA [25]. These proposed techniques have enhanced all performance metrics of the CM-based FCOTA except that the power dissipation (P_{dis}) of the two-stage FCOTA is greater than that of the single-stage FCOTA. Therefore, in order to enhance all the performance metrics of the FCOTA, including the P_{dis}, it is preferable to use a simple cascode CM (CCMs)-based single-stage FCOTA, which also provides a self-frequency compensation with load capacitor (C_L) [26]–[30].

In this paper, a design methodology that includes design techniques and equations for a low-voltage (LV) generally enhanced single-stage FCOTA with a FC current source and a simple CCMs load is presented. It presents an enhancement in the trans-conductances (g_m), output resistance (R_{out}), $A_{v,dc}$, GBW, $SR^{\pm}$, T_S, $V_{in,os}$, $V_{out,sw}$, $Noise$, and ir. The organization of the rest of this paper is as follows: in section 2, the description, enhancement techniques, and design equations of the proposed FCOTA are presented. HSPICE 2019 simulation-based results are presented in section 3. Finally, section 4 concludes this paper.

2. DESIGN METHODOLOGY

In this section, a brief description of the proposed FCOTA along with techniques for enhancement its various performance metrics are presented first. Then, the equations for the proposed FCOTA design are presented. This section's techniques and equations introduce essential concepts simplified for designing the proposed single-stage self-compensated FCOTA with high-performance metrics.

2.1. FCOTA description and enhancement techniques

The schematic structure of the proposed FCOTA is shown in Figure 1. This structure is favorable over RFCOTA and two-stage FCOTA for larger g_m, comparable $A_{v,dc}$, higher GBW, better $V_{out,sw}$ and input common-mode range voltage ($V_{in,cm}$), larger $SR^{\pm}$, better power-supply rejection ratios ($PSRR^{\pm}$) and common-mode rejection ratio (CMRR), it has a class AB (push-pull) output.
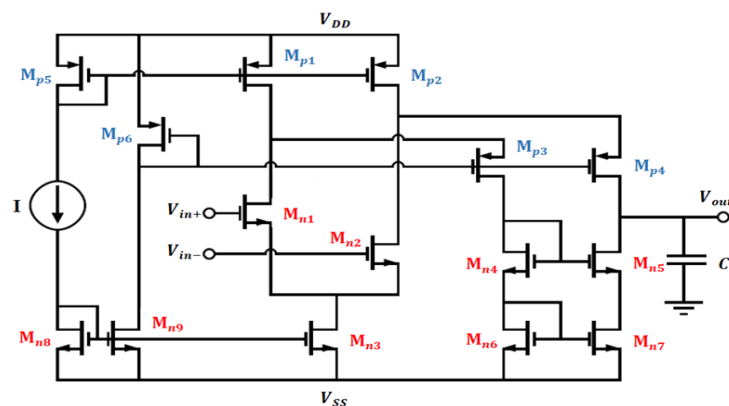

Figure 1. The proposed FCOTA

In this proposed FCOTA, the differential-input core consists of the nMOSFETs drivers M_{n1} and M_{n2}. The use of nMOSFETs drivers instead of pMOSFETs drivers in the differential-input is a good alternative in enhancing the $A_{v,dc}$, GBW, and other performance metrics of the FCOTA because the $g_{m,n}$ of nMOSFETs are much greater than the $g_{m,p}$ of pMOSFETs. The FC current sources consist of the pMOSFETs M_{p1}, M_{p2}, M_{p3}, and M_{p4}. The drain trminals of M_{n1} and M_{n2} are connected to the drain terminals of the pMOSFETs FC current sources M_{p1} and M_{p2}, respectively, thus this extends the maximum $V_{in,cm}$. The nMOSFET M_{n3} represents the tail-current source. The simple CCMs that consist of the nMOSFETs M_{n4}, M_{n5}, M_{n6}, and M_{n7} represent the load of the FCOTA. This CCMs load increases the R_{out} at output node and thus enhances the $A_{v,dc}$, UGB, $V_{out,sw}$, $SR^{\pm}$, T_S, and other performance metrics of the FCOTA. Furthermore, the CCMs load provides single-ended conversion and self-frequency compensation with C_L without the need for Miller or other frequency compensation techniques. The DC bias current and voltages are provided by the DC bias circuit block that ensures all MOSFETs in the proposed FCOTA are polarized in their saturation regions. This DC bias circuit consists of a current source (I), pMOSFETs M_{p5} and M_{p6}, and nMOSFETs M_{n8} and M_{n9}.

2.2. FCOTA design equations

For the proposed FCOTA, shown in Figure 1, the square-laws of the nMOSFETs and pMOSFETs drain bias currents ($I_{D,n,p}$), listed in (1) and (2), are used to design the practical aspect ratios ($S_{n,p}$) of all MOSFETs, as listed in (3) to (8).

$$I_{D,n,p} = \frac{K'_{n,p}W_{n,p}}{2L_{n,p}} (V_{GS,n,p} - V_{th,n,p})^2 \left(1 + \lambda_{n,p} V_{DS,n,p}\right) \tag{1}$$

$$I_{D,p1,p2} = 1.2I_{D,n3} \; to \; 1.5I_{D,n3} \tag{2}$$

where $W_{n,p}$ is the n,pMOSFET channel length, $L_{n,p}$ is the n,pMOSFET channel width, $K'_{n,p}$ is the n,pMOSFET trans-conductance parameter, $V_{GS,n,p}$ is the gate-source voltage of n,pMOSFET, $V_{th,n,p}$ is the threshold voltage of n,pMOSFET, $\lambda_{n,p}$ is the channel-length modulation parameter of n,pMOSFET, and $V_{DS,n,p}$ is the n,pMOSFET drain-source voltage.

$$S_{n,p}|_i = \begin{cases} (W_n/L_n)_i, & i = 1 \; to \; 9 \\ (W_p/L_p)_i, & i = 1 \; to \; 5 \end{cases} \tag{3}$$

Such that,

$$S_{n1} = S_{n2} \tag{4}$$

$$S_{n3} = S_{n8} = S_{n9} \tag{5}$$

$$S_{n4} = S_{n5} = S_{n6} = S_{n7} \tag{6}$$

$$S_{p1} = S_{p2} = S_{p3} = S_{p4} \tag{7}$$

$$S_{p5} = \left(I/I_{D,p1}\right)S_{p1} \tag{8}$$

The listed practical design (9) to (18) cover the proposed FCOTA important performance metrics. The slew rate ($SR^{\pm}$) is given by (9):

$$SR^{\pm} = I_{D,n3}/C_L \tag{9}$$

The GBW is given by (10):

$$GBW = g_{m,n1,n2}/(2\pi C_L) \tag{10}$$

The maximum $V_{in,cm}$ is:

$$V_{in,cm(max)} = V_{DD} - V_{SD,p1,p2} + V_{th,n1,n2} \qquad (11)$$

The minimum $V_{in,cm}$ is:

$$V_{in,cm(min)} = V_{SS} + V_{DS,n3} + V_{GS,n1} \qquad (12)$$

The $V_{out,sw}$ is:

$$V_{SS} + V_{th,n4,n5,n6,n7} + 2V_{DS,n4,n5,n6,n7} \leq V_{out,sw} \leq V_{DD} - 2V_{SD,p1,p2,p3,p4} \qquad (13)$$

The single-dominant pole at the high-impedance output node is given by (14).

$$p_{dominant} = -1/(R_{out}C_L) \qquad (14)$$

The total R_{out} at the output node is given by (15).

$$R_{out} = (g_{m,n5}r_{ds,n5}r_{ds,n7}) \parallel [g_{m,p4}r_{ds,p4}(r_{ds,n2} \parallel r_{ds,p2})] \qquad (15)$$

Therefore, the small-signal $A_{v,dc}$ becomes:

$$A_{v,dc} = \left[\frac{1+(k_{lf}/2)}{1+k_{lf}}\right](g_{m,n1,n2}R_{out}) \qquad (16)$$

where k_{lf} is an unbalanced low-frequency parameter given by (17).

$$k_{lf} = [(g_{m,n5}r_{ds,n5}r_{ds,n7})(g_{ds,n2} + g_{ds,p2})]/(g_{m,p4}r_{ds,p4}) \qquad (17)$$

Finally, the total P_{dis} is given by (18):

$$P_{dis} = (V_{DD} + |V_{SS}|)(I + I_{D,n9} + I_{D,n3} + I_{D,n6} + I_{D,n7}) \qquad (18)$$

3.   RESULTS AND DISCUSSION

The proposed single-stage self-compensated FCOTA is designed with 65 nm PTM-BSIM4 CMOS process. The performance metrics results in the open-loop differential-mode and unity-gain negative feedback-mode of the proposed single-stage self-compensated FCOTA are simulated using HSPICE2019 software and their waveforms are plotted using Synopsys CosmosScope tool. In addition, the DC biasing current (I) is set to 100 uA at the $V_{DD}/|V_{SS}|$ of 1V, and C_L is set to 0.5 pF. Besides, Based on the iterative design equations and HSPICE2019 software simulations to have trade-offs between high $A_{v,dc}$, GBW, $V_{out,sw}$, $SR^{\pm}$, low T_S, and other performance metrics, the $S_{n,p}$ values of all n,pMOSFETs are reported in Table 1.

Table 1. Size of nMOSFETs and pMOSFETs

MOSFET	$M_{n1,2}$	$M_{n3,8,9}$	$M_{n4,5,6,7}$	$M_{p1,2,3,4}$	M_{p5}	M_{p6}
$S_{n,p}$ $(\mu m/\mu m)$	11.487/0.3	6.9/0.3	8.922/0.3	8.1/0.3	5.661/0.3	1.416/0.3

3.1. Open-loop differential-mode response

The proposed FCOTA was simulated in the open-loop differential-mode to determine the efficiencies of its performance metrics by measuring the various performance metrics associated with it in this mode. Figure 2 depicts the simulated AC small-signal frequency responses of the proposed FCOTA. The FCOTA achieves $A_{v,dc}$ of 65.64 dB, GBW of 263 MHz, and $\emptyset_M$ of 73°. These simulation results confirm that the proposed FCOTA has a high $A_{v,dc}$, very high GBW, and very high stability.

Figure 3 depicts the simulated $V_{in,os}$ and $V_{out,sw}$ responses of the proposed FCOTA. The measured $V_{in,os}$ is 0.14 uV and $V_{out,sw}$ is swing from −0.97 to 0.91 V. Consequently, the proposed FCOTA has a perfect $V_{in,os}$ and high $V_{out,sw}$ close to positive/negative-rail values (V_{DD}/V_{SS}).

The P_{dis}, input resistance (R_{in}), and R_{out} of the proposed FCOTA are foun to be 0.97 mW, 59.4 MΩ, and 2.2 MΩ, respectively. Figure 4 depicts the simulated $Noise, ir$ frequency response of the proposed FCOTA. The FCOTA achieves $Noise, ir$ of 15.8 nV/$\sqrt{Hz}$ at 1 MHz. Consequently, the proposed FCOTA has a very high noise rejection from the internal/external noise sources.
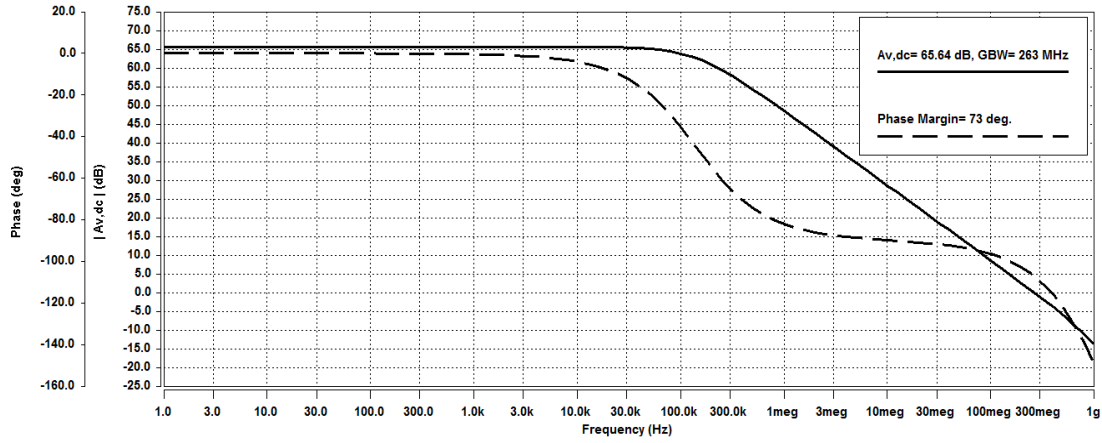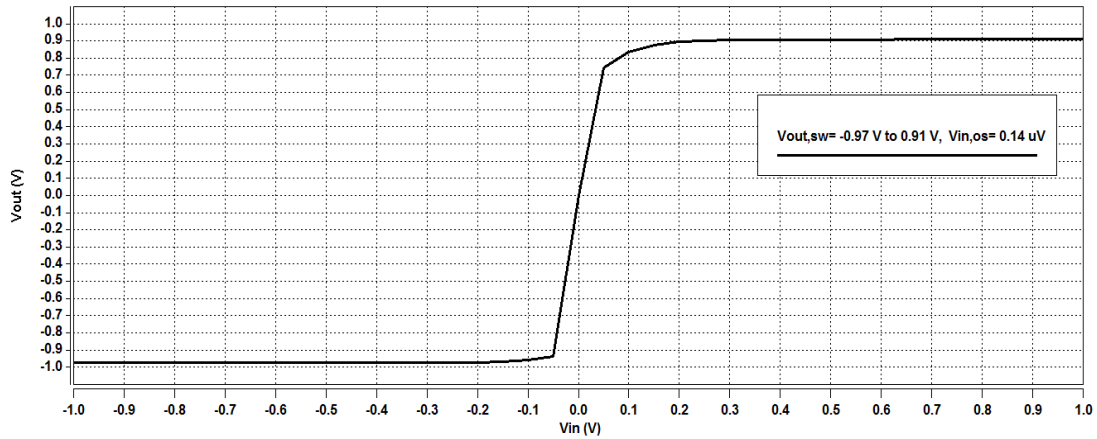

Figure 2. Simulated gain and phase responses

Figure 3. Simulated DC input-offset voltage and output voltage-swing responses
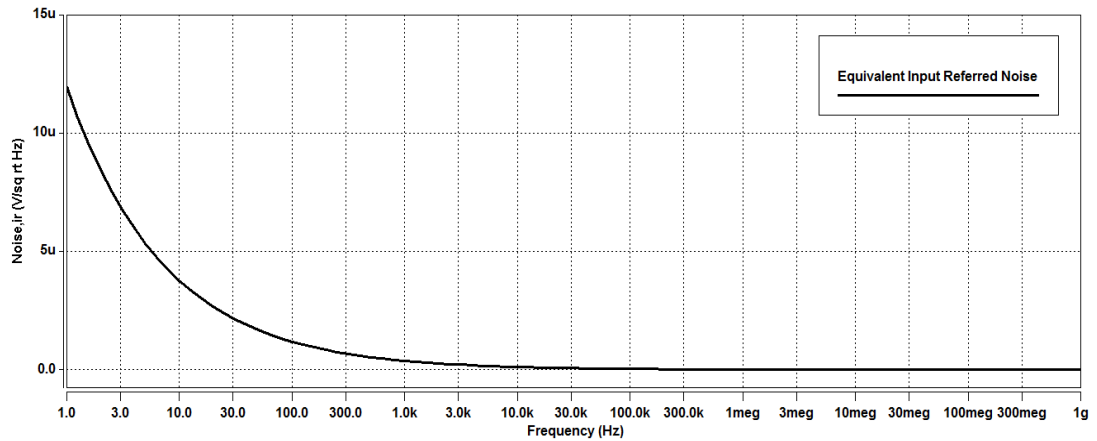
Figure 4. Simulated equivalent input-referred noise response

3.2. Common-mode response

The proposed FCOTA was simulated in the common-mode to determine its CMRR performance metric efficiency. Figure 5 depicts the simulated common-mode voltage gain ($A_{v,cm}$) frequency response of the proposed FCOTA. The FCOTA achieves $A_{v,cm}$ of -125 dB. Consequently, the achieved very high CMRR is found to be 190.64 dB.
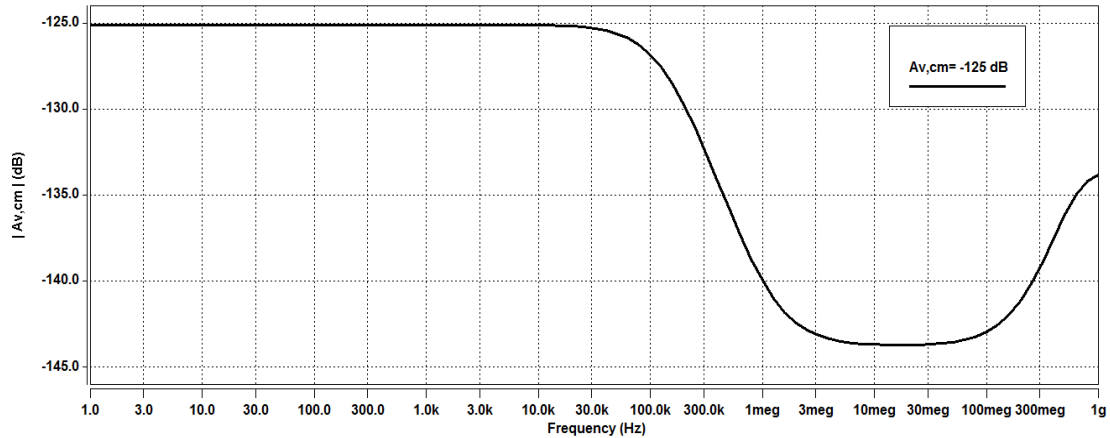

Figure 5. Simulated common-mode voltage gain response

3.3. Unity-gain negative feedback-mode response

The proposed FCOTA was simulated in the unity-gain negative feedback-mode to determine the efficiencies of its performance metrics by measuring the various performance metrics associated with it in this mode. Figure 6 depicts the simulated positive/negative $SR^{\pm}$ and T_S transient responses of the proposed FCOTA. The FCOTA achives positive/negative $SR^{\pm}$ of 157.5/58.3 V/us, and T_S of 5.1 ns. These simulation results confirm that the proposed FCOTA has a very high stability and very fast settling-time.
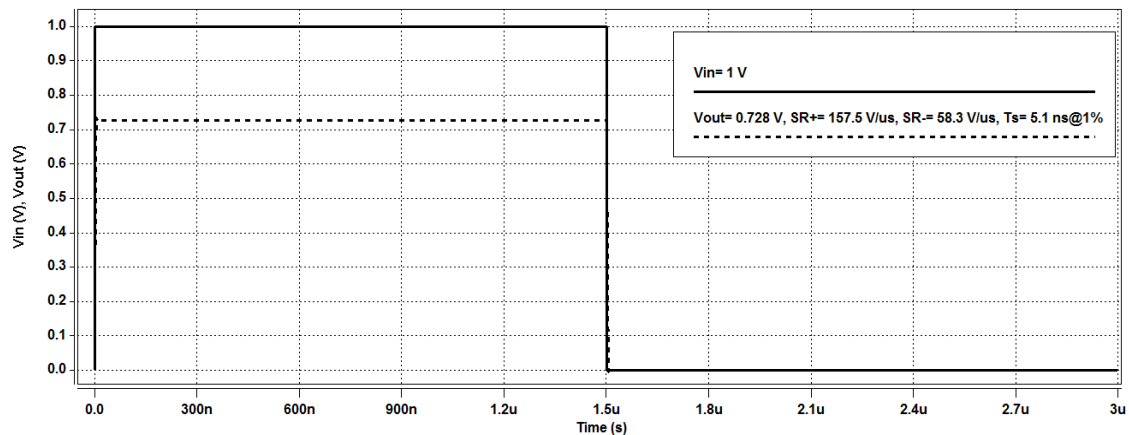

Figure 6. Simulated slew-rates and settling-time responses

Figure 7 depicts the simulated minimum/maximum $V_{in,cm}$ responses of the proposed FCOTA. The $V_{in,cm(min)}$ is -0.44 V and $V_{in,cm(max)}$ is 1 V. Consequently, the proposed FCOTA has a high extension maximum $V_{in,cm}$ equal to the positive-rail value (V_{DD}).

Figures 8 and 9 depict the simulated positive/negative $PSRR^{\pm}$ frequency responses of the proposed FCOTA, respectively. The FCOTA achieves positive $PSRR^{+}$ of 75.5 dB and negative $PSRR^{-}$ of 68.8 dB. These simulation results confirm that the proposed FCOTA has high ripples/noise rejections from the V_{DD}/V_{SS} sources.
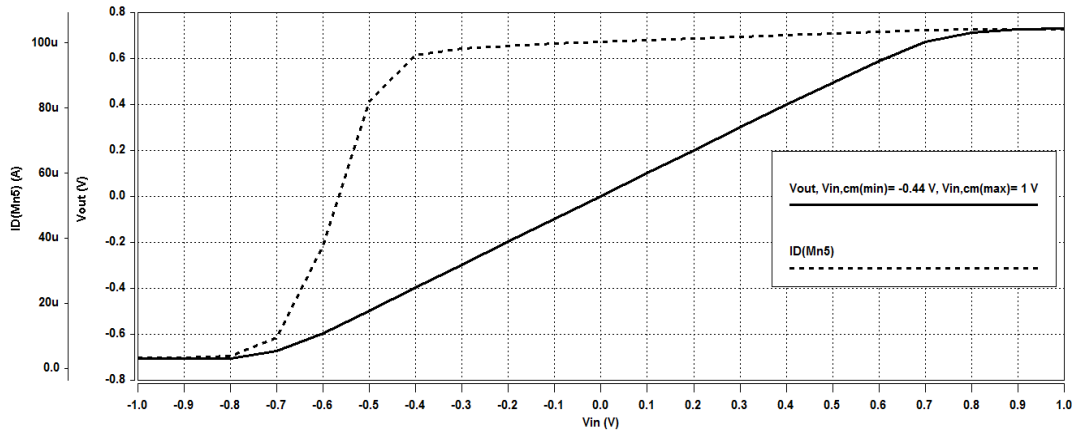
Figure 7. Simulated minimum/maximum input common-mode voltage responese
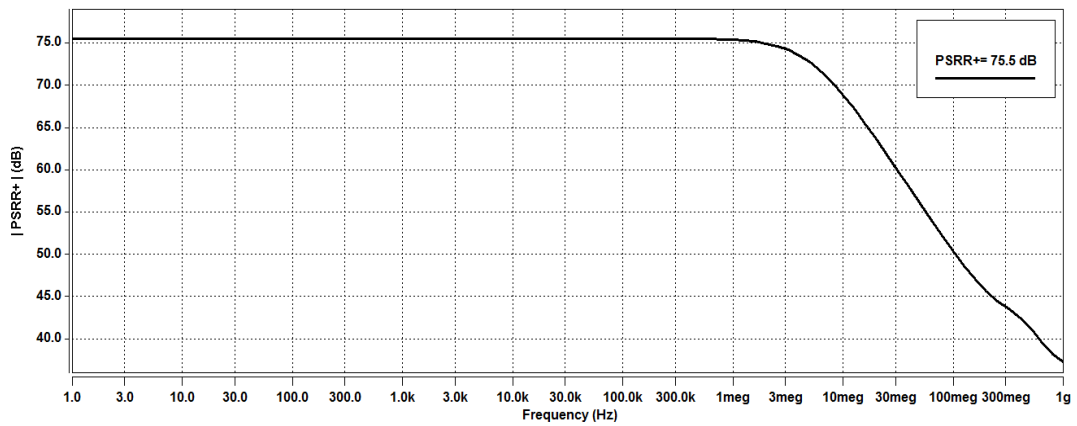

Figure 8. Simulated positive power-supply rejection ratio response
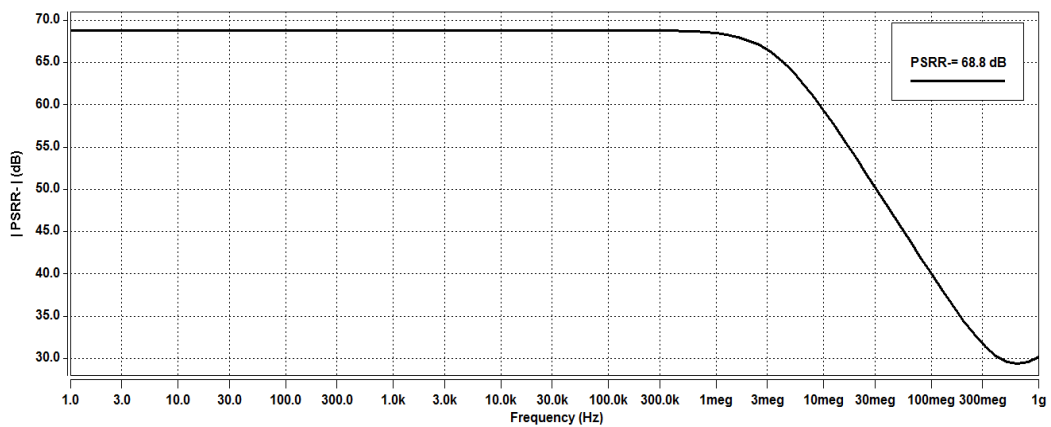

Figure 9. Simulated negative power-supply rejection ratio response

3.4. Design performance metrics comparison

The simulated performance metrics of the designed FCOTA have been compared with the prior works. The results of the performance metrics comparisons are summarized in Table 2. The designed FCOTA has substantiated to be an excellent contribution in the field of state-of-the-arts single-stage FCOTAs because it has the highest small/large-signal figures-of-merits ($FoMs$), FoM_{SS}, FoM_{LS}, $IFoM_{SS}$, and $IFoM_{LS}$, respectively.

Table 2. Summary of performance metrics comparisons

Parameter	[3]	[5]	[6]	[7]	[9]	[10]	[11]	[13]	[15]	[20]	[22]	[24]	[25]	[26]	This work
Process (nm)	130	130	130	130	350	180	180	90	350	500	130	180	180	90	65
Supply (V)	1	3.3	1.2	±0.5	±2.5	1.8	1.8	1.2	0.9	±1	1.2	1.8	1	1.2	±1
$A_{v,dc}$ (dB)	92	58	156	63.88	80.15	72	98	62	65	76.8	65.27	95.82	92.3	66.2	65.64
GBW (MHz)	0.141	202	63	4.48	14	86.5	21	164	1	3.4	29.24	182.81	6.51	190	263
$\varnothing_M$ (°)	79	52	74	61	75.3	50	71	50	60	75.1	54.17	40.08	75.81	81	73
$V_{in,os}$ (uV)	−14	45000	n/a	n/a	n/a	n/a	14600	n/a	4600	n/a	n/a	n/a	n/a	n/a	0.14
SR_{avg} (V/us)	0.03	35.04	69.5	6.4	12.307	74.1	51	39.3	0.25	19.25	0.2	78.4	15.19	71	107.9
T_S (ns)	n/a	80 at 1%	40 at 0.1%	n/a	n/a	n/a	n/a	13.8 at 1%	1800 at 1%	120 at 1%	53.9 at 1%	n/a	94 at 1%	7.25 at 1%	5.1 at 1%
CMRR (dB)	87	104.8	119	56.7	88.94	100	n/a	66	45	112	69.5	n/a	133.5	n/a	190.64
$PSRR^{\pm}$ (dB)	86	62.6	200/198	61.5/71.9	84.6/100.3	100	n/a	n/a	51	92/113	n/a	n/a	92.4/128.6	n/a	75.5/68.8
$Noise, ir$ $\left(\frac{nV}{\sqrt{Hz}}\right)$	220 at 10 KHz	3.06 at 195 MHz	4 at 1 MHz	27.5 at 1 MHz	n/a	1.13 at 100 KHz	250 at 100 KHz	n/a	65 at 100 KHz	23 at 1 MHz	n/a	n/a	15.8 at 1 MHz	3800 at 10 MHz	15.8 at 1 MHz
P_{dis} (uW)	130	3630	686	30	2144	11900	3000	672	72	100	352.7	1224	50	6720	970
FoM_{SS} $\left(\frac{MHz.dB.deg}{uW}\right)$	1035.13	167.83	106.16	581.90	39.40	26.16	48.70	756.54	54.16	196.10	293.11	573.59	911.04	151.60	1299.19
FoM_{LS} $\left(\frac{V.MHz.dB}{us.uW}\right)$	0.39	113.09	995.69	61.05	6.44	38.78	34.98	594.64	0.22	50.26	1.08	1121.99	182.54	132.89	1920.32
$IFoM_{SS}$ $\left(\frac{MHz.dB.deg}{uA}\right)$	1035.13	553.84	11019.27	581.90	131.91	311.40	87.70	907.85	144.44	1961.01	1406.57	3510.37	911.04	727.72	12602.22
$IFoM_{LS}$ $\left(\frac{V.MHz.dB}{us.uA}\right)$	0.39	373.20	10349.18	61.05	21.56	461.49	63	713.57	0.60	502.65	5.19	6866.60	182.54	637.88	18627.12

4. CONCLUSION

The enhancement techniques and design equations are presented in this paper to improve the performance metrics of the proposed single-stage FCOTA. The FC current sources with CCMs load techniques are used to improve the various performance metrics, provide single-ended conversion, and self-frequency compensation with C_L of the designd single-stage FCOTA. This single-stage FCOTA design at the $V_{DD}/|V_{SS}|$ values of 1V achieves an open-loop differential-mode DC voltage gain of 65.64 dB, GBW of 263 MHz, $\varnothing_M$ of 73°, low P_{dis} of 0.97 mW, $V_{in,os}$ of 0.14 uV, $V_{out,sw}$ from −0.97 to 0.91 V, $Noise, ir$ of 15.8 nV/$\sqrt{Hz}$, CMRR of 190.64 dB, positive/negative $SR^{\pm}$ of 157.5/58.3 V/us, T_S of 5.1 ns, minimum/maximum $V_{in,cm}$ from −0.44 to 1 V, and positive/negative $PSRR^{\pm}$ of 75.5/68.8 dB. Indeed, the designed single-stage FCOTA has achieved the highest small/large $FoMs$ values of any other state-of-the-arts FCOTAs. Accordingly, the designed single-stage FCOTA has proven its effective contribution in the field of state-of-the-arts single-stage FCOTAs.

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