

Open-circuit fault resilient ability multi level inverter with reduced switch count for off grid applications

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Article Info

Article history:

Received Apr 17, 2021

Revised Dec 22, 2021

Accepted Jan 2, 2022

Keywords:

Fault resilient ability

Multi-level inverter

Phase disposition pulse width modulation

Reliability

ABSTRACT

In a multi-level inverter (MLI), the switching component number effect on volume and reliability is a major concern in on-grid and off-grid applications. The recent trend in MLI, reduced component number of power switches, and capacitors in multi-level inverter topologies have been driven for power conversion. The concept of fault tolerance is not considered in many such configurations; due to this the reliability of the MLI is very low. So now it is a major research concern, to develop a strong fault resilient ability power electronic converter. In this work, a novel configuration of a multilevel inverter with a lower switch count is proposed and analyzed with fault tolerance operation for improvement of reliability. Generally, the fault-tolerant operation is analyzed in only any one of the switches in MLI. But the proposed topology is concerned with multiple switch fault tolerance. Further, the phase disposition pulse width modulation (PDPWM) control scheme is utilized for the operation of the proposed inverter topology. The proposed inverter topology is simulated in MATLAB/Simulink environment under normal and faulty condition; the results are obtained and validated.

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1. INTRODUCTION

Day to day increment of utilization of electrical energy and for the future generation of electrical energy it should be focused on non-conventional energy sources (NCES). Due to shortage of fossil fuels and without any pollution effect, the NCES are more predominant in generation of electrical power [1]. Due to rapid development of power electronic control techniques in electrical power generation and more advantages of solar photovoltaic (PV) systems, the solar photovoltaic (SPV) systems are used in many industrial and residential applications. In order to utilize this SPV power, for this application two stage power conversion is required. But to avoid the increment of losses and improve the efficiency the single stage power conversion of two level inverters are used [2], [3]. The conventional two level inverters are having, high harmonic content, more switching losses, and lower fundamental magnitude.

To overcome these drawbacks in traditional 2-level inverters, the multi-level inverter (MLI) are predominantly developed with the help of power electronic devices for medium and high voltage applications [4], [5]. The output voltage of MLIs is in stepped in nature, and then the error between the reference waveform to actual waveform may reduce. So, the MLIs are having less harmonic content with improved performance with development of pulse width modulation technique for switching operation of devices [6]. The MLI are having in different configurations such as diode clamped [7], flying capacitor [8] and cascaded H-bridge inverters [9]. But to enhance the voltage levels, the number devices are required more

and the switching losses are higher in the above type of configurations. Also, the sharing of voltage across each device is also not in same. So, the new topologies of MLI are introduced with modular of addition and subtraction of sources for lower switching losses along with equal sharing voltage across each device, which are hybrid multilevel inverters [10]–[12].

In off grid or islanded application, the solar PV power generation systems are more preferable as compared to other non-conventional energy sources [13], [14]. Generally, a small scale power supply network in remote areas will operated in off grid application. But the probability of power failure issues, because of source and switches of inverter topologies are more. So, this effect may cause to damage the solar PV system and it requires more time to settle in steady state. To avoid these issues, the MLI are operated with fault resilient ability technique for SPV systems without any interruption of power supply to loads [15], [16]. In study [17], the multilevel inverter with a switch failure problem under fault condition and in study [18], coupled Scott transformer based fault-tolerant configuration for grid connected fed solar PV system is presented. Generally, under normal operation the MLI operates with less number of switches, but under faulty operation the extra leg of switch is replace with fault switch. In study [19], the three level inverter with T type topology is discussed with fault resilient control strategy for open circuits faults without extra devices. The fault tolerant in CHB inverter is analyzed by using a network of relays [20]. Furthermore, the configuration has been altered to protect the switches against larger blocking voltages with extra devices. The reduced switch count inverter configuration is designed in [21] to overcome the problem in [22]. But the inverter configuration is required polarity changer circuit which is not needed in fault tolerant [23]. The pre-fault ability of output power is provided in [24], without increasing the ripple voltage across capacitor is designed under fault condition. But the output power must increases in it, due to active switches are placed instead of faulty switches under abnormal operation. In [25], the open and short circuit faulty operation of switches is discussed in inverter configuration with placing redundant switches [26].

In this paper, to overcome the above mentioned drawbacks the single phase multilevel inverter topology with low switch count for off grid application with fault resilient ability technique is proposed. The proposed technique is having more capability, when open circuit fault occurs across the source or switch. The proposed topology is more reliable with less number of switches and a very small modification in switching operation. The paper is organized as follows. The proposed MLI configuration with less number of switches is described in section 2. In section 3 generation of voltage levels across the load for proposed inverter, the proposed inverter under normal and faculty condition operation explained, and also switching signal generation of the multilevel inverter is described. The MATLAB simulation results of the proposed inverter configuration are analyzed in section 4. The conclusion of the proposed work is mentioned in section 5.

2. PROPOSED SYSTEM CONFIGURATION

The schematic diagram as shown in Figure 1 is proposed configuration of fault resilient ability MLI with optimized switches for single phase. It consists of main inverter with six unidirectional switches and three redundant bidirectional switches. The main inverter is for the production of seven output voltage levels and the redundant switches are for improving the fault resilient ability.

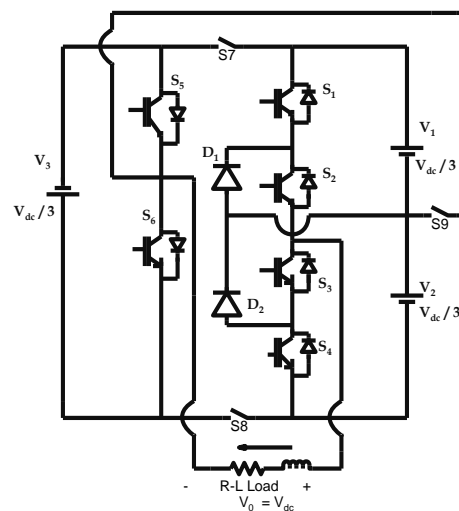


Figure 1. Schematic diagram of a fault resilient ability seven level inverter

The proposed novel seven-level inverter topology is designed by parallel connection of neutral point diode clamped three-level inverter with half-bridge two-level inverter through one redundant switch. It consists of three DC symmetrical voltage sources. The load must be placed between the neutral point diode clamped inverter and half-bridge inverter circuit. In general, almost all residential and industrial application the load may considered as inductive load, so for the off grid applications the proposed system is analyzed with RL-load.

3. OPERATION AND MODULATION TECHNIQUE

In order to operate the proposed inverter configuration for generation of seven level output voltage the phase disposition pulse width modulation switching technique is presented.

3.1. Modes of operation of proposed inverter

To understand the principal operation of proposed novel 1-phase 7-level inverter is explained in various modes with generation of seven voltage levels and also provided the direction of flow of current from source to load. In each mode of operation, the active switches are appeared in Figure 2 (in Appendix) under normal operation or without any faulty. The switching combination for production of seven level output voltages is presented in Table 1 under normal operation i.e., without fault operation. The seven modes of operations:

- Mode 1: The switches S1, S2, S5 and S8 are enabled to activate and remaining switches are deactivated, then the combination of switches action the load voltage is produced, which is equal to V_{dc} volts. Because of all three-voltage source module of addition the highest magnitude of voltage is produced across the load. The operation of active circuit with direction of flow of current is appeared in Figure 2(a).
- Mode 2: The switches S1, S2, S6 and S8 are enabled to activate and remaining switches are deactivated, then the combination of switches action the load voltage is produced, which is equal to $2 V_{dc}/3$ volts. Because of two voltages source addition the medium magnitude of voltage is produced across the load. The operation of active circuit with direction of flow of current is appeared in Figure 2(b).
- Mode 3: The switches S3, S4, S5 and S8 are enabled to activate and remaining switches are deactivated, then the combination of switches action the load voltage is produced, which is equal to $V_{dc}/3$ volts. Because of single voltage source presents the low magnitude of voltage is produced across the load. The operation of active circuit with direction of flow of current is appeared in Figure 2(c).
- Mode 4: The switches S1, S2, S5 and S7 are enabled to activate and remaining switches are deactivated, then the combination of switches action the load voltage is produced, which is equal to Zero volts. Because the short circuit of the all the switches with respect to load, the zero magnitude of voltage is placed across the load. The operation of active circuit with direction of flow of current is appeared in Figure 2(d).
- Mode 5: The switches S1, S2, S6 and S7 are enabled to activate and remaining switches are deactivated, then the combination of switches action the load voltage is produced, which is equal to $-V_{dc}/3$ volts. Because of single voltage source presents the low magnitude of voltage is produced across the load with negative polarity. The operation of active circuit with direction of flow of current is appeared in Figure 2(e).
- Mode 6: The switches S3, S4, S5 and S7 are enabled to activate and remaining switches are deactivated, then the combination of switches action the load voltage is produced, which is equal to $-2 V_{dc}/3$ volts. Because of two voltages source addition the medium magnitude of voltage is produced across the load with negative polarity. The operation of active circuit with direction of flow of current is appeared in Figure 2(f).
- Mode 7: The switches S3, S4, S6 and S7 are enabled to activate and remaining switches are deactivated, then the combination of switches action the load voltage is produced, which is equal to $-V_{dc}$ volts. Because of all three voltages source module of addition the highest magnitude of voltage is produced across the load with negative polarity. The operation of active circuit with direction of flow of current is appeared in Figure 2(g).

In off grid or islanded application, the solar PV power generation systems are more preferable as compared to other non-conventional energy sources. Generally, a small scale power supply network in remote areas will operated in off grid application. But the probability of power failure issues, because of source and switches of inverter topologies are more. So, this effect may cause to damage the solar PV system and it requires more time to settle in steady state. To avoid these issues, the multilevel inverter are operated with fault resilient ability technique for solar PV systems without any interruption of power supply to loads, which already discussed in introduction also.

Table 1. Switching strategy under normal operation for seven-level output voltage

Magnitude of voltage	S1	S2	S3	S4	S5	S6	S7	S8	S9
V_{dc}	1	1	0	0	1	0	0	1	0
$2(V_{dc}/3)$	1	1	0	0	0	1	0	1	0
$V_{dc}/3$	0	0	1	1	1	0	0	1	0
0	1	1	0	0	1	0	1	0	0
$-V_{dc}/3$	1	1	0	0	0	1	1	0	0
$-2(V_{dc}/3)$	0	0	1	1	1	0	1	0	0
$-V_{dc}$	0	0	1	1	0	1	1	0	0

3.2. Modes of operation of proposed inverter under fault condition

In the proposed inverter, if any one of the switch damages it means it may act as open circuit fault in that case the inverter unable to procure the same number of output voltage levels. But with fault resilient ability technique will providingthecontinues power to load with reduced number of levels. If one of the switches has faulted, it produces five numbers of output voltage levels and similarly two switches at time having faulty condition; it produces three level output voltages. The switching strategy is shown in Table 2 under faulty condition.

The Figure 3(a) represents positive higher voltage level, the switches S2, S5 and S8 are enabled to activate and remaining switches are deactivated, Figure 3(b) denotes the positive middle voltage level, the switches S2, S6 and S8 are enabled to activate and remaining switches are deactivated, Figure 3(c) shows the zero voltage level, the switches S3,S4, S6, and S8 are enabled to activate and remaining switches are deactivated, Figure 3(d) represents the negative middle voltage level, the switches S3, S4 and S9 are enabled to activate and remaining switches are deactivated, and Figure 3(e) denote the negative higher voltage level during single switch failure, The switches S3, S6, and S7 are enabled to activate and remaining switches are deactivated. The modes of operation of proposed inverter with single switch failure condition is explained in detail and it also shows the production of five level output voltages across the load. The single switch S1 is considered for the analysis. If any of other single switch also failure to operate, then similar to the S1 operation, the five level of output voltages are produces across load, but the switching sequence operation changes. Figure 3 see in Appendix.

Table 2. Switching strategy under fault condition

	Switches levels	S1	S2	S3	S4	S5	S6	S7	S8	S9
Case-I: During Fault Resilient of switch S1	$2 V_{dc}/3$	0	1	0	0	1	0	0	1	0
	$V_{dc}/3$	0	1	0	0	0	1	0	1	0
	0	0	0	1	1	0	1	0	1	0
	$- V_{dc}/3$	0	0	1	1	0	0	0	0	1
	$-2 V_{dc}/3$	0	0	1	0	0	1	1	0	0
During Fault Resilient of switch S2	$2 V_{dc}/3$	0	0	1	1	0	0	1	1	1
	$V_{dc}/3$	0	0	1	1	1	0	0	1	0
	0	0	0	1	1	0	1	0	1	0
	$-V_{dc}/3$	0	0	1	0	1	1	0	0	1
	$-2 V_{dc}/3$	0	0	1	0	0	1	1	0	0
During Fault Resilient of switch S3	$2 V_{dc}/3$	0	1	0	0	1	0	0	1	0
	$V_{dc}/3$	0	1	0	0	0	1	0	1	0
	0	1	1	0	0	1	0	1	0	0
	$-V_{dc}/3$	1	1	0	0	0	1	1	0	0
	$-2 V_{dc}/3$	1	1	0	0	1	1	0	0	1
Case-II: during fault resilient of switch S1 and S5	$V_{dc}/3$	0	1	0	0	0	1	0	1	0
	0	0	0	1	1	0	1	0	1	0
	$- V_{dc}/3$	0	0	1	1	0	0	0	0	1
During Fault Resilient of switch S1 and S6	$V_{dc}/3$	0	0	1	1	0	0	0	0	1
	0	0	0	1	0	0	0	0	0	1
	$-V_{dc}/3$	0	0	1	0	1	0	1	0	0
During Fault Resilient of switch S2 and S5	$V_{dc}/3$	0	0	1	1	0	0	0	0	1
	0	0	0	1	0	0	0	0	0	1
	$-V_{dc}/3$	1	0	1	0	0	0	0	0	1

3.3. Modulation technique

To produce switching signals, for the intended inverter operation phase disposition pulse width modulation technique is utilized. The PD-PWM techniques similar to Sinusoidal pulse width modulation technique only, but the number carrier signals are more than one and which have different magnitude levels. To generate switching signal, the reference signal sinusoidal waveform is compared with every magnitude

level of carrier triangular signal. When the reference signal magnitude is more than the carrier signal at every level, the pulses generated which are applied to the inverter switches. The PD-PWM switching strategy waveforms are shown in Figure 4. The Figure 4(a) PD-PWM strategy is applicable when the inverter is operating under normal operation or without any fault switch. If any one of the switches is failed to operate, but for continuous power deliver to the load. The switching sequence of operation will be changes. In Figure 4(b) the PD PWM strategy for switching operation under faulty condition of single switch failure condition is shown. Similarly, the Figure 4(c) shows that the PD PWM strategy of two switches failure condition.

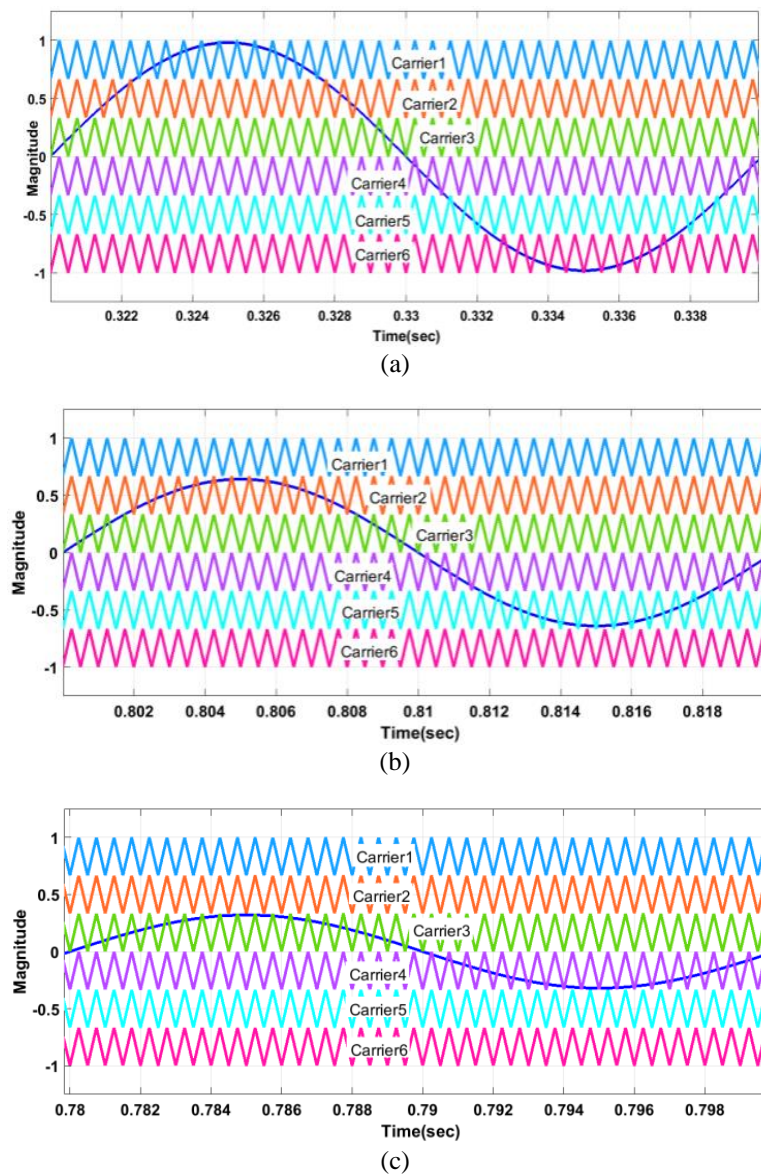


Figure 4. PDPWM under different conditions: (a) PDPWM control strategy with normal condition, (b) PDPWM control strategy for single switch fault condition and (c) PDPWM control strategy for dual switches failure operation

4. SIMULATION RESULTS AND ANALYSIS

In this section, the proposed single phase MLI with and without faulty operation is discussed based on the simulation results. The simulation of the inverter configuration is done in MATLAB/Simulink software tool. For analysis of off grid application, the load is considered as RL-load i.e., partially inductive load. For the simulation of inverter configuration, the following parameters are considered in Table 3. In Figure 5(a)-(d), the Figure 5(a) shows that the output current and voltage waveforms of proposed inverter

with partially inductive load i.e., RL-load for the modulation index of 0.98. It has shown the inverter under normal operation that means without any switch failure.

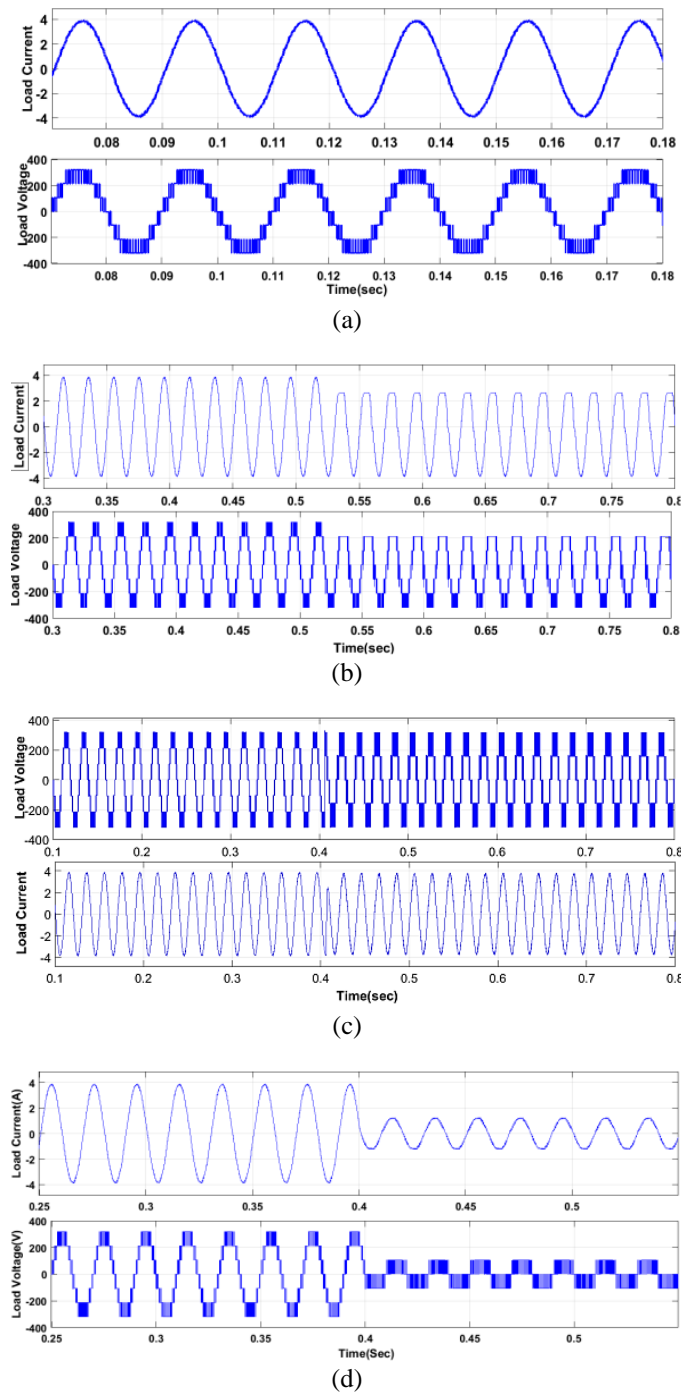


Figure 5. Voltage and current waveforms of 7-level inverter: (a) proposed inverter output waveforms during normal mode operations for R-L load, (b) inverter output waveform under switch S1 fault condition, (c) load current and voltage waveform under switch S1 faulty resilient condition and (d) load current and voltage waveform under switch S1 and S5 fault resilient condition

The Figure 5(b) shows that, the proposed inverter output current and voltage waveforms operating with fault operation. The inverter is started with normal operation till reaches the 0.52 seconds. At time $T=0.52$ seconds, the switch S1 is failure to operate the seven level operation. It treated as faulty condition.

Once the switch failure occurs, the output voltage and current waveforms are distorted, so the source and load of connected to the faulty switch inverter may cause damage. To avoid this problem the redundant switching combinations are to be provided to make the system continuous. The resilient operation of the proposed inverter is shown in Figure 5(c) under single switch S4 failure condition. Once the switch failure occurs, in this operation at T=0.52 seconds on words the output voltage level are reduced to five and the same maximum magnitude is presented across the load.

Similarly, the proposed inverter operating under two switches failure condition also the continuous power must be delivered to load without any interruption by using redundant switches with reduced number of levels of output voltages as shown in Figure 5(d). But it is observed that the magnitude of voltage and current is also reduces. To avoid the source and load fluctuations under two switches failure operation, the magnitude of voltage always maintained as rated value by using a tapped transformer. With the transformer operation the output voltage and current waveforms as shown in Figure 6.

Table 4 shows that the comparison of proposed topology with recently proposed topologies of fault resilient tolerance ability. The comparison is analyzed based on number of switches, number of voltage sources, number capacitors, the number of bidirectional switches and turn on switches before and after fault operation. And finally, it reveals that the proposed topology achieves the better performance over the recently presented topologies.

Table 3. For the simulation required parameters

Parameter	Value
Input voltage	96 V-3 No's
Reference signal frequency	$f_m=50\text{ Hz}$
Switching or carrier signal frequency	2 KHz
Load resistance	$R=80\ \Omega$,
Load inductance	$L=50\text{ mH}$
Modulation index	0.98

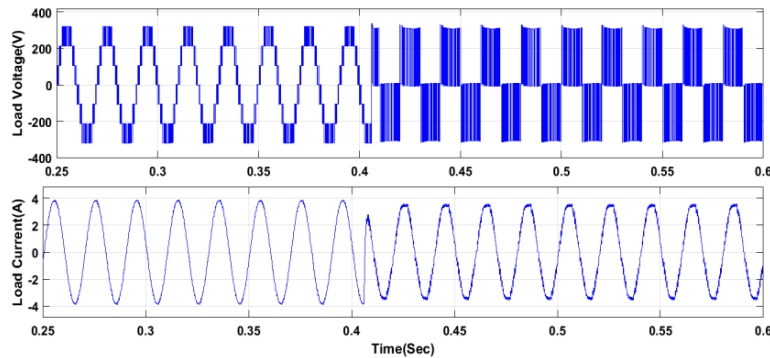


Figure 6. Load current and voltage waveform under switch S1 and S5 fault resilient condition with transformer

Table 4. Comparison of recent topologies with proposed

Reference paper number parameters	[12]	[18]	[26]	[14]	[16]	Proposed topology
Voltage sources	2	3	1	2	3	3
Capacitors	0	0	1	0	0	0
Bidirectional switches	1	18	3	0	11	3
Total number of switches	6	16	7	14	12	6
Total number of switches turned ON at instant of time before fault	3	12	3	4	8	3
Total number of switches turned ON at instant of time after fault	5	10	4	3	6	2
Single switch open circuit failure-resilient	√	√	√	√	√	√
Multiple switch open circuit failure-resilient	√	x	x	√	x	√

5. CONCLUSION

In this work, a novel configuration of a MLI with lower number of switch count is proposed and the reliability of the proposed MLI configuration is improved by analyzing the fault tolerance operation. From the performance analysis in the results, it was observed that, the proposed novel inverter configuration is having enough capability to tolerate open circuit faults not only for single switch and also for number of

switches. And it maintains the constant voltage pre and post fault operation with the help of transformer. And also, it is observed that with the help of multi carrier PDPWM switching control strategy the proposed multi-level inverter improved efficiency has enhanced. From this analysis, it is found that it can be applicable for grid connected and adjustable speed drive applications.

APPENDIX

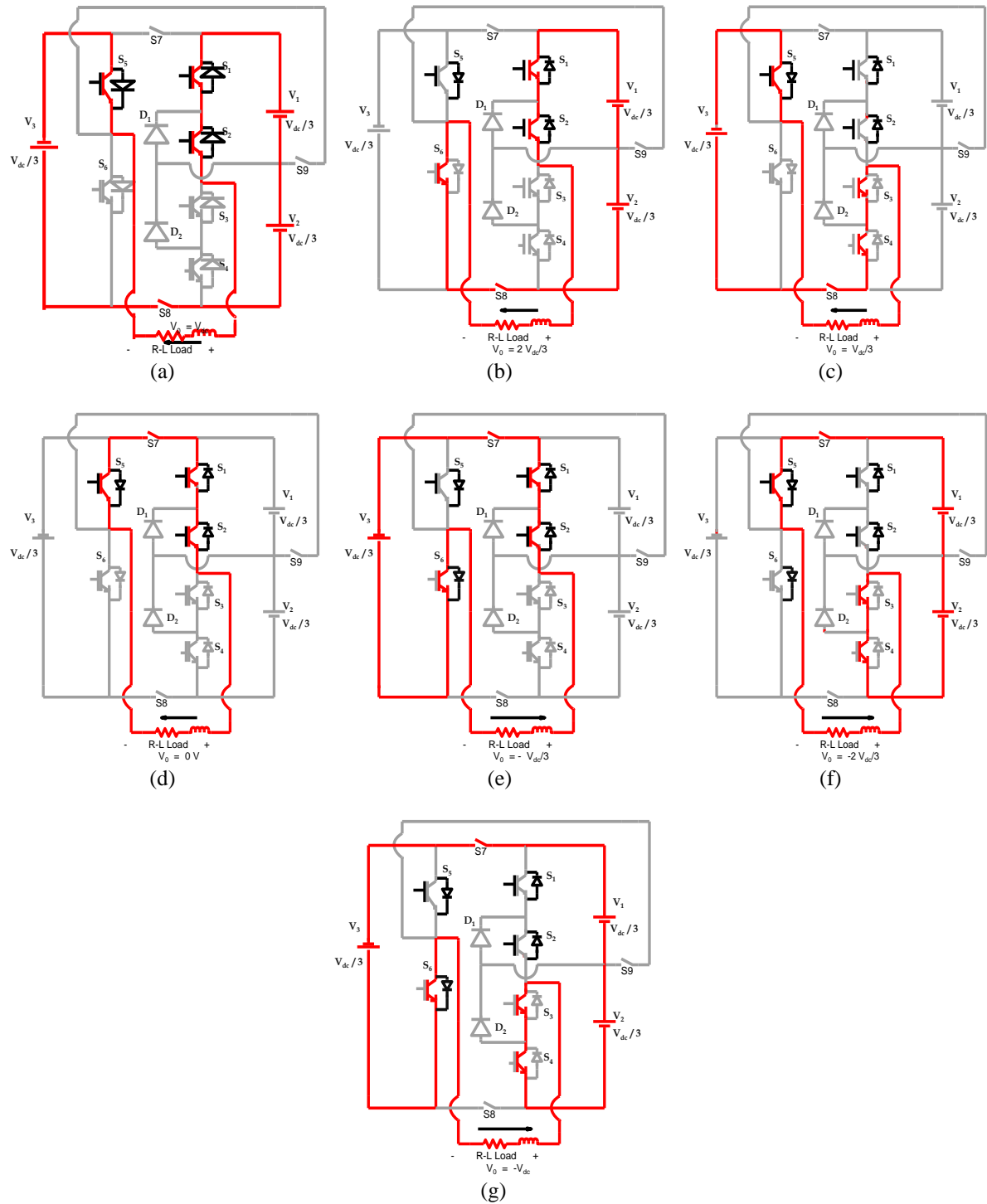


Figure 2. Current direction and working state of each voltage level during normal operation, (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, (e) Mode 5, (f) Mode 6, and (g) Mode 7

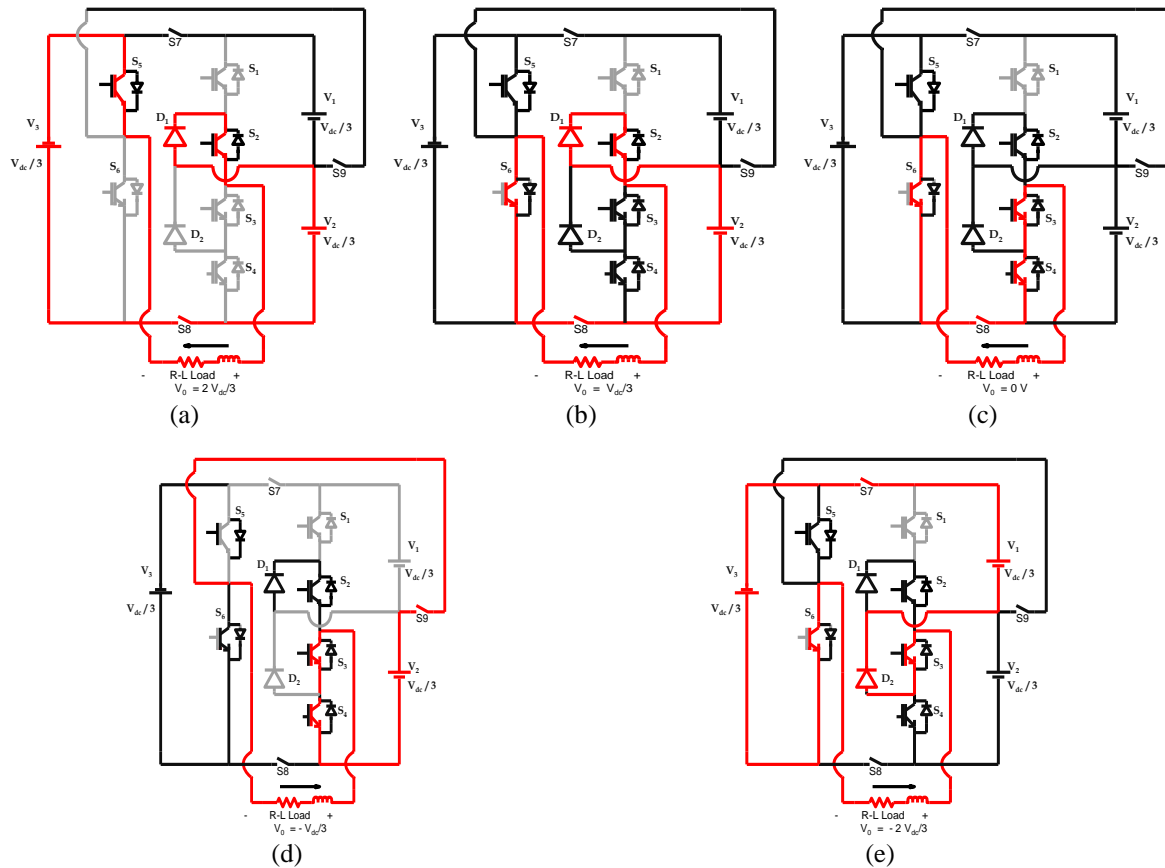


Figure 3. Current direction and working state of each voltage level under fault operation: (a) represents positive higher voltage level, (b) denotes the positive middle voltage level, (c) shows the zero voltage level, (d) represents the negative middle voltage level, and (e) denote the negative higher voltage level during single switch failure




REFERENCES

- [1] S. Ould Amrouche, D. Rekioua, T. Rekioua, and S. Bacha, "Overview of energy storage in renewable energy systems," *International Journal of Hydrogen Energy*, vol. 41, no. 45, pp. 20914–20927, Dec. 2016, doi: 10.1016/j.ijhydene.2016.06.243.
- [2] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality ac–dc converters," *IEEE Transactions on Industrial Electronics*, vol. 50, no. 5, pp. 962–981, Oct. 2003, doi: 10.1109/TIE.2003.817609.
- [3] A. Bughneda, M. Salem, A. Richelli, D. Ishak, and S. Alatai, "Review of multilevel inverters for PV energy system applications," *Energies*, vol. 14, no. 6, Mar. 2021, Art. no. 1585, doi: 10.3390/en14061585.
- [4] A. Sinha, K. Chandra Jana, and M. Kumar Das, "An inclusive review on different multi-level inverter topologies, their modulation and control strategies for a grid connected photo-voltaic system," *Solar Energy*, vol. 170, pp. 633–657, Aug. 2018, doi: 10.1016/j.solener.2018.06.001.
- [5] L. Franquelo, J. Rodriguez, J. Leon, S. Kouro, R. Portillo, and M. Prats, "The age of multilevel converters arrives," *IEEE Industrial Electronics Magazine*, vol. 2, no. 2, pp. 28–39, Jun. 2008, doi: 10.1109/MIE.2008.923519.
- [6] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 858–867, Aug. 2002, doi: 10.1109/TIE.2002.801073.
- [7] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Transactions on Industry Applications*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981, doi: 10.1109/TIA.1981.4503992.
- [8] M. F. Escalante, J.-C. Vannier, and A. Arzande, "Flying capacitor multilevel inverters and DTC motor drive applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 809–815, Aug. 2002, doi: 10.1109/TIE.2002.801231.
- [9] V. Anil Kumar and A. Mouttou, "Improved performance with fractional order control for asymmetrical cascaded H-bridge multilevel inverter," *Bulletin of Electrical Engineering and Informatics (BEEI)*, vol. 9, no. 4, pp. 1335–1344, Aug. 2020, doi: 10.11591/eei.v9i4.1885.
- [10] A. M. Rao, N. K. Kumar, and K. Sivakumar, "A multi-level inverter configuration for 4n pole induction motor drive by using conventional two-level inverters," in *2015 IEEE International Conference on Industrial Technology (ICIT)*, Mar. 2015, pp. 592–597, doi: 10.1109/ICIT.2015.7125163.
- [11] M. A. Hutabarat, S. Hasan, A. H. Rambe, and S. Suherman, "Design and simulation hybrid filter for 17 level multilevel inverter," *Bulletin of Electrical Engineering and Informatics (BEEI)*, vol. 9, no. 3, pp. 886–897, Jun. 2020, doi: 10.11591/eei.v9i3.890.
- [12] M. R. A and K. Sivakumar, "A fault-tolerant single-phase five-level inverter for grid-independent PV systems," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 12, pp. 7569–7577, Dec. 2015, doi: 10.1109/TIE.2015.2455523.
- [13] P. C. D. Goud and R. Gupta, "Dual-mode control of multi-functional converter in solar PV system for small off-grid




- applications,” *IET Power Electronics*, vol. 12, no. 11, pp. 2851–2857, Sep. 2019, doi: 10.1049/iet-pel.2018.6313.
- [14] M. Aly, E. M. Ahmed, and M. Shoyama, “A new single-phase five-level inverter topology for single and multiple switches fault tolerance,” *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9198–9208, Nov. 2018, doi: 10.1109/TPEL.2018.2792146.
- [15] X. Kou, K. A. Corzine, and Y. L. Familiant, “A unique fault-tolerant design for flying capacitor multilevel inverter,” *IEEE Transactions on Power Electronics*, vol. 19, no. 4, pp. 979–987, Jul. 2004, doi: 10.1109/TPEL.2004.830037.
- [16] M. M. Haji-Esmaili, M. Naseri, H. Khoun-Jahan, and M. Abapour, “Fault-tolerant structure for cascaded H-bridge multilevel inverter and reliability evaluation,” *IET Power Electronics*, vol. 10, no. 1, pp. 59–70, Jan. 2017, doi: 10.1049/iet-pel.2015.1025.
- [17] M. R. Airineni and S. Keerthipati, “DC offset minimisation of three-phase multilevel inverter configuration under fault and DC link voltage unbalance conditions,” *IET Power Electronics*, vol. 11, no. 2, pp. 293–301, Feb. 2018, doi: 10.1049/iet-pel.2017.0128.
- [18] H. K. Jahan, F. Panahandeh, M. Abapour, and S. Tohidi, “Reconfigurable multilevel inverter with fault-tolerant ability,” *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 7880–7893, Sep. 2018, doi: 10.1109/TPEL.2017.2773611.
- [19] U.-M. Choi, F. Blaabjerg, and K.-B. Lee, “Reliability improvement of a T-Type three-level inverter with fault-tolerant control strategy,” *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2660–2673, May 2015, doi: 10.1109/TPEL.2014.2325891.
- [20] N. Devarajan and A. Reena, “Reduction of switches and DC sources in cascaded multilevel inverter,” *Bulletin of Electrical Engineering and Informatics (BEEI)*, vol. 4, no. 3, pp. 186–195, Sep. 2015, doi: 10.11591/eei.v4i3.501.
- [21] E. H. Aboadla *et al.*, “A novel optimization harmonic elimination technique for cascaded multilevel inverter,” *Bulletin of Electrical Engineering and Informatics (BEEI)*, vol. 8, no. 2, pp. 405–413, Jun. 2019, doi: 10.11591/eei.v8i2.1500.
- [22] Madhukar Rao A, M. Sahoo, and Sivakumar K, “A three phase five-level inverter with fault tolerant and energy balancing capability for photovoltaic applications,” in *2016 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Dec. 2016, pp. 1–5, doi: 10.1109/PEDES.2016.7914527.
- [23] A. Chappa, S. Gupta, L. K. Sahu, and K. K. Gupta, “A fault-tolerant multilevel inverter topology with preserved output power and voltage levels under pre- and postfault operation,” *IEEE Transactions on Industrial Electronics*, vol. 68, no. 7, pp. 5756–5764, Jul. 2021, doi: 10.1109/TIE.2020.2994880.
- [24] N. K. Dewangan, T. Prakash, J. K. Tandekar, and K. K. Gupta, “Open-circuit fault-tolerance in multilevel inverters with reduced component count,” *Electrical Engineering*, vol. 102, no. 1, pp. 409–419, Mar. 2020, doi: 10.1007/s00202-019-00884-9.
- [25] M. R. Airineni, P. R. Bhimoreddy, M. Sahoo, and S. Keerthipati, “A multi-string fault-tolerant multilevel inverter configuration for off-grid photovoltaic applications,” *International Transactions on Electrical Energy Systems*, vol. 31, no. 3, Mar. 2021, doi: 10.1002/2050-7038.12803.
- [26] S. P. Gautam, L. Kumar, S. Gupta, and N. Agrawal, “A single-phase five-level inverter topology with switch fault-tolerance capabilities,” *IEEE Transactions on Industrial Electronics*, vol. 64, no. 3, pp. 2004–2014, Mar. 2017, doi: 10.1109/TIE.2016.2626368.

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