International Journal of Electrical and Computer Engineering (IJECE)
Vol. 12, No. 2, April 2022, pp. 1211~1222
ISSN: 2088-8708, DOI: 10.11591/ijece.v12i2.pp1211-1222

Integrated energy management converter based on maximum power point tracking for photovoltaic solar system

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Article Info

Article history:

Received Mar 25, 2021
Revised Nov 12, 2021
Accepted Nov 23, 2021

Keywords:

CMOS technology
DC-DC boost power converter
Integrated MPPT
Ripple correlation control algorithm
Solar energy

ABSTRACT

This paper presents an integrated power control system for photovoltaic systems based on maximum power point tracking (MPPT). The architecture presented in this paper is designed to extract more power from photovoltaic panels under different partial obscuring conditions. To control the MPPT block, the integrated system used the ripple correlation control algorithm (RCC), as well as a high-efficiency synchronous direct current (DC-DC) boost power converter. Using 180 nm complementary metal-oxide-semiconductor (CMOS) technology, the proposed MPPT was designed, simulated, and layout in virtuoso cadence. The system is attached to a two-cell in series that generates a 5.2 V average output voltage, 656.6 mA average output current, and power efficiency of 95%. The final design occupies only 1.68 mm^2.

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1. INTRODUCTION

Today, renewable energy such as solar power, wind power, and others, are being progressively employed in many applications of the industrial and civil field [1]–[4]. To provide maximum output power from photovoltaic (PV) panels under all conditions generates a major challenge due to variations of the output power of PV panels with temperature and solar irradiance level. To overcome this difficulty, maximum power point tracking (MPPT) controllers are employed to assure the highest efficiency levels of the PV panels. Many techniques are being developed and applied like perturb and observe (P&O) algorithm [5]–[8], incremental conductance (IncCond) algorithm [9]–[12], open-circuit voltage (VOC) based technique, and short-circuit (Isc) current based technique [13], [14]. Nevertheless, with multiple output power peaks, these methods struggle to detect the highest power point that arises from partial obscuring conditions [15]–[19]. Another technique known as distributed maximum power point tracking (DMPPT) has been introduced to enhance MPPT performance in larger solar power plants. They function to extract more energy while the solar panels in the system are not exposed to consistent operation circumstances [16]–[21]. Figure 1 depicts a traditional MPPT design that incorporates array-level shared MPPT. As the MPPT placement step progresses through the cell level, the DMPPT method reduces the partial shading impact [16], [17]. The addition of each solar cell receives a power converter and a controller circuit. Raises the cost, size, and power consumption.

In a cell-level dedicated MPPT design, this paper describes a ripple correlation control (RCC)-based integrated MPPT controller with a power stage that monitors the maximum power point of a single solar cell.

The RCC algorithm generates a quick, parameter-insensitive PV system MPPT. RCC is an effective MPPT method for tracking a PV array's MPP under varying solar irradiation conditions. This technique has many benefits, including the fact that no artificial perturbations are needed. Instead, it makes use of the switching power converter's underlying voltage or current ripples, and it makes no measurements or representations of the PV array since it is possible to integrate it using digital microcontrollers. Lastly, the RCC is a well-known algorithm capable of achieving maximum power point tracking at a rapid pace in constantly changing environmental and solar illumination conditions. Under different loads and varied irradiation levels, the system design and application specifications are investigated.

The structure of this paper is given as follows: the architecture configuration is presented in section 2. Description of the proposed circuit design of the integrated power management with MPPT in section 3. Simulations results and Layout of the proposed circuit design described in section 4, conclusion in section 5.

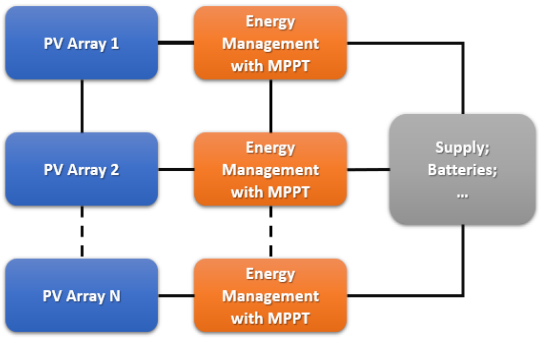
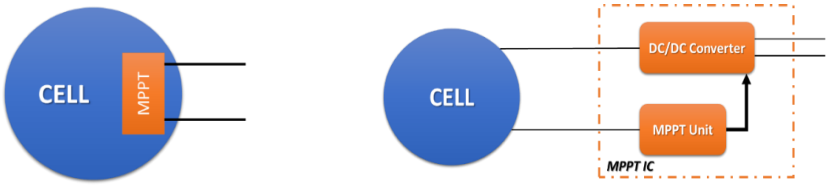


Figure 1. Design of a classic PV system with display-level MPPT design

2. ARCHITECTURE CONFIGURATION

Every PV cell's output is related to an integrated MPPT, as shown in Figure 2 [16]–[18], [22], [23]. Figure 2(a) displays the design of a single cell connected to an embedded MPPT. As shown in Figure 2(b), the MPPT block contains an embedded direct current (DC-DC) synchronous boost power converter and the MPPT controller, producing an MPPT embedded unit at the cell level. The integrated module's output is increased by using a DC-DC synchronous boost power converter. To draw out the MPPT in the integrated model we applied the ripple correlation control (RCC) algorithm [24].



(a) (b)

Figure 2. Design of PV cell: (a) a single cell is connected to an integrated MPPT design and (b) schematic of a single PV solar cell connected to MPPT IC

System ripples have the most impact on the RCC MPPT algorithm [24]. Figure 3 depicts the ripple correlation control method. The RCC technique works by continuously measuring the solar cell's voltage and current. The steepness of the transition in cell current and voltage is designed to extract the difference in cell energy as the power system begins voltage and current ripples. If the signs of power derivative (dP) and voltage derivative (dV) are same, the power converter's duty cycle (boost) must be increased, which is referred to as region-1. If the signs are flipped, the duty cycle of the power converter (boost) should be lowered, which is referred to as region-2. By regulating the service cycles of the boost converter, the photovoltaic cells set point is pushed toward its MPPT.

Based on an analysis of Figure 4, when I_L is less than I_L^*, a current ripple applied along with the curve results in an in-phase power ripple, implying that the sum of $i_L(di_L/dt)$ time derivative and $p(dp/dt)$

time derivative is positive. When I_L is greater than I_L^*, the current and power ripples are out of phase, resulting in a negative product of di_L/dt and dp/dt. These results can be integrated in (1):

$$\frac{di_L}{dt}\frac{dp}{dt} > 0 \Rightarrow I_L < I_L^* ; \frac{di_L}{dt}\frac{dp}{dt} < 0 \Rightarrow I_L > I_L^* \quad (1)$$

which will lead to one form of the RCC law. If I_L rises when the product of (1) is higher than 0 and drops otherwise, then I_L can approach I_L^*. One method to do this is to integrate the product that express in (2).

$$d = k \int \frac{di_L}{dt}\frac{dp}{dt} dt \quad (2)$$

Where d is the duty cylcle on the switch and k is a positive gain constant. If the duty cycle increases and decreases, the inductor current increases and decreases, so changing d can have the right movement of I_L.

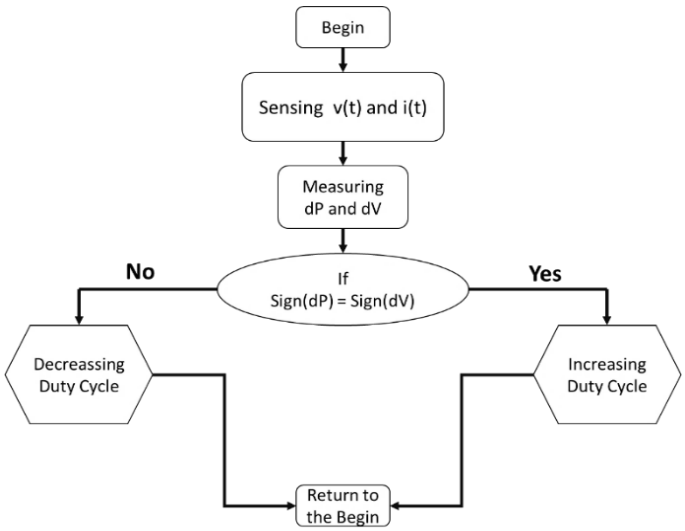


Figure 3. The RCC MPPT algorithm flowchart [24]

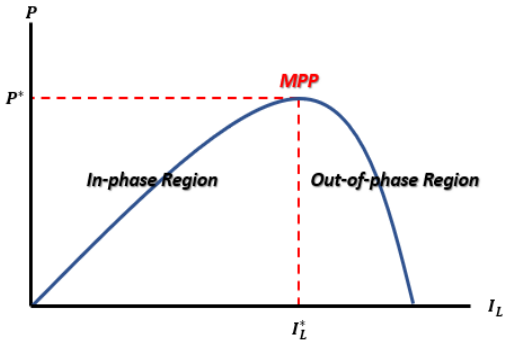


Figure 4. Average power of a PV array vs average inductor current

To operate around the maximum power point, apply the RCC MPPT control circuit to the synchronous boost converter circuit [25]. As seen in Figure 5, the transistor MN1 is used as a synchronous transition to improve device operation. Figure 6 illustrates the RCC MPPT control circuit's block diagram. A current sensor circuit senses inductor current and provides a voltage signal proportional to the amount of current detected. The output voltage of the cell is calculated by multiplying the cell voltage by the voltage signal.

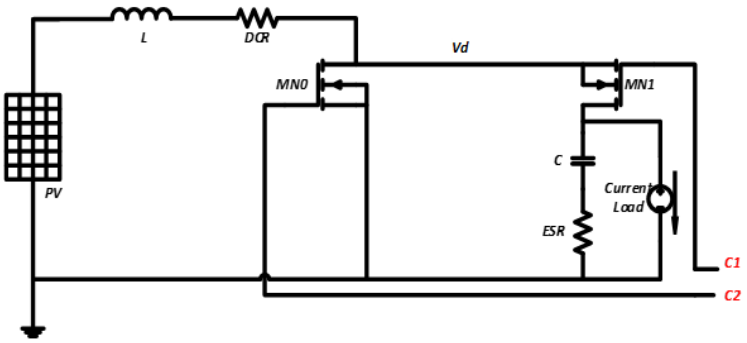


Figure 5. Schematic of synchronous DC-DC boost power converter

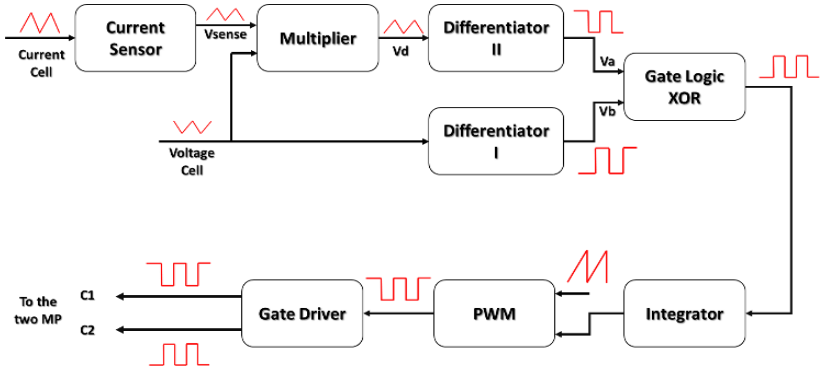


Figure 6. The RCC Maximum power point circuit design's block diagram

3. CIRCUIT DESIGN OF THE INTEGRATED POWER MANAGEMENT WITH MPPT

As illustrated in Figure 7, the power signal and the voltage signal are connected to two differentiators to determine the operation region on the PV curve, a XOR circuit is used to compare the output of the two differentiators. When the outputs of the two differentiators are in sync, the system enters zone 2 and the XOR generates a value 0, which is connected to an integrator circuit. The pulse width modulator (PWM) will generate a duty cycle which is supplied to the switches over the gate driver block. However, in region 1 the duty cycle is decreasing while the maximum power point is achieved.

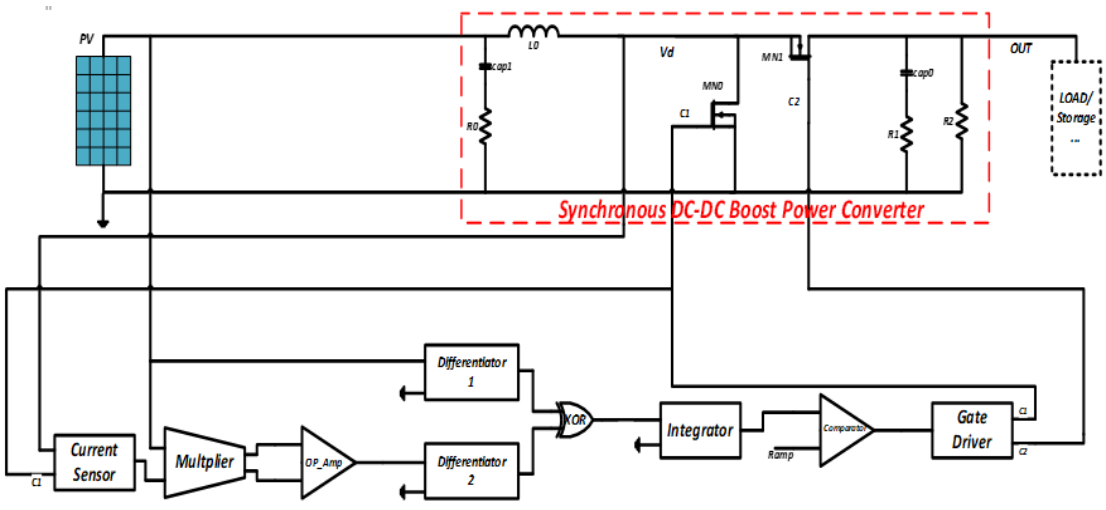


Figure 7. Schematic of the proposed RCC MPPT circuit

3.1. Synchronous DC-DC boost power converter

Figure 7 illustrates in detail the proposed analog circuit for the analog MPPT interface. As previously said, size and cost are major requirements in cell-level PV MPPT configuration. The DC-DC block is implemented on the same chip as the MPPT block to take advantage of the solar cell's slightly lower voltage. In this article, the designed synchronous DC-DC is enhanced for 0.5 V input, which corresponds to the entire open-circuit voltage of the cell, 1.2 A output current, and 500 KHz switching frequency. To limit condition losses, this architecture hires two NFets. In addition, select a low input capacitor value for RCC regulation depending on the required input voltage ripple. In addition, the input voltage is critical for RCC control to ensure high tracking reliability in low irradiation conditions for the highest power point.

3.2. Current sensor circuit

The circuit design of the current sensor is shown in Figure 8, in this architecture both transistor MN2 and MN3 are connected by their gates. The inductor current goes over MN2 when it is in the on-time function. The current that crosses MN3 and MN4 this circuit corresponds to the positive slew rate of the inductor current, also MN3 and MN4 are utilized to copy the positive slew rate of the spontaneous inductor current with an appropriate gain, which is determined by the number of field effect transistor's (FET) used for MN3. To have an equal drain voltage of MN4 and MN5 a voltage follower is used by connecting the gates of MN5 and MN7, as a result, the drain current of MN4 matches the drain current of MN5. The output voltage of the current sensor block (Vsense) is the voltage that crosses MP3 and MP4, this voltage is a copy of the voltage on the capacitor C1 while charging. During the off-time of MN2, MN3 is turned off. The capacitor C1 discharges within the internal resistor of MN4, also the current IBias defines the drain current of MN4. Furthermore, the negative slew rate of the inductor current is provided by the signal generated within the capacitor with the exact gain as the positive slew rate of the inductor current.

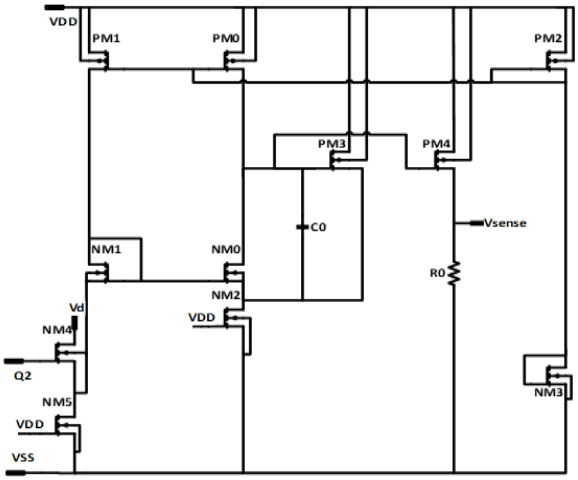


Figure 8. Current sensor circuit design

3.3. Analog multiplier circuit

The architecture of the multiplier used in this paper is based on reference [26] as illustrated in Figure 9. In the saturation zone, the incoming voltage is supplied to the gate and source of each transistor. The shunt-feedback buffer and active attenuator outputs are sent into the differential squaring circuit. Every transistor's drain current can be written as expressed in (3) to (6):

$$I_{D1} = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)\left[\left(\frac{V_x}{4}+a\right)-\left(\frac{V_y}{4}+b\right)-V_{Th}\right]^2 \quad (3)$$

$$I_{D2} = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)\left[\left(\frac{-V_x}{4}+a\right)-\left(\frac{V_y}{4}+b\right)-V_{Th}\right]^2 \quad (4)$$

$$I_{D3} = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)\left[\left(\frac{-V_x}{4}+a\right)-\left(\frac{-V_y}{4}+b\right)-V_{Th}\right]^2 \quad (5)$$

$$I_{D4} = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)\left[\left(\frac{V_x}{4}+a\right)-\left(\frac{-V_y}{4}+b\right)-V_{Th}\right]^2 \quad (6)$$

where, $a = \frac{|V_{Tp}|+V_{DD}}{2}$ and $b = \left(\frac{|V_{Tp}|+V_{DD}}{2}\right) - \sqrt{\frac{I}{K_N}} - V_{Th}$.

The multiplier circuit will create the cell current by multiplying the cell voltage signal with the output signal of the current sensor in order to obtain an output that reflects the cell's power. The differential output current is calculated using (3) to (6):

$$I_{out} = (I_{D1}+I_{D3}) - (I_{D2}+I_{D4}) = \frac{\mu C_{ox}}{8}\left(\frac{W}{L}\right)V_x * V_y \quad (7)$$

where, Vx (x=1 or 4) and Vy (y=2 or 3) are the input signals of the multiplier, W/L is the aspect ratio of transistors MN1, MN2, MN3 and MN4.

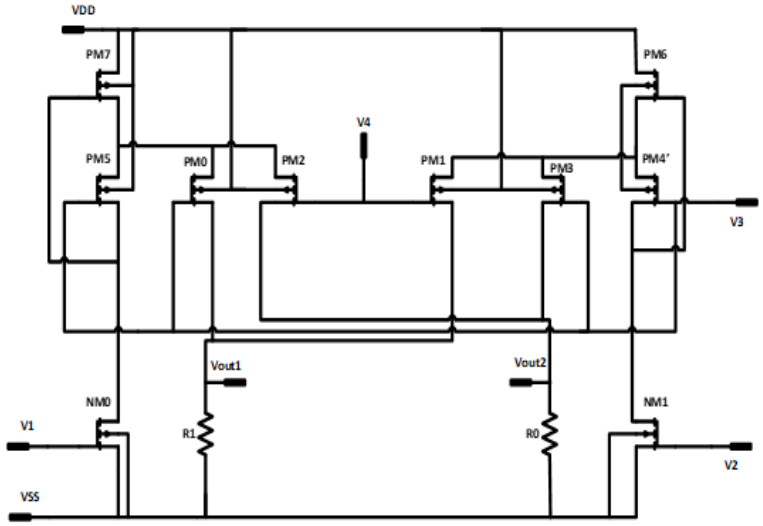


Figure 9. Analog multiplier circuit design

3.4. Differentiator circuit

The differentiator circuit used in this work, which will differentiate its input signal that increases or decreases, differentiator circuit is based on complementary metal-oxide-semiconductor (CMOS) operational amplifier as shown in Figure 10. To make sure that the differentiator function independently of A capacitor is also employed to block the DC component of the incoming signal, which is sent to the differentiator circuit, depending on the value of the input signal. The presented integrated MPPT circuit design includes two differentiators, the primary of which is used to differentiate the cell voltage and to display the cell power the secondary differentiator is used by differentiating the output signal coming from the multiplier circuit. The output signal is connected to the input signal; If the input is negative, the output is 0, and if the input is positive, the output is 1; both of these signals are sent into the XOR block.

3.5. Integrator circuit

An integrator circuit is attached to the XOR circuit output to turn the digital signal to an analog signal, which induces the required duty cycle of the DC-DC block in order to get the voltage level of the XOR output signal. The output of the integrator block is sent into the PWM circuit block, which uses a basic low filter circuit to control the switches with the generated control signal. If the XOR block output signal is 1, the output of the integrator circuit rises, as does the duty cycle; hence, duty cycle variance is proportional to the integrator circuit gain. Which may be determined using the (8).

$$G = 1/RC \quad (8)$$

3.6. Pulse width modulator circuit

The pulse width modulator (PWM) includes two components, the comparator circuit, and the sawtooth generator circuit. To command the switches of the power converter, the PWM design will generate a pulse width signal by comparing the output signal produced by the integrator circuit with the generated sawtooth signal.

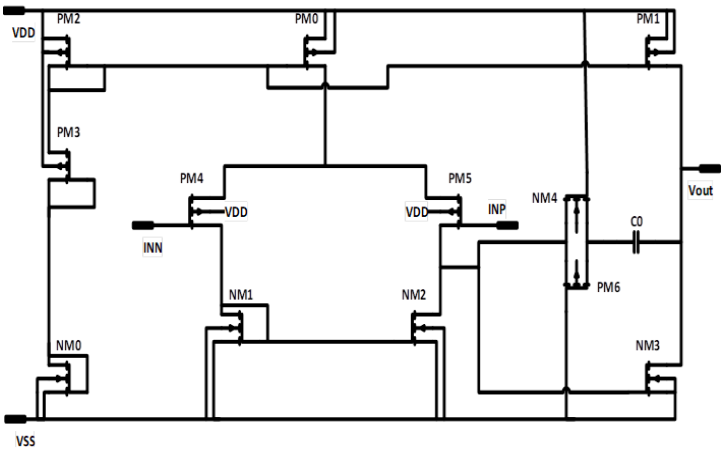


Figure 10. Circuit of the operational amplifier used in differentiator

3.7. Gate driver circuit

To make sure that the power transistors will not be switch on simultaneously, a gate driver circuit is used, and it's connected to the PWM circuit output. Figure 11 display the circuit design of the gate driver [27]. The output of the integrator block is the signal generated by comparing the signal of the sawtooth generator with a DC voltage.

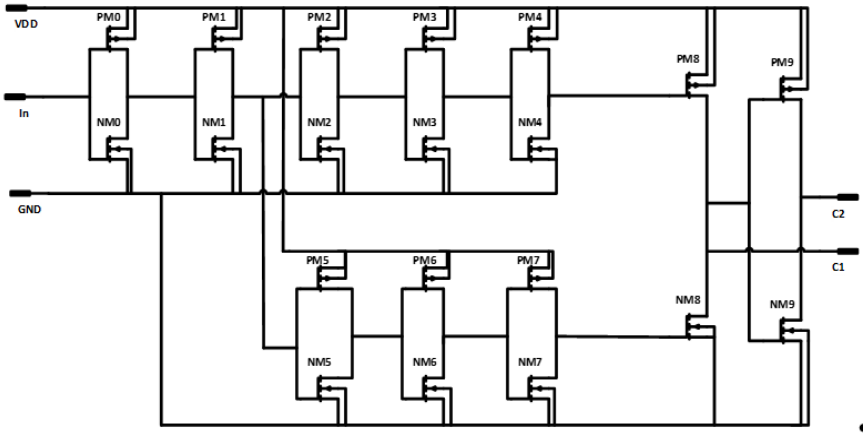


Figure 11. Gate driver circuit design

4. SIMULATION RESULTS AND LAYOUT

The proposed circuit design consists of an asynchronous DC-DC boost power converter block, besides the externally attached power inductor, and a controller circuit it carries out MPPT for a voltaic cell is used. The planned architecture has been developed and tested with CADENCE virtuoso in 180 nm CMOS technology. First, we going to display the simulation results of each block of the proposed architecture. As for the first block of the current sensor circuit, Figure 12 shows the simulation results of the current sensor, which illustrate the input and output of the current sensor circuit. Based on these results, the current sensor circuit provides a good response with Vsense varying from 0.65 V to 1.2 V while maintaining the same waveform of the input signal produced by the solar cell.

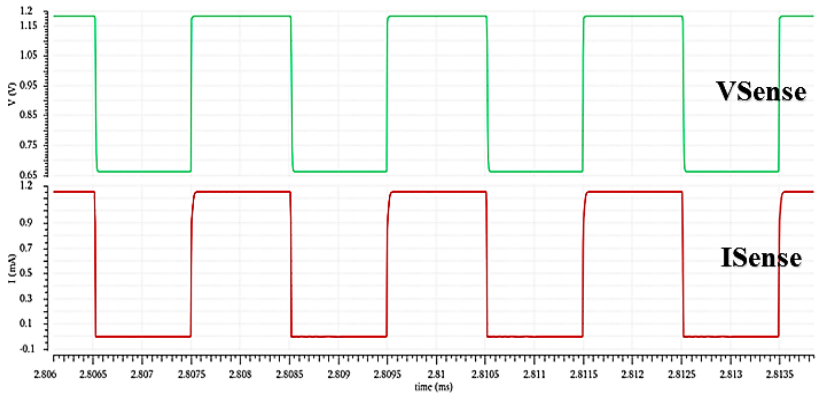


Figure 12. Simulation results of the input and output of the current sensor circuit

Figure 13 depicts the analog multiplier simulation results, which shows the input V1 produced by the PV cell and the second input V2 generated by the current sensor circuit, with Vout being the product of V1 and V2. The output signal of the analog multiplier circuit shows the circuit's strong functionality. Figure 14 represents the simulation results of a PWM circuit that compares the signal from the integrator circuit with the Ramp signal, resulting in a PWM circuit output (Vout) that varies from 0.1 V to 1.8 V. The simulation results of the gate driver circuit are shown in Figure 15, which displays the waveforms of the two outputs (C1) and (C2) with the input signal coming from the PWM circuit. The simulation results demonstrate clearly that the gate driver circuit controls the two power metal oxide semiconductor's (MOS) by switching them separately.

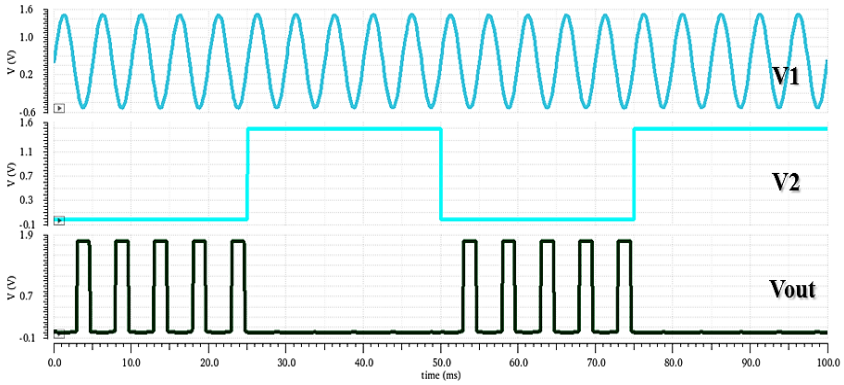


Figure 13. Simulation results of the two inputs and output of the analog multiplier circuit

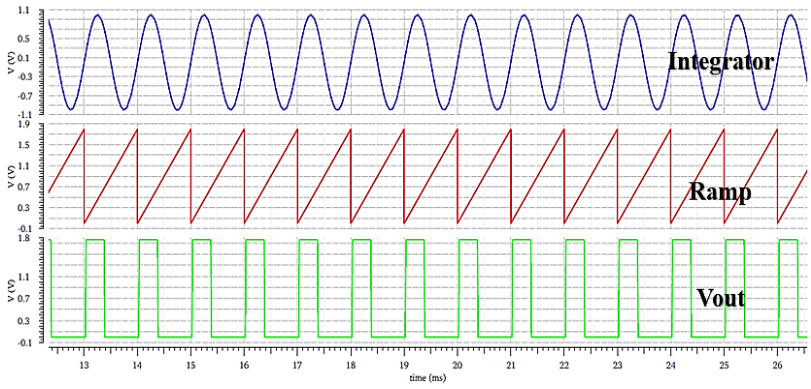


Figure 14. Simulation results of PWM circuit

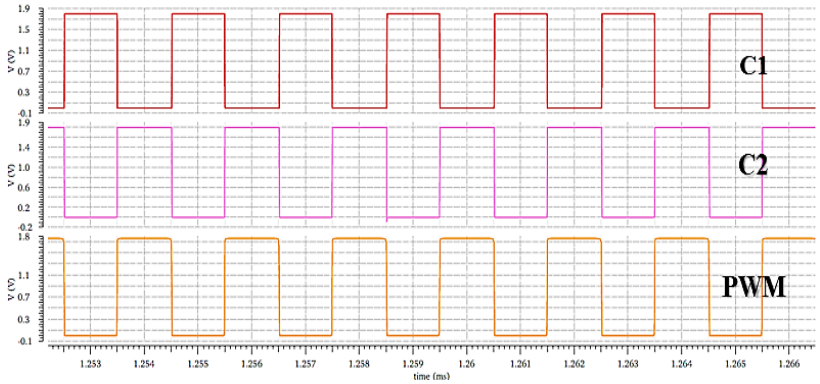


Figure 15. Simulation results of gate driver circuit

The PV cell used in this work is modeled and simulated in the second part of the simulation, as defined in [15], [20]. Photovoltaic models are intended to function in a certain range of power, voltage, and current to provide a graph that is similar to the actual MPP curve. The cell has a particular V-I curve with low voltage and high current that necessitates greater attention in modeling by combining various models. The PV model does not need to be implemented in hardware; the MPPT should function with a real cell. Figure 16 shows the P-V and V-I characteristic curves of the PV cell model used.

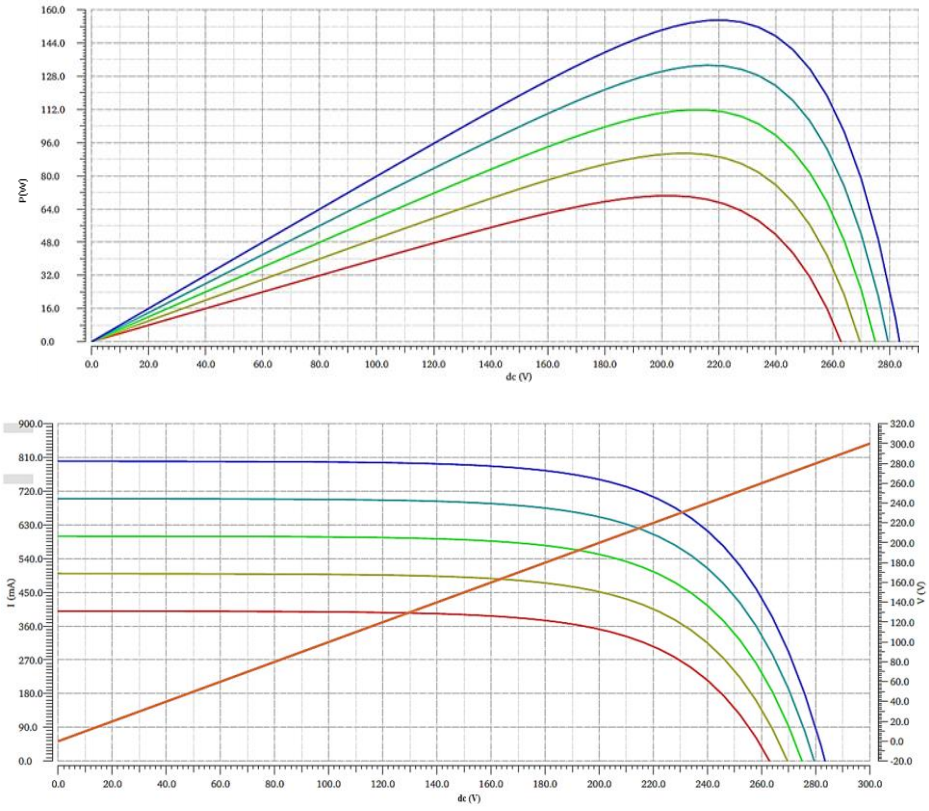


Figure 16. Power-voltage P-V characteristic curve; current-voltage I-V characteristic curve of the photovoltaic panel

The proposed architecture in this paper is tested under these parameters, 2 W PV cell with 0.5 V open circuit voltage and 6 A for short circuit current, which provides a 1.2 A for load current. To verify the designed maximum power point control circuit, the system has been tested for multiple irradiation levels. The suggested circuit's simulation results with different illumination levels 800, 600, 400 W/m², as shown in

Figure 17. After a transitory period, the system achieves a state of stability, the results are presented in the following Table 1.

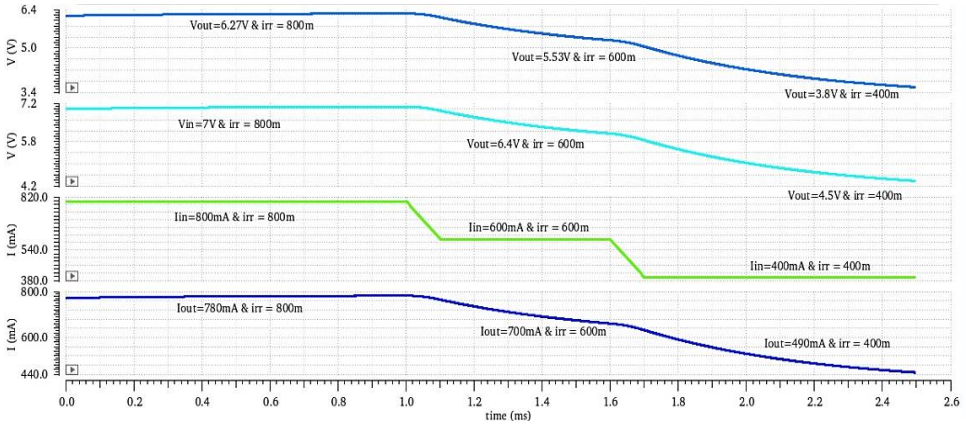


Figure 17. The boost converter circuit's cell input and output voltages under various irradiations

Table 1. Summary of the current and voltage for different irradiation levels of the proposed system

Irradiation levels (W/m²)	Cell voltage (V)	Cell current (mA)	Output voltage (V)	Output current (mA)
800	7	800	6.27	780
600	6.4	600	5.53	700
400	4.5	400	3.8	490

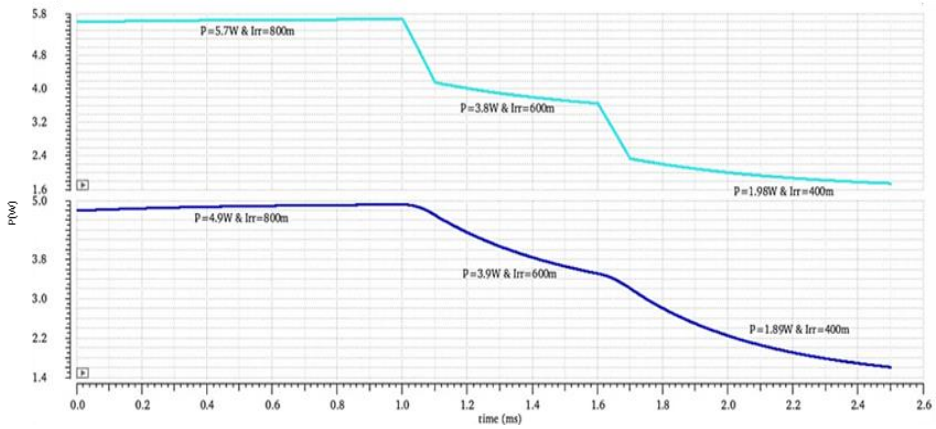


Figure 18. Input power and output power under different irradiations of the proposed circuit

The produced power decreases due to diminution of the cell voltage and output voltage caused by the decrease in the irradiation levels. The simulation results of the synchronous DC-DC converter for three different irradiation 800, 600, 400 W/m² are represented in Figure 18. The results prove that the proposed circuit in this paper track the maximum power point at every level, also it verifies the appropriate functioning of the integrator circuit, as Table 2 summarizes the value of the results of the input and output power for different irradiation levels. Figure 19 shows the efficiency of the system as a function of the output power with an input frequency of 1 kHz. The peak efficiency of the system is 95%.

Table 2. Summary of the input power and output power for different irradiation levels of the proposed system

Irradiation levels (W/m²)	Input power (W)	Output power (W)
800	5.7	4.9
600	3.8	3.9
400	1.98	1.89

Finally, Figure 20 display the layout of the proposed architecture of the integrated power management based on MPPT for the PV solar system. The two power MOS occupy the majority of the chip area, also the layout respects the design rules and the design constraint information. The surface area of the proposed architecture is 218.29x76.4 µm. A comparison between the proposed power management and other previous works is summarized in Table 3.

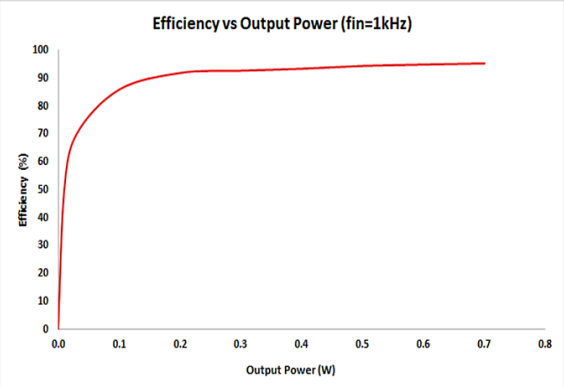


Figure 19. System efficiency versus output power with (fin=1 kHz)

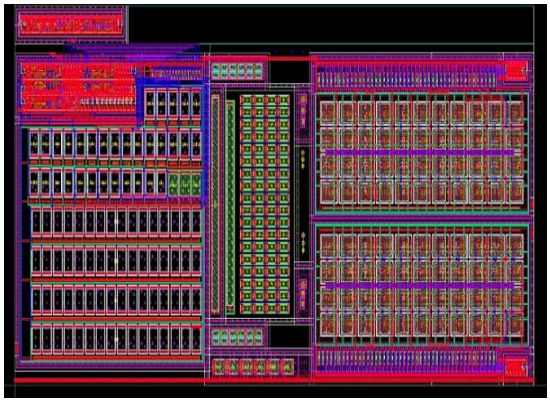


Figure 20. Layout of the proposed architecture

Table 3. Summary and comparison performance

References	[28]	[29]	[30]	This Work
Process CMOS	350 nm	180 nm	130 nm	180 nm
MPPT algorithm	RCC MPPT	RCC MPPT	DMPPT	RCC MPPT
Output power (W)	2	6 µ-1.4 m	45-160 m	1.89-4.9
Efficiency (%)	92.3	74.6	92	95
Chip area (mm²)	2.925	8	4.8	1.68

5. CONCLUSION

In conclusion, integrated power management based on a maximum power point circuit has been developed successfully on 180 nm CMOS technology. This study involves circuit design, simulation, analysis, and layout design. The proposed architecture gives independence to the PV cell to work at the maximum power point excluding any limitations, also fixing the problem of the partial effect by tracking the maximum power point of each cell. Moreover, the shadowed cell can generate a maximum power point of its own without influencing the lighted cell. The system is connected to a two-cell connected in series, generating 5.2 V average output voltage, 656.6 mA average output current, and power efficiency of 95%. The chip area is only 1.68 mm^2.

ACKNOWLEDGEMENTS

The National Center for Scientific and Technical Research (CNRST Morocco) funded this research under the PPR2 project.

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