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Operational transconductance amplifier-based comparator for high frequency applications using 22 nm FinFET technology

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ABSTRACT

Fin field-effect transistor (FinFET) based analog circuits are gaining importance over metal oxide semiconductor field effect transistor (MOSFET) based circuits with stability and high frequency operations. Comparator that forms the sub block of most of the analog circuits is designed using operational transconductance amplifier (OTA). The OTA is designed using new design procedures and the comparator circuit is designed integrating the sub circuits with OTA. The building blocks of the comparator design such as input level shifter, differential pair with cascode stage and class AB amplifier for output swing are designed and integrated. Folded cascode circuit is used in the feedback path to maintain the common mode input value to a constant, so that the differential pair amplifies the differential signal. The gain of the comparator is achieved to be greater than 100 dB, with phase margin of 65°, common mode rejection ratio (CMRR) of above 70 dB and output swing from rail to rail. The circuit provides unity gain bandwidth of 5 GHz and is suitable for high sampling rate data converter circuits.

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1. INTRODUCTION

Mixed signal circuit design is gaining importance in most of the system on chip (SOC) that is used in every electronic system operating at few GHz. Operational transconductance amplifier (OTA) is one of the primary building blocks of analog and mixed signal circuits that is used as sub system in every circuit design. Design of OTA requires estimating the W/L geometries of transistors to meet performances such as DC gain, unity-gain bandwidth (UGB), common mode rejection ratio (CMRR), slew rate (SR), input common-mode voltage (VICM) and power dissipation. Process variation and nonlinear behavior of metal oxide semiconductor field effect transistor (MOSFETs) have been a challenging task to be addressed by circuit design engineers. Devices such as multi-gate MOSFET, Fin field-effect transistor (FINFETs), ultra-thin body silicon on insulator are gaining prominence in replacing MOSFETs for all mixed signal circuit design [1]. FinFET is demonstrated to be more advantages than MOSFET with additional gate control input, attenuated drain induced barrier lowering (DIBL), improved sub threshold swing and immunity to short channel effects [2]. FinFET based analog circuits are designed and demonstrated to be advantageous over MOSFETs [3]. Two stage amplifiers are designed using FinFET and is observed to be having advantageous over MOSFET based op-amp [4]. FinFET has been recognized as a hopeful device as it enables additional gate length scaling due to its superior immunity to short channel effect by making the channel controlled by gate from more than one side [5].

OTA circuit design using FinFET with 32 nm silicon on insulator (SOI) model is presented in [6] demonstrating its performance metrics. Sohn *et al*. [7] have presented general guidelines for design of analog circuits based on FINFETs. Threshold voltage in FinFET imposes limitations in analog circuit design and to overcome these bulk driven (BD) floating gate (FG) method is presented by Khateb [8]. In order to reduce power dissipation and to increase output swing self-biasing technique is used in circuit design [9]. Low power analog circuits are designed considering DC shifting and BD differential technique with rail-to-rail OTA [10]. FinFET based OTA is designed for low power applications using three stage structure and the design using 32 nm model that is found to operate at maximum frequency of 20 MHz, UGB and gain of 64 dB with a 33° phase margins [11]. A class AB tunable transconductor featuring low quiescent power consumption and the circuit features good dynamic performance with low distortion is presented in [12].

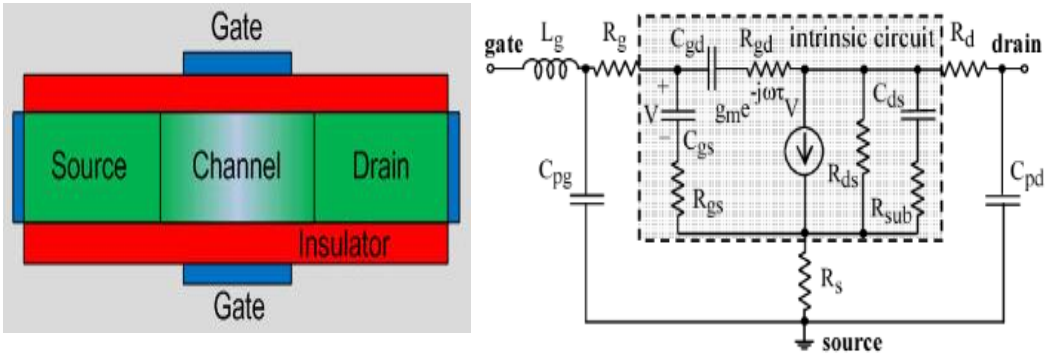
A pseudo-differential fully balanced, fully symmetric CMOS OTA architecture with inherent common mode detection is presented in [13]. An ultra-low power recycling folded cascode OTA which employs a power reduction technique that substantially reduces the power consumption while satisfying the gain and bandwidth requirements is presented in [14]. A simple rail-to-rail CMOS Miller OTA topology for ultra-low-voltage and ultra-low-power applications using DC shifting and BD differential pair configuration is presented in [15]. The concept of programmable FG-OTAs as well as building second order sections using these amplifiers is discussed in [16]. By combining the techniques pseudo differential pair and the bulk driven MOS transistors the OTA proposed for ultra-low voltage operation is presented in [17].

A new architecture for improvement of slew rate for an input signal with a rise time an OTA in FinFET technology is presented in [18]. One of the most commonly used low voltage output buffers was proposed by Monticelli [19]. A simple single stage OTA which is also known as five transistor OTA is presented in [20]. OTA based circuits are gaining importance in analog circuit applications such as filters, converters, and oscillators. The use of FinFET based OTA exhibits better performance in comparison to conventional CMOS based OTA is discussed in [21]. In this paper, comparator circuit which forms the sub system in every data converter circuit is designed using OTA from basic principles and is evaluated for its performances to operate at high frequencies. Section 2 discusses FinFETs and its fundamentals detailing device parameters and small signal model. Section 3 discusses OTA concepts, internal structure, design specifications and design of OTA. Section 4 discusses comparator design based on OTA. Section 5 discusses modeling of OTA and comparator. Results and discussion are presented in section 6 and conclusion is presented in section 7.

2. FinFET

Double gate FinFET device shown in Figure 1(a) and its characteristics demonstrating the increased current flow in the channel by controlling with two gate voltage is presented in [22]. Small signal model for the DG FET is presented in Figure 1(b). Cgd, Cgs and Cds are the parasitics in FinFET that limits the device operation at high frequencies and Rgd, Rgs, Rds and Rsub limits the device for low power operations.

Predictive technology model (PTM) parameters for FinFET presented in Table 1 and the corresponding model files are considered for design of OTA and OTA based comparator. Considering structural and electrical parameters of FinFET device modeling is carried out for analysis of input and output characteristics. The theoretical and practical mismatches are identified based on simulation results and the appropriate geometry settings for FinFET is identified for maximum frequency of operation and low power dissipation.



(a) (b)

Figure 1. FinFET, (a) FinFET device-structure of DGFET [22] and (b) small signal model [22]

Table 1. FinFET device parameters

Parameter	Value
Channel length	22 nm
Oxide thickness 1	2.5 nm
Oxide thickness 2	2.5 nm
Gate length	22 nm
Source/drain extension length	50 nm
Gate to source/drain overlap	2 nm
Work function	4.6 eV
Source/Drain doping	1×10^{19} cm^{-3}
Dielectric constant of channel	11.7
Dielectric constant of insulator	3.9
Band gap	1.12 eV
Affinity of channel material	4.05 eV
Mobility of electrons	1400 cm^2/Vs
Saturation velocity	1.07e + 07 cm/s

3. OTA DESIGN

The primary building blocks of OTA are presented in Figure 2. The input stage performs level shifting, second stage is the folded cascode stage with feedback and the last stage is the output stage. OTA connected in the unity gain configuration the operating signal swing is limited by the common-mode range of the input stage and the allowable output signal range. To allow maximum signal amplitudes, the rail-to-rail voltage ranges should extend from the positive supply to the negative supply levels. A simple class-AB amplifier is used as the output stage to an amplifier, allowing rail-to-rail output signal swing [23]. The simple OTA circuit is presented in Figure 3 that is realized using eleven transistors. The transistors F1 and F2 are the differential pair and forms the transconductance cell that converts the input voltage V+in and V–in (differential input voltages) to current. The differential current output (Iout) of the differential pair is converted to single ended current at the output by using the current mirrors F3 to F8, F10 and F11. F9 transistor is used to bias the differential pair and is used as current sink circuit. The cut-off frequency of the OTA is decided by setting the appropriate bias current and the load capacitance of the OTA. The transconductance gain gm of the OTA is controlled by setting the current that enters the transistor F9 and the gate voltage Vb is appropriately set. Design of OTA is primarily identifying the transistor geometries such that the simulation results are matching the hand calculations. A systematic procedure for the design of a single stage OTA using gm/ID methodology is discussed in [24]. Design methodology based on gm/ID method is the most popular approach that identifies the transistor geometries based on data sheets and simulation results. In this method of design of OTA circuits based on datasheet several design variables that were required for the design were assumed without clear rules. The design specifications meeting input range, common mode rejection and noise parameters were not considered in this approach. Even the channel length variations with regard to gm/ID were not considered in the design process. Considering the limitations of designing OTA circuit, a detailed approach that is based on gm/ID method is presented in this work with necessary modifications for design of simple OTA. The design approach presented in this work considers both design and optimization procedures considering small signal model of FinFET and device parameters. Table 2 presents the specifications considered for OTA design.

The maximum current that is available at the OTA bias is considered as 20 µA and the gain bandwidth product (GBW) is assumed to be approximately equal to closed loop bandwidth (BMCL) and the buffer input range is considered as common mode input range. Design of OTA is considered using step by step procedure. In step 1 the input pair is designed considering the input range assumed to be close to the ground rail between 0.15 to 1.05 V. With (1) the transconductance of the differential pair is determined [25]. The internal parasitics are considered for accurate calculation of gm.

$$GBW = \frac{g_{m1,2}}{2\pi C_L} \quad (1)$$

Substituting GBW and CL in (1) gm is approximated to 160 µS. Considering the OTA bias current of 20 µA which is split as the current flows through F1 and F2 is considered as 16 S/A(gm/ID1,2). The DC gain of the OTA considering differential signaling is given by (2),

$$A_{vdc} = \frac{g_{m1,2}}{(g_{ds_2} + g_{ds_4})} \quad (2)$$

Considering gm/ID1,2 and the A_{vdc} parameter (open loop DC gain is 32 dB) the requirements for maintaining output conductance is given as in (3).

$$g_{ds_2} + g_{ds_4} < 4\mu S \quad (3)$$

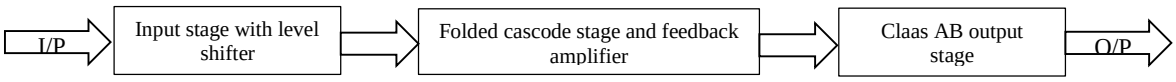


Figure 2. OTA block diagram

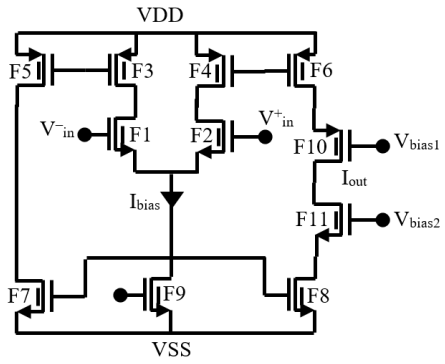


Figure 3. FinFET based OTA circuit [21]

Table 2. OTA design specifications

Parameters	Value
Technology	22 nm
Slew Rate=SR	>1 V/µS
Supply Voltage	1.2 V
Reference Current	10 µA
Load Capacitance	5 fF
Phase Margin	65°
Gain bandwidth	5 GHz
Open loop DC gain	32 dB
V_{out} range	±1.5 V
ICMR	0.15 to 1.05 V
CMRR	70 dB
Power Dissipation	≤10 µW

Assuming that transistor F2 and F4 are having similar output conductance gds2=gds4≤2 µS from which the intrinsic gain is (gm/gds) 1,2 is ≥80. Considering (3) gds2 and gds4 is assumed to be less than or equal to 2 µs. From the data sheet curves shown in Figure 4, the minimum intrinsic gain is constrained to 80. From the results that relate intrinsic gain of the amplifier with the gm/I_D (taken from datasheet) as shown in Figure 4, the transistor length is a trade-off between the gain and operating speed. For optimum design, the length of F1 and F2 is set to 22 nm resulting in gm/gds approximately equal to 90 satisfying the requirement. Considering the data sheet that gives relation between I_D/W vs gm/I_D as shown in Figure 5, the width of the transistors is computed as in (4).

$$W_{1,2} = \frac{I_D}{I_D/W} \approx 660\ nm \quad (4)$$

Design of n channel FinFET based current mirror circuit (transistors F3 and F4) is considered by considering the output conductance of the circuit that satisfies (5).

$$g_{d.s3,4} \leq 2\ \mu S \quad (5)$$

From the data sheet relations presented in Figure 4 the channel length that satisfies the gm requirements are identified as L3,4=16 nm. The minimum input voltage that can be considered that can drive the input pair beyond saturation is given as in (6).

$$V_{in,min} = 0.2V \geq -\left|V_{GSI,2}\right| + \left|V_{dsat1,2}\right| + V_{GS3,4} \quad (6)$$

The parameter V_{dsat} is the drain to source voltage that will keep the device in saturation. The parameter $V_{GS1,2}$ and $V_{dsat1,2}$ is identified from the model file of p channel FinFET and is approximated to be of 550 mV and 90 mV, respectively. Substituting in (6), $V_{GS3,4}$ is computed to be 0.61 V. The width of transistors F3 and F4 are identified from the current mirror datasheet as shown in Figure 4. Width of F3 and F4 are identified as 55 nm. Determination of tail current of p channel FinFET requires consideration of CMRR parameter and is given by (7), and choosing the appropriate length from Figure 4 L5,6=33 nm.

$$CMRR(dB) = A_{vdc}(dB) - A_{vdc,CM}(dB) \quad (7)$$

To limit the tail current in saturation the maximum allowable input voltage is given by (8).

$$V_{in,max} = 1.1V < V_{DD} - |V_{GSI,2}| - |V_{dsat\ 5,6}| \quad (8)$$

Considering p channel current density chart in Figure 5, the transistor widths W5=1430 nm and W6=715 nm. Figure 6 presents the circuit schematic of OTA with input stage, differential pair and output stage including the bias circuits. Based on the discussion presented in this section the final design of OTA is computed from fundamental principles and the transistor geometries are presented in Table 3.

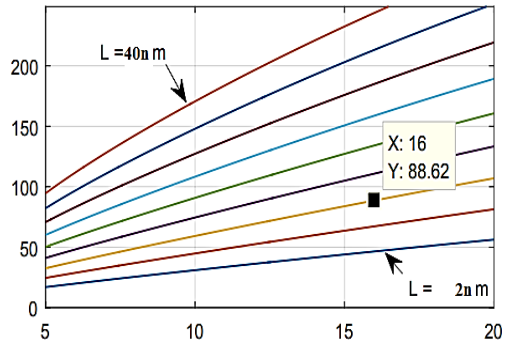


Figure 4. Gain vs g_m/I_D relation from datasheet [24]

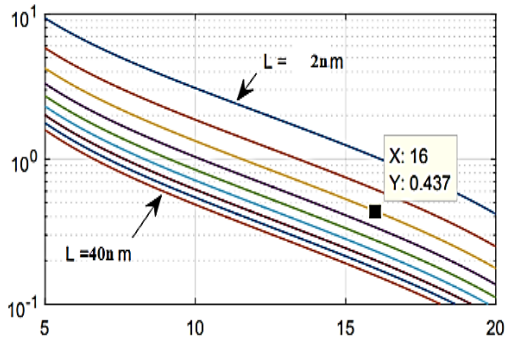


Figure 5. I_D/W vs g_m/I_D relation from datasheet [24]

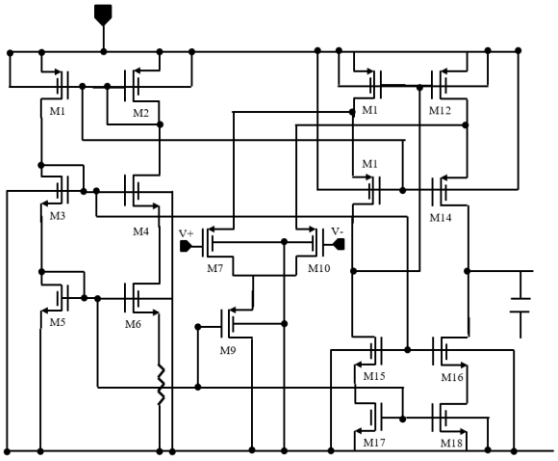


Figure 6. Schematic of folded cascode OTA by virtuoso schematic editor

Table 3. FinFET based OTA device geometries and circuit parameters

Transistor	W/L(nm/nm)	I_{ds} uA	V_{GS} (mV)
FN0	44.3/22.16(f:10/m:1)	2.7	490
FN1	660/22.16(f:10/m:1)	2.7	490
FN2	660/22.16	5.4331	553.
FP8	44.32/22.16	–5.4331	–741.662
FP7	44.32/22.16	–5.432	–741.662
FN13	44.32/22.16	5.433	553.745
FN14	44.32/22.16	5.4387	553.944
FN11	44.32/22.16	5.4387	553.745
FN12	44.32/22.16(f:1/m:4)	5.4387	485.762
FP3	55/22.16(f:6/m:1)	–8.1138	–881.306
FP4	55/22.16(f:6/m:1)	–8.1138	–881.306
FP6	1430/22.16(f:10/m:5)	–5.4113	–518.656
FP5	715/22.16(f:10/m:5)	–5.4113	–518.655
FN7	4.32/22.16	5.4113	669.962
FN4	55/22.16	5.4113	669.962
FN8	55/22.16	5.4113	553.745
FN9	55/22.16	5.4113	553.745
FP9	30.2/22.16(f:7/m:1)	–71.56	-881.306
FN16	60/22.16	71.58	918.694
R_1	12.5 Ohms	C_1	2 pF

4. OTA BASED COMPARATOR

For an OTA to function as a comparator, it has to be operated in the non-linear region of its characteristic. The OTA will basically act as a comparator with current output. The circuit for OTA-based comparator is shown in Figure 7(a). For the proper operation, the output current (or voltage across load) should be constant value $I(_1)$ or $V(_1)$ for Vi>VR and another constant value $I(_0)$ or $V(_0)$ for $V_i<V_R$. The transfer characteristic is shown in Figure 7(b). The special features of an OTA-based comparator are that the voltages V_0 and V_1 may be varied simply by varying the bias current I_B or the voltage V_B. Because I_0 is directly proportional to I_B, the change in I_B causes the OTA to saturate at different levels of voltages. Thus, different levels of output voltages may be obtained through bias current control.

A comparator is a circuit, which compares input signal V_i with a reference voltage VR. Usually, the reference voltage VR is applied to non-inverting terminal with a proper load and buffer connected at the output, the OTA behaves like a differential voltage current voltage source. With the buffered OTA, the output voltage will switch from a positive V_1 level to a negative V_0 level, as the inverting signal is less than or greater than

the reference level. The design specifications for the comparator based on OTA is presented in Table 4. The differential pair of the comparator is shown in Figure 8. It is an N-channel FinFET differential amplifier whose tail current is supplied through a current mirror.

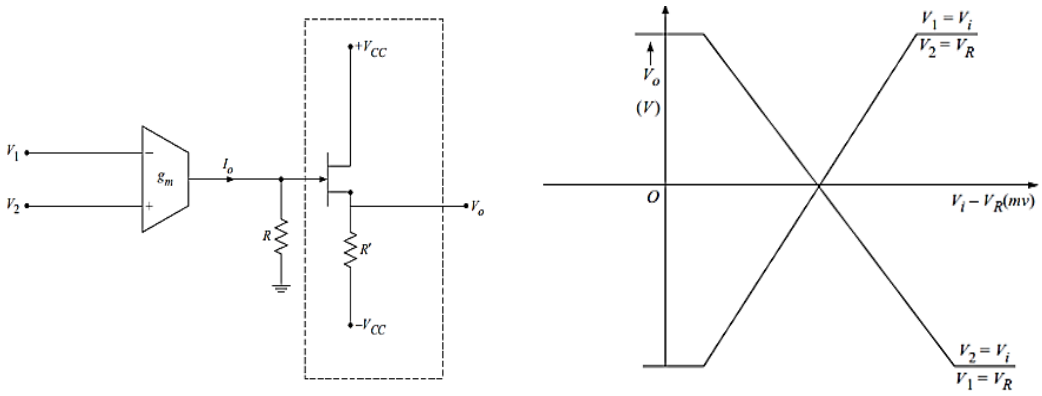


Figure 7. Comparator, (a) comparator circuit using OTA and (b) transfer characteristics

Table 4. Comparator specifications

Sl. No	Parameter	Value
1	DC open loop gain	103 dB
2	Phase margin	63°
3	Offset voltage	900 mV
4	CMRR	76 dB
5	Unity gain bandwidth	5 GHz
6	Voltage swing	0 to 1.8 V
7	Transconductance	0.4% to 0.8%

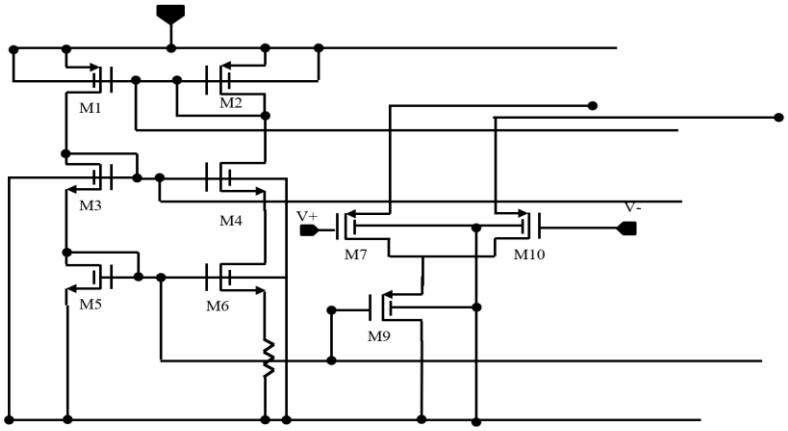


Figure 8. Differential pair by virtuoso schematic editor

Instead of using a simple current mirror for transistors, a low voltage current mirror is used. This will enhance output swing range as it will have only Von of five transistors deducted from VDD. However, this configuration would induce two mirror poles in AC response which would be heavily detrimental to phase response. Figure 9(a) presents the folded cascode schematic of comparator circuit and Figure 9(b) presents the output stage of the comparator circuit.

The main function of output stage is to enhance overall OVSR and simultaneously providing gain enhancement to previous stage. However, it would induce extra pole in the AC response of the circuit. It is also desirable that this stage should consume low current. The output stage used in this design is a common source amplifier with a current source load.

Output is taken from joining point of output stage. The upper transistor is acting as a current source and bottom transistor is acting as a driver. The level shifter, which contains folded topology and resistive

divider network, ensures the common mode input voltage to 0.9 V. The DC level shifter is a resistive divider network, with input at one end and a feedback folded OTA at the other end. A class AB amplifier is used to get output swing from rail to rail. The advantage of class AB is low power, only one transistor is on at a time. The other implementation of class AB is useful in meeting output capacitance to compensate resistive load without affecting the gain. The class AB amplifier eliminates the current source limitation of charging and discharging the load capacitance is desirable. Beta multiplier is used to bias the transistor in saturation. The main advantage of it is the reference current is independent of voltage variation in the power supply.

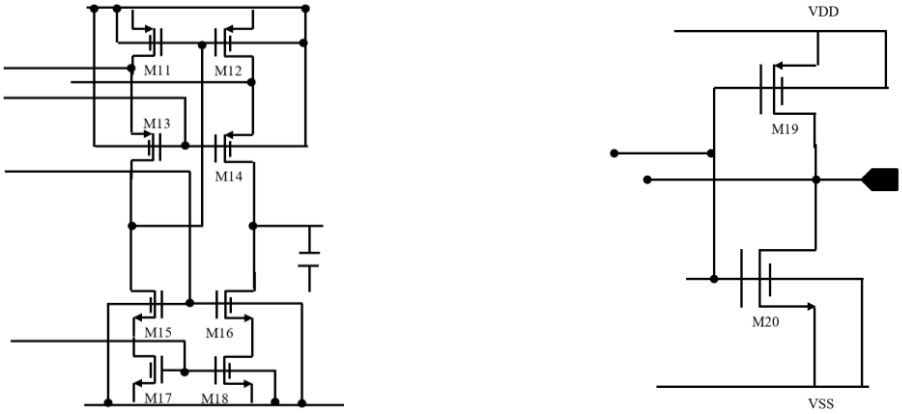


Figure 9. Comparator circuit, (a) comparator circuit folded cascode and (b) comparator circuit output stage

5. MODELLING OF COMPARATOR

The complete comparator which is integrated with all sub circuits integrated is shown in the Figure 10. Both out-n and out-p are connected to latch currently in the design. The latch is designed to produce both the logical outputs. But in the current design only the out-n will be used.

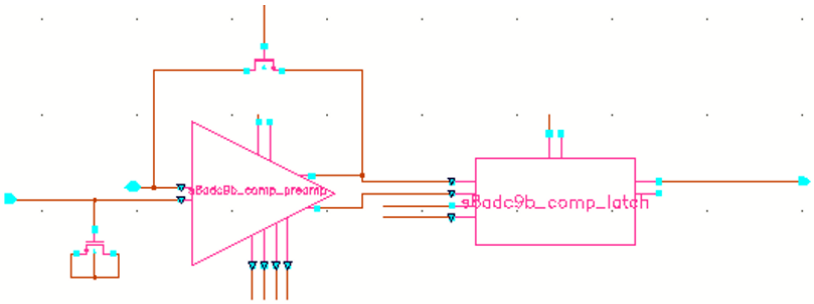


Figure 10. Schematic of comparator module

6. RESULTS AND DISCUSSION

The simulation of the comparator was done with a test case where a PWL signal was provided as the analog input to the comparator. Power supply was given as 1.2 V and the clock operating at 10 GHz is considered. A delay of 0.3 ns was introduced in the clock to compensate the layout parasitic capacitance causing the clock delay. The simulation results for the comparator operation are shown in the Figure 11. From the simulation results it is demonstrated that the output follows the input with the set delay of 0.3 nS. The positive transitions are 1.6 times faster than the negative transitions. To minimize the negative transition delay or to achieve symmetry it is required to choose transistors geometry appropriately. The comparator will be operated in the closed loop in the offset cancellation cycle. So, the gain and phase margin simulations were carried out using electronic neutron dosimeter (ELDO) simulator. The results are illustrated in the Figure 12.

From the results the phase margin is 65° and is between the considered specifications of 55° to 75°. The stabilization in phase margin is observed to be constant for variation in input frequency. Figure 13 presents

the transient analysis of the comparator circuit. The comparator circuit is connected with feedback to identify the voltage swing in the output. The input voltages are set to V_1=0 V and V_2=sinusoid varying from 0 to 1.2 V. The output of comparator follows the input with full voltage swing demonstrating the rail-to-rail voltage swing of the comparator circuit. In Figure 14 the input is a step input which goes from 0 to 0.5 V in 0.2 µS and remains constant thereafter. This input is used to find out the slew rate of the comparator and settling time of the comparator. Considering 10% of output rise which is observed at 40.1 µS and 90% of output rise time at 40.23 µS. The slew rate is observed to be 0.31 µS at which the output settles down to 0.5 V and remains stable. The overshoot of 0.05 is observed at 40.25 µS which is less than 10% of design specification.

Figure 15 represents the rail-to-rail output voltage swing between 0 to 1.76 V. Considering safety margin, the feedback circuit limits the voltage swing at the output to 1.25 V. The input common mode voltage for which the comparator remains stable is in the range between 0 to 1.2 V. Figure 16 represents the power supply rejection ratio (PSRR) at which the comparator exhibits constant value that is 81.2 dB till 10 MHz, after which the comparator exhibits linear behavior till 10 GHz. Table 5 presents the achieved comparator specification identified based on simulation results. The achieved specification is well within the required limits. The transconductance deviation is on the higher side of the required specifications. The achieved common-mode rejection ratio (CMRR) needs to be further improvised. From the simulation studies obtained considering standard test cases the slew rate is obtained to be 6 V/µS. For higher slew rate achieved the power dissipation is estimated to be 0.3 mW. The area, power density factor is optimized in layout design and the total area for the comparator is 0.3 mm^2. OTA based comparator designed in this work is demonstrated to handle higher currents with good stability factor. It is required to further improvise the transconductance deviations by design of proper biasing circuits.

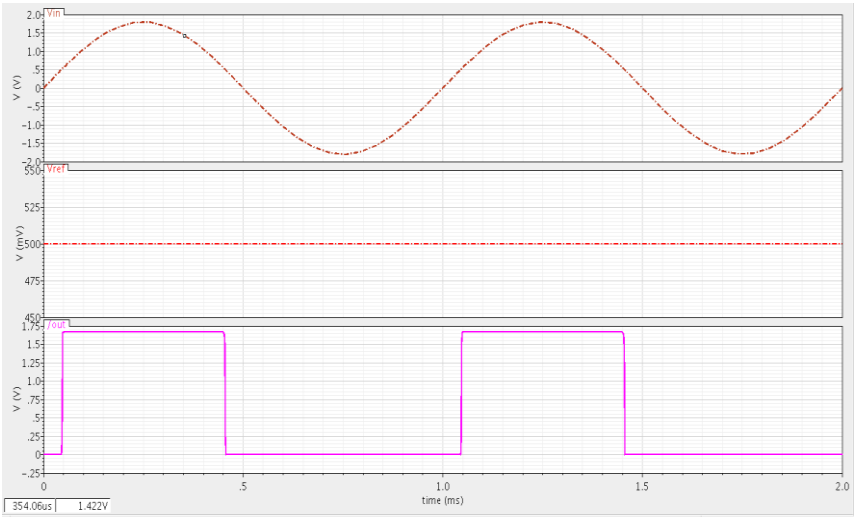


Figure 11. Simulation results of comparator

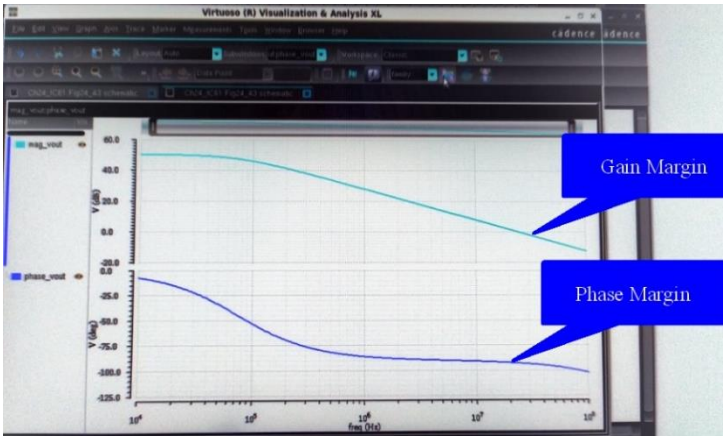


Figure 12. Gain and phase-margin plots of comparator

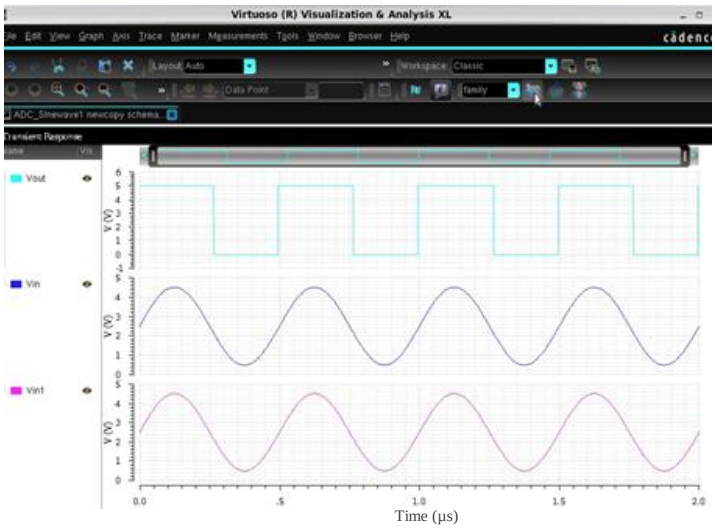


Figure 13. Transient analysis of comparator

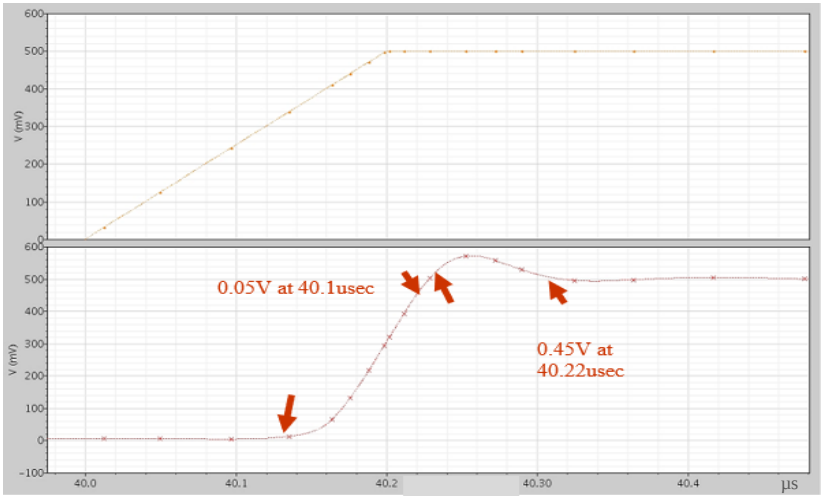


Figure 14. Slew rate and settling time of comparator

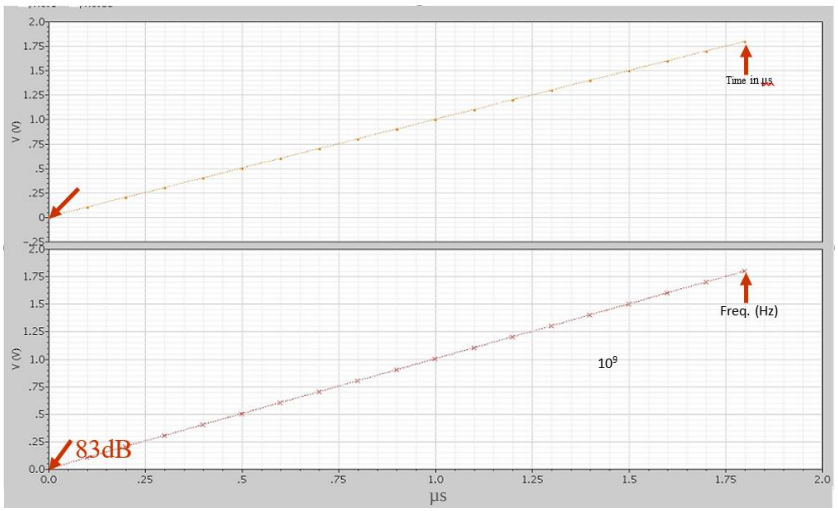


Figure 15. ICMR and output swing of comparator

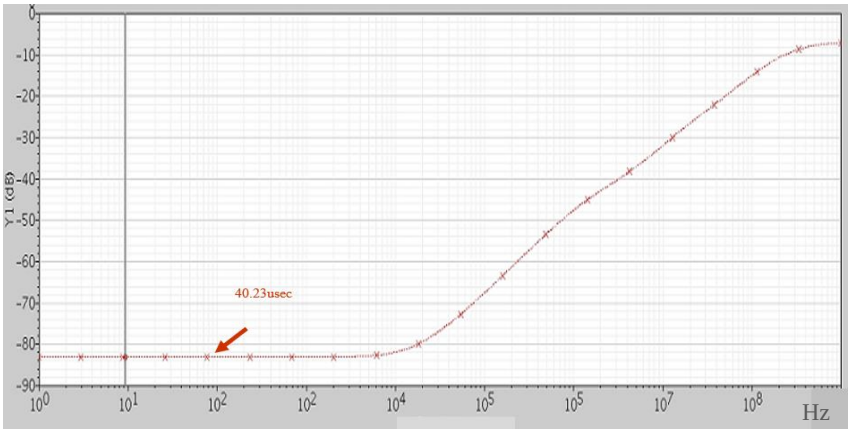


Figure 16. PSRR of comparator

Table 5. Comparison of required specifications and achieved results

Specifications	Required	Achieved
Gain of the Comparator	>100 dB	106 dB
Phase Margin	55° to 75°	65°
CMRR	65 dB to 90 dB	76 dB
Unity Gain Bandwidth	>2 GHz	5 GHz
Transconductance	0.4% to 0.8%	0.71%
Technology	22 nm	22 nm

7. CONCLUSION

A new method for achieving constant in a rail-to-rail OTA design is discussed in this work that is based on one input differential pair and level shifters. The common mode of the OTA is shifted to a constant value before the signal is input to the differential pair. Since the common-mode level of the differential pair is fixed, consistent operation for rail-to-rail common-mode inputs is achieved. Furthermore, since only one differential pair is used, there is no degradation in the CMRR for any input common-mode levels. Simulated results of this comparator show 0.71% deviation as compared with the desired requirements. The performances of OTA based comparator is suitable for data converters.

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