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Novel asymmetric space vector pulse width modulation for dead-time processing in three-phase power converters

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ABSTRACT

This research analyzes the asymmetric control strategies in multilevel inverters, including asymmetric techniques in space vector modulation of power converters. Modulation parameters such as reference voltage vector (V_{ref}), switching time, and duty cycle are derived in the three-dimensional spatial vector geometry formulation. Asymmetric space vector pulse width modulation (SVPWM) is unique in specifying modulation parameters, has unequal tetrahedron patterns, accompanied by application examples for the upper and lower sector pairs of a tetrahedron. The combination of the switch in the form of an inclined cylinder produces twelve pairs of asymmetric tetrahedrons where the voltage vector positions are in the other twenty-four tetrahedrons. The calculation shows processing dead-time in switching, which is used for current compensation in three-phase power converters.

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1. INTRODUCTION

Space vector pulse width modulation (SVPWM) was one of the switching signals in power converters obtained from intersection triangular carrier waves and fundamental sinusoidal waves in space vector due to the necessity to calculate the switching time for the modulation process. The switching combination carried out in αβ0-coordinate using a three-dimensional space vector produced sixteen voltage vector used to adjust the modulation signal in three-phase power converters [1], [2]. According to [3] the switching characteristics occur due to high total harmonic distortion (THD) and lengthy iteration. Therefore, improvements were needed by trigonometric equation to determine the right space vector. This method was developed to provide problem-solving solutions although it has a small error rate.

Three-phase power converters were used to compensate for harmonic distortion in three-phase shunt active power filters (APF). Compensation was suitable for improving the electrical power quality in these devices, which were carried out based on hysteresis current, and used for harmonic, reactive power, and neutral current compensations [4]. Meanwhile, interpretation based on the d-q theory or the synchronous reference frame (SRF) theory by [5] stated that single-phase APF is also used to extract reference current. The experiment results obtained from this single-phase have similarities to the three-phase APF in the form of improved frequency-independent operation, accurate reference current extraction, and relatively fastest transient response. A mathematical model has been developed by the source current control strategy to balance the supply currents of a three-phase four-wire distribution network to three phase power converters

based on the principle of the internal sinusoidal model [6]. The proposed strategy guarantees good compensation performance and the experimental results indicated that this strategy significantly increases precision compared to conventional methods especially in the imbalance load current compensation.

Asymmetric "word" was defined according to the research on multilevel inverters (MLI), which have been carried out in several studies and were validated between mathematical calculations, simulations, and experimental measurement. According to [7] asymmetric on MLI was designed to minimize the number of switches power electronic devices in high voltage applications. Asymmetric also was compared between multilevel inverters in terms of the number of switches, gate driver circuits, and blocking voltage, thereby leading to the maximum number of output voltage levels suitable for high-voltage applications with low-voltage power converters. Furthermore, asymmetric consists of two configurations, the first has an output voltage spike and a higher harmonic distortion of voltage and current, while the second has a better output voltage without surge and lower harmonic distortion. Meanwhile, according to [8] asymmetric was an effort control to eliminate repeated harmonic spectrums over a wide range of MLI with different displacement patterns for each sector. The selective harmonic elimination technique obtained was used to maximize the solution of the switching angle.

Research on the modulation of three-to-six-phase matrix converters control with asymmetric six-phase output states produced consisting of the displacement of voltage vector in two sets of three-phase isolated loads [9]. A voltage vector was used to synthesize a reference voltage and to obtain a sinusoidal output by an asymmetrical load. It was further maintained to achieve a maximum gain output of the voltage vector and to ensure the reactive power at unity from the supply utility of the power factor. According to [10] asymmetric is used to balance capacitor voltage control with differences between the upper and lower legs in a space vector. Conventional capacitor voltage control led to a poor operating performance on the alternating current (AC) and direct current (DC) sides with the occurrence of unbalanced frequency and voltage oscillations. A mathematical model was developed to balancing capacitor voltage control between legs of the space vector with high efficiency. This was carried out by distributing the capacitor voltage evenly across each leg and balancing the capacitor voltage between different legs. In another research conducted by [11], [12], an asymmetric definition was used for microgrid power flow analysis using a hybrid technique. Similarly, it was used in adjusting the amount that is not the same between the output voltage and dc source on the MLI. Asymmetric ideas are also used in field programmable gate array (FPGA) techniques [13] and SVPWM to produce an imbalance of the two outputs between the voltages in the main and auxiliary windings [14]. Three-dimensional space vector modulation is a signal generation modulation by adjusting the voltage vector in the ab0 coordinate system. The voltage vector is the result of a combination of switching active power filters in a three-phase system. For three-dimensional spatial vector modulation, this switching combination produces sixteen voltage vectors in the form of a vertical cylinder.

SVPWM in three-phase power converters produced compensate current used to reduce distortion in an electrical power system. Asymmetric SVPWM was developed from the analysis of a pair of tetrahedrons of the voltage vector in a skewed cylindrical shape. Asymmetric SVPWM has an inequality form of tetrahedron pairs in each sector. In the asymmetric SVPWM model, voltage vector organized and selected in the three-dimensional skewed cylindrical sector corresponding to change the load current phase angle was distorted with the result capable of determining reference voltage vector (V_{ref}). Furthermore, it produced the twenty-fourth voltage vector switching combination used to determine the reference voltage vector (V_{ref}), duty cycle, and switching time. A control signal can be used in three-phase power converters. The reference voltage vector (V_{ref}) was determined by a single line drawn from three voltage vectors to obtain a tetrahedron. Duty cycle and switching time were used to the modulation control signal in three-phase power converters. It produced compensation currents that can be used to reduce distortion [15], [16]. Therefore, this research analyzes novel asymmetric SVPWM in αβ0-coordinates, modulation parameters determination, and describes its application to dead-time processing in three-phase power converters. This research is described as follows: section 2 analyzes several analytical steps in determining modulation parameters. Section 3 presents the calculation results and the occurrence of the dead time process. Finally, section 4 provides conclusions and applications of the asymmetric SVPWM concept.

2. RESEARCH METHOD

2.1. Step of an asymmetric SVPWM

An asymmetric voltage vector in a skewed cylindrical shape was projected from the pqr-coordinate to the αβ0-coordinate (Clarke transformation) obtained from the switching combination of voltage vector [15], [16]. Furthermore, three voltage vector combinations in skewed cylindrical shape coordinates were made into twelfth of asymmetrical tetrahedron pairs for modulation control with side lengths of ½ V_{dc}. The determining steps of an asymmetric SVPWM in modulation parameters were carried out by [17] where the

difference lies in a three-dimensional skewed cylindrical shape and used as the basis of analysis. The determining step of the modulation signal tends to produce a control signal in three-phase power converters. The compensation current control was carried out by the switching process. The modulator is used for current control and generates a modulation signal, which produces a compensating current that can be injected into the load current to be distorted hence, the source current becomes sinusoidal.

The combined result of the twelfth asymmetrical tetrahedron pair which voltage vector position produces twenty-fourth asymmetric voltage vectors. There were six pairs of asymmetric prisms occupied by twenty-fourth coordinate points in a skewed cylindrical shape. The position of the voltage vector in a skewed cylindrical three-dimensional space is created in a table with each coordinate visible in a three-dimensional cylindrical space. Table 1 shows that a total of twenty-fourth voltage vectors were used to describe asymmetrical tetrahedron pairs. It appears that the important quantities were needed in the prismatic slice in (1/2, 1/4, and √3/4) V_{dc} of long sides.

With Euler's angular rotation method as a projection of xyz coordinates to ab0 coordinates, an oblique cylinder with length $V_a=V_b=V_0=½\ V_{dc}$ is formed. This description of the inclined cylinder is similar to the strategy in [18], [19] when determining the voltage vector using the abc coordinates. The difference with this research lies in the initial states of (1111) and (0000), as well as those that do not coincide with each other in one position.

Table 1. Asymmetric voltage vector length of ½ V_{dc} in a skewed cylindrical shape

Voltage vector	Vα/a	Vβ/a	V0/a	Voltage vector	Vα/a	Vβ/a	V0/a
V_1	0	0	0	V_{13}	0	$\sqrt{3/2}$	0
V_2	0	0	-1/2	V_{14}	1/4	$\sqrt{3}/4$	0
V_3	0	0	1/2	V_{15}	-1/4	$\sqrt{3}/4$	1/2
V_4	-1/4	$-\sqrt{3}/4$	-1/2	V_{16}	-1/4	$\sqrt{3}/4$	0
V_5	1/4	$-\sqrt{3}/4$	1/2	V_{17}	-1/2	0	1/2
V_6	1/2	0	-1/2	V_{18}	-3/2	$\sqrt{3}/4$	1/2
V_7	1/4	$\sqrt{3}/4$	-1/2	V_{19}	-1/2	$\sqrt{3}/2$	1/2
V_8	-1/4	$\sqrt{3}/4$	-1/2	V_{20}	0	$\sqrt{3/2}$	1/2
V_9	-1/2	0	-1/2	V_{21}	1/4	$\sqrt{3}/4$	1/2
V_{10}	-1/2	0	0	V_{22}	1/2	0	0
V_{11}	-3/4	$\sqrt{3}/4$	0	V_{23}	1/4	$-\sqrt{3}/4$	0
V_{12}	-1/2	$\sqrt{3}/2$	0	V_{24}	-1/4	$-\sqrt{3}/4$	0

2.2. Modulation parameters

In an asymmetric model of skewed cylindrical, the tetrahedron of each sector has unequal upper (positive) and lower (negative) pairs of voltage vectors. The pairs of the upper (positive) and lower (negative) sectors of tetrahedron produced different duty cycles according to each pair's interval period. The Centre point of the upper (positive) and lower (negative) sectors were in the V_{16} and V_1 vectors. The reference voltage vector (V_{ref}) is determined when three voltage vectors are connected closest to the coordinate center. Defining reference voltage vector (V_{ref}) needs some basic principles of geometry in accordance with the formulation developed by [20]–[22].

After determining the reference voltage vector (V_{ref}) the next step is to determine the time duration of each of the tetrahedrons, to connect the voltages (V_{an}, V_{bn}, V_{cn}, and V_{nn}) and switching time duration of each conductor with A, B, C, and neutral legs obtained on three-phase power converters. Duty cycle in % was obtained later by comparing the duration time of each tetrahedron with a period cycle.

In this study, the concept of three-dimensional SVPWM [23] and control of the NPC [24] also used the idea of offset voltage in determining the modulation parameters [25]. The results of the analysis obtained have not yet reached the simulation and experimental stages. This method is fascinating because, for asymmetric tetrahedron pairs, the calculation results show dead-time processing in three-phase power converters. Calculations using offset voltage are also carried out in determining the band-gap of the semiconductor material recombination process, especially in solar cells [26] and in the hall effect [27].

2.3. Analytic solution for asymmetric SVPWM

Calculation of asymmetric SVPWM was performed to determine modulation parameters such as reference voltage vector (V_{ref}), switching time duration, and duty cycle on the upper sector and the lower sector of a tetrahedron. Table 2 neighboring three voltage vectors formed the tetrahedron of the asymmetric voltage vector model. Modulation parameters are derived from three voltage vectors neighboring locations as

shown in Table 2. Figure 1 shows a pair of the first upper sector (S11) of a tetrahedron and the third lower sector (S32), as partner tail.

Table 2. Twenty-fourth tetrahedron form of asymmetric voltage vector

Point 0	Point A,B,C	Point 0	Point A,B,C	Point 0	Point A,B,C	Point 0	Point A,B,C
V_{16}	V_{20}	V_{16}	V_{18}	V_1	V_{23}	V_1	V_{23}
	V_{12}		V_9		V_{19}		V_{19}
	V_{21}		V_8		V_9		V_9
V_{16}	V_{12}	V_{16}	V_9	V_1	V_{20}	V_1	V_9
	V_{22}		V_8		V_{16}		V_{10}
	V_{13}		V_1		V_7		V_{24}
V_{16}	V_{14}	V_{16}	V_1	V_1	V_{16}	V_1	V_{10}
	V_{22}		V_2		V_{19}		V_{11}
	V_{18}		V_{20}		V_8		V_{24}
V_{16}	V_{15}	V_{16}	V_{21}	V_1	V_9	V_1	V_{12}
	V_{18}		V_{20}		V_{19}		V_{11}
	V_{19}		V_6		V_3		V_{20}
V_{16}	V_{19}	V_{16}	V_{21}	V_1	V_9	V_1	V_{20}
	V_1		V_{22}		V_{10}		V_{12}
	V_{24}		V_7		V_3		V_{16}
V_{16}	V_{20}	V_{16}	V_{22}	V_1	V_{10}	V_1	V_{16}
	V_1		V_{18}		V_{11}		V_{17}
	V_{12}		V_7		V_4		V_{19}

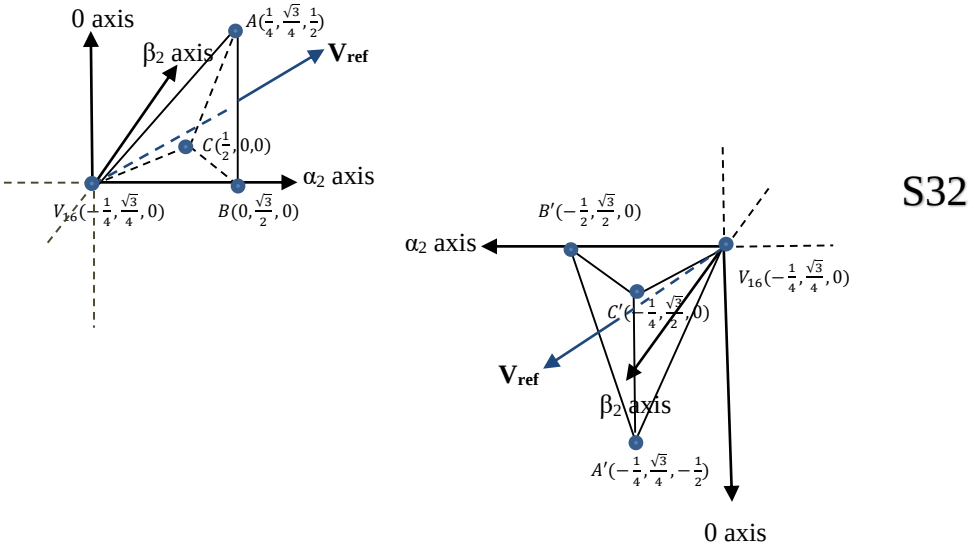

Figure 1. Asymmetric reference voltage vector (V_{ref}) as result pair of the first upper sector (S11) and "tail" the third lower sector (S32) of a tetrahedron

3. RESULTS AND DISCUSSION

Calculation switching time between the first (S11) and third sectors (S32) has an asymmetric result (unequal). For example, on leg A active filter, a switch to A11 or A32 does not ensure the occurrence of an equal time modulator in unison. Calculation results of modulation parameters from a frequency of 200 kHz or a period of 1 microsecond (µs) obtained leg A switch of A11 or A32 with an asymmetric tetrahedron in unequal time. Figure 2 shows the switching signal for a switch of A11 and A32. Therefore, when a switch of A11 in ON position in 0.368 µs (stage I) it is first then in OFF position in a period of 4,263 µs (stage III) before turning ON again at 4,632 µs (stage V). A switch of A32 has an asymmetric commutation process in line with A11. At the same time, at first in OFF position on a switch of A32 occurs during 0.564 µs (stages I and II) after which it experiences in ON position in 3,872 µs (stage III) and finally in OFF position at 4,443 µs (stages IV and V). There has been overlapping in the ON-OFF process between a switch of A11 and a switch of A32 (stages II and IV). Switching time overlapping between a switch of A11 and a switch of A32 were caused by asymmetric SVPWM and this state name was dead-time processing.

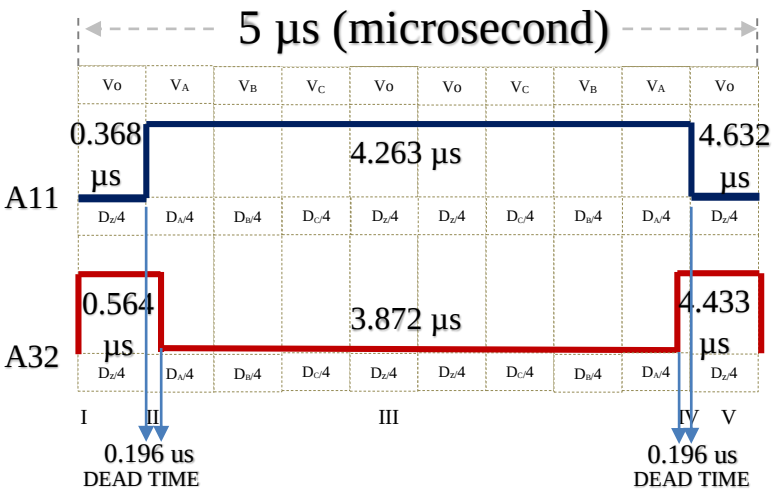

Figure 2. Dead-time between a switch of A11 and a switch of A32 in asymmetric SVPWM

In dead-time processing, compensation current needs to be limited during commutation. A switching signal that passes through leg A in the first condition when inrush current in a switch of A11 was still in ON position while a switch of A32 was switched OFF [28]–[30]. Figure 3 shows that a switch of A11 in ON position in 0.368 µs at the first time and harmonic current through a switch of A32 in separating capacitor. A switch of A32 flowed harmonic current for 0.564 µs and their position was a pause in the process of ON-OFF (0.564-0.368) µs=0.196 µs. This indicates that were a time duration of 0.196 µs, which closes simultaneously between a switch of A11 and A32.

Compensation current regulation was carried out by a modulator in three-phase power converters. The current connection flowed to the separated capacitor at (–½ V_{dc}) and (+½ V_{dc}) DC voltage and then in opposite direction with the result injected into the grid. Asymmetric SVPWM from calculation was obtained from switching combinations on each gate signal in these devices.

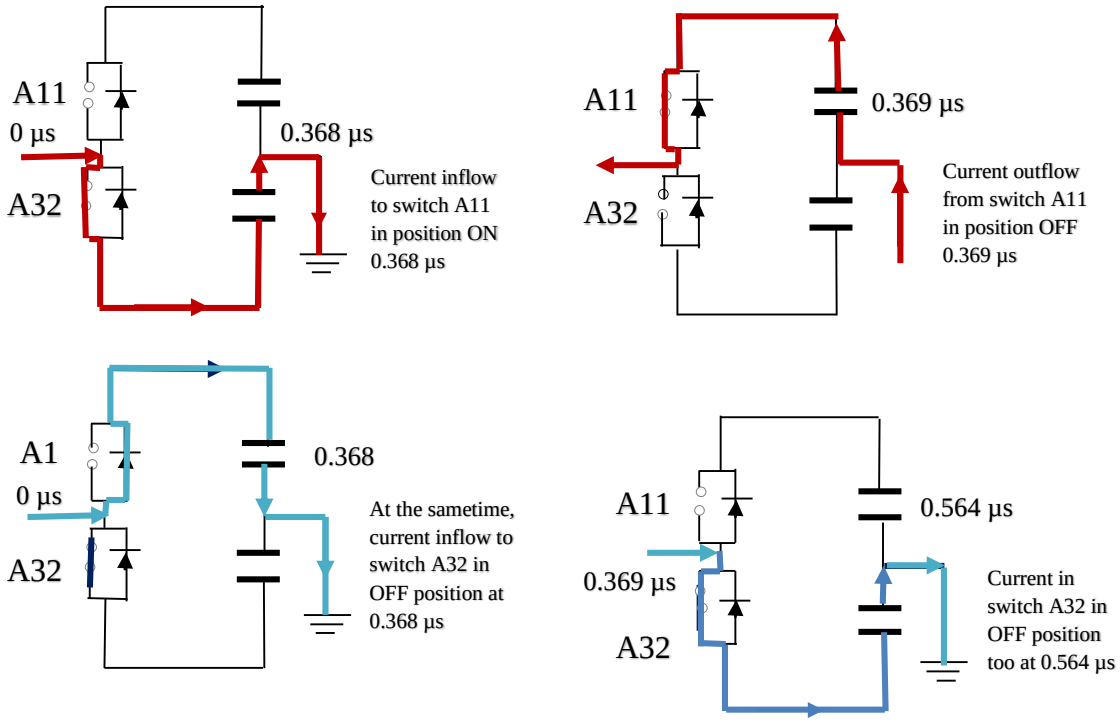

Figure 3. Dead-time closes simultaneously between a switch of A11 and a switch of A32

4. CONCLUSION

A control signal from asymmetric SVPWM generates a compensation current used to reduce distortion with the switching process leading to dead time. This indicates that the time duration closes simultaneously between a switch of A11 and a switch of A32 on three-phase power converters. Furthermore, asymmetric SVPWM research still needs to be developed especially for its application which uses electric power systems. Subsequent research is that the SVPWM asymmetric technique was developed as a control to compensate for currents in power converters. The dead-time process caused by different tetrahedron pairs is an interesting phenomenon to observe.

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