

## Design and development of multiphase buck converters for voltage regulator modules

Mini Puthenpurakkal Varghese<sup>1</sup>, Ashwathnarayana Manjunatha<sup>1</sup>, Thazhathu Veedu Snehaprabha<sup>2</sup>

<sup>1</sup>Department of Electrical and Electronics Engineering, Sri Krishna Institute of Technology, Bangalore, India

<sup>2</sup>Department of Electrical and Electronics Engineering, Presidency University, Bangalore, India

### Article Info

#### Article history:

Received Feb 21, 2021

Revised Jun 17, 2021

Accepted Jun 29, 2021

#### Keywords:

Compensation

Frequency analysis

Multiphase buck converter

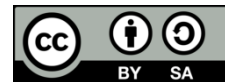
Ripple cancellation

Transient analysis

### ABSTRACT

Modern microprocessors in high-power applications require a low input voltage and a high input current, necessitating the use of multiphase buck converters. As per microprocessor computing complexity, the power requirements of the switching converter will also be more important and will be increasing as per load demand. Previous studies introduced some methods to achieve the advantages associated with multiphase regulators. This paper presents an effective closed-loop control scheme for multiphase buck converters that reduces ripple and improves transient response. It is suitable for applications that require regulated output voltage with effectively reduced ripple. The analysis began with a simulation of the entire design using the OrCAD tool, followed by the construction of a hardware setup. Experiments on a 200 Khz, 9 V, 12 A, 2-phase buck voltage regulator were conducted and the proposed experiment found to be useful.

This is an open access article under the [CC BY-SA](https://creativecommons.org/licenses/by-sa/4.0/) license.



### Corresponding Author:

Mini Puthenpurakkal Varghese

Department of Electrical and Electronics Engineering, Sri Krishna Institute of Technology

Bangalore-560090, Karnataka, India

Email: mini.jinan@gmail.com

## 1. INTRODUCTION

To reduce power consumption, modern data processing systems are required to lower the voltage level of the central processing unit (CPU) power supply. As a result, the power supply is able to deliver a large current while maintaining low voltage levels [1]-[3]. The modular approach to constructing DC-DC converters has been used for more than two decades to meet specific input/output needs, such as good transient response and reduced ripple. However, single-cell converters are not efficient in achieving these requirements. In this regard, to meet design requirements, two or more single-cell converters are connected in parallel [4]. The main problem in a single stage buck converter is its increased ripple content at the output voltage. In single-stage converters, the traditional method for reducing output ripple voltage was to use multiple stages of filters, but this process adds to the circuit's complexity. This issue has resulted in research on multiphase converters. Multiphase power converters are made up of M equal converters connected in parallel, splitting total current into M routes or phases. When compared to a single converter, multiphase converters reduce switching and conduction losses by dividing the total current among phases. Interleaving each phase current ripple enhances total current ripple features, including amplitude reduction and frequency increase to M times the switching frequency  $F_{sw}$  [5]-[7]. The multiphase buck topology has the advantage of becoming extremely simple to implement and providing great transient response, very low ripple voltage, high efficiency, small size, and low cost. The load is divided by the number of phases, while the effective switching frequency is multiplied by the number of phases [8].

In multiphase converters, ripple reduction in the output voltage can be achieved by a technique called ‘current ripple cancellation among the phases. It is a key characteristic of multi-phase switching converters since it allows each converter in the system to run at a higher ripple than the total load-current ripple due to phase interleaving [9]-[13]. The overall current ripple of the output inductors is the most important influencing element on the voltage ripple. Because the multiphase identical filter inductance restricts the converter’s power transfer speed, the output capacitor is employed to release its conserved energy to load during the transient period [14]. Individual inductor current ripples are neutralized, lowering the overall ripple current that flows through the output capacitor. The output voltage ripple can be greatly reduced with such ripple cancellation [15]. The current ripple going into the output is minimized when the inductor current is cancelled, requiring a reduced capacitance to meet the very same output voltage ripple demands [14].

Another vital concern in voltage regulator modules is system stability. It’s a difficult control loop problem to stabilize a buck converter with multiphase. The feedback loop compensation of a multiphase DC-DC converter is necessary to supply the regulator circuit with an adequate level of stability. A prototype is designed and evaluated in this work. This paper describes how to attain stability via analysing the loop. The open-loop gain/phase response (the transfer function) of the entire chain is examined using a bode plot, and the transfer function is shaped using the closed loop compensation to balance the converter across a range of input/output configurations [15].

This study presents a two-phase multiphase buck converter. The following is a breakdown of the structure of this paper. The second section explains the design, mathematical model and simulation results of a two-phase buck converter. The experimental data that validate the simulation results achieved from the mathematical model are described in the third section, and the conclusion is described in the fourth section.

## 2. MULTIPHASE BUCK CONVERTER

Figure 1 presents a multi-phase buck converter, which is a circuit topology in which basic buck converter circuits are paralleled between the input and load [16]. Multiphase buck converter improves dynamic performance, ripple cancellation, overall efficiency and the system stability over the entire operating range. Each buck converter stage is with its inductor and set of power metal–oxide–semiconductor field-effect transistors (MOSFETs). Low ripple content in the input and output current is one of the advantages of multi-phase buck converters over single-phase buck converters. It lowers the values of both input and output capacitors while also improving dynamic performance [17]. Each inductor will be attached to the power supply at distinct phases in steady state, with phase intervals equal to  $360^\circ=np$ , where  $n$  indicates the number of stages and  $p$  indicates phase angle (or inductors that are connected in parallel). The output load is distributed across all inductors, causing the DC across each inductor to decrease as  $np$  decreases. Because the separate inductor currents are at different phases, the output voltage ripple is greatly decreased as a result of the reduced output current ripple [18].

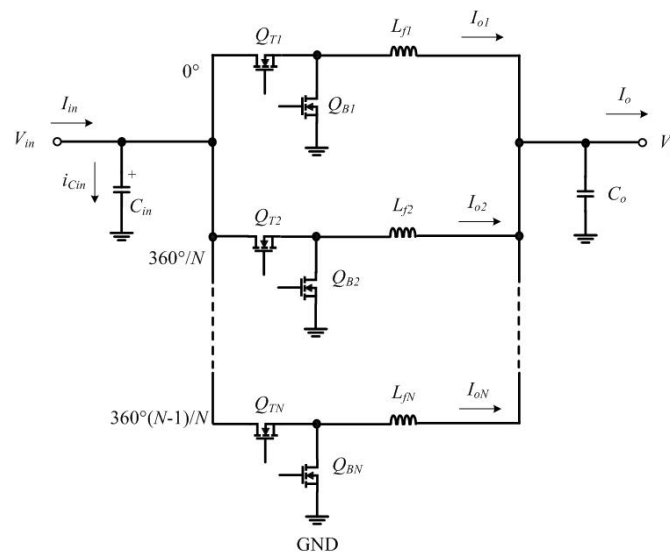


Figure 1. Multi-phase buck converter with N phases

System stability is another factor in multiphase buck converters. The input voltage is one of the most essential circuit characteristics for power supply stability. One of the causes of power supply instabilities is a change in input voltage [19]. Many improved control algorithms for Buck converters have been presented, taking into account the output voltage regulation problem while considering parameter uncertainties or load changes [20]. A system can be stabilized by adding an appropriate compensation technique. The power stage is made up of four power-train modules, each with its own input and output. A comparator, error amplifier, and pulse-width modulator comprise the feedback loop controller [21]. A compensator would receive the voltage output signal. A compensational voltage signal is then generated by the compensator. To generate a voltage, the current signal will travel via a resistor. This will then be transferred to a comparing circuit, where it will be compared to a present value. Finally, the comparing voltage and clock voltage signals will be supplied to a pulse width modulation (PWM) generator, which will generate a PWM voltage signal. The converter will then be controlled by a PWM voltage signal [22]. This control regulates the output voltage during each transient since every DC-DC converter needs to have appropriate regulation for proper functioning.

## 2.1. Design

Calculations capacitor  $C_{out}$

$$C_{out} = \frac{I_{pp}}{8f_{SW} \times \Delta V_{out(ripple)}} = 3.673 \mu\text{F} \quad (1)$$

$$L = \frac{V_{out}(1-D)}{f_{SW} \times I_{p-p}} \quad \left| \begin{array}{l} 25\% \text{ of o/p current} \\ I_{p-p} = 0.25 \times \frac{I_o}{n} = 48 \mu\text{H} \end{array} \right. \quad (2)$$

Selected an inductor close to 48 $\mu\text{H}$  and with a current of 3 A (12 A/4 phases).

$$L = 68 \mu\text{H}$$

$$\begin{aligned} V_{in} &= (45-65) \text{ V} \\ V_{out} &= 9 \text{ V} \\ I_{out} &= 12 \text{ A} \\ V_{out(ripple)} &= 1\% \text{ of } 9 \text{ V (90 mV)} \\ f_{SW} &= (200-800) \text{ KHz} \end{aligned}$$

Inductor losses:

Inductor conduction losses

$$P_L = I_{RMS}^2 \times R_{DCR} \quad (3)$$

$R_{DCR} \rightarrow$  DC resistance of the inductor

$$I_{RMS}^2 = \frac{I_o^2}{4} + \frac{\Delta I^2}{12} \quad (4)$$

As per specification  $\Delta I$  (Output ripple current) is 0.75A. Output current ripple ( $\Delta I$ ) = 25% of  $I_{out}$ .

$$= \frac{.25 \times I_o}{n} = 0.75\text{A}$$

But since the inductor value is selected as 68 $\mu\text{H}$ , need to recalculate  $\Delta I$  as per the new inductor value.

$$L = \frac{V_{out}(1-D)}{f_{SW} \times I_{p-p}} \quad (5)$$

$$\begin{aligned} (\Delta I) I_{p-p} &= \frac{7.2}{200\text{K} \times 68\mu} \\ &= 0.529 \text{ (Ripple current in single Phase)} \end{aligned}$$

Substitute  $I_{p-p}$  ( $\Delta I$ ) in (4)

$$I_{RMS}^2 = \frac{12^2}{4} + \frac{[\Delta I]^2}{12} = 9.023 \quad (6)$$

Substitute in (1)

$$P_L = I_{RMS}^2 \times R_{DCR} = 1.353 \quad (7)$$

Since  $\frac{[\Delta I]^2}{12}$  is a small contribution of AC ripple current that is the DC Component and if can be neglected. Therefore, the power dissipated in the inductor can be calculated as;

$$P_L = I_o^2 \times R_{DCR} = 1.35 \text{ W} \quad (8)$$

Power dissipated in the MOSFET:

Power the dissipated in the High side MOSFET (low side switch is a diode)

$$PQ = I_{RMS}^2 \times R_{DS(ON)} \quad (9)$$

$$I_{RMS}^2 = \frac{V_o}{V_{inmin}} \left[ \frac{I_o^2}{n} + \frac{\Delta I^2}{12} \right] = 1.8$$

$$PQ = I_{RMS}^2 \times R_{DS(ON)}$$

Need to select switch to get  $R_{DS ON}$ .

MOSFET can be selected as per max voltage across MOSFET and maximum current through it. Maximum voltage across MOSFET with maximum supply voltage such as 65 V and 30% more.

$$\begin{aligned} 65+20 \text{ V} &= 85 \text{ V} \\ I_{peak} &= I_{dc} + \Delta I \\ &= 3.529 \text{ A} \end{aligned} \quad (10)$$

Now selecting MOSFET, with;

$$\begin{aligned} V &= 85 \text{ V} \\ I_{peak} &= 3.529 \end{aligned}$$

Select a MOSFET,

RD3P050SNFRA, 100 V ( $V_{DSS}$ ), 5 A ( $I_D$ )  $R_{DS(ON)(MAX)}$  [190 mΩ]

From (3)

$$\begin{aligned} PQ &= I_{RMS}^2 \times R_{DS(ON)} \\ &= 342 \text{ mW} \end{aligned} \quad (11)$$

Diode losses

Need to select a schottkey diode with the voltage across diode and current through it

$$\begin{aligned} V &= 65, \\ I &= 3 \text{ A} \end{aligned}$$

Selected a schottkey diode

RBO88BM100FH,  $V_R = 100 \text{ V}$ ,  $I_o = 10 \text{ A}$ ,  $V_F = 0.74 \text{ V}$

Diode losses,

$$\begin{aligned} &= V_F \times I_{RMS} \\ &= 5.34 \end{aligned} \quad (12)$$

## 2.2. Simulation results

Orcad software is used to analyze a two-phase buck converter. Figure 2 shows a simulation model schematic drawn for time-domain analysis. Figure 3 is the ripple current in each phase of the two-stage buck

converter, which is simulated. Because the simulation is two-phase, the ripple current at the output capacitor cancels out, leading the ripple at the output voltage to be reduced to a larger extent. Frequency domain analysis is done by creating an open-loop circuit simulation model as shown in Figure 4. Figure 5 shows a bode plot obtained from the open-loop analysis, which also shows the position of poles and zeros, later compensated for in closed-loop analysis. Figure 6 shows the controlled system [23] with compensation, which is known as a compensated circuit. The frequency response of a compensated closed-loop converter with the desired bandwidth is shown in Figure 7.

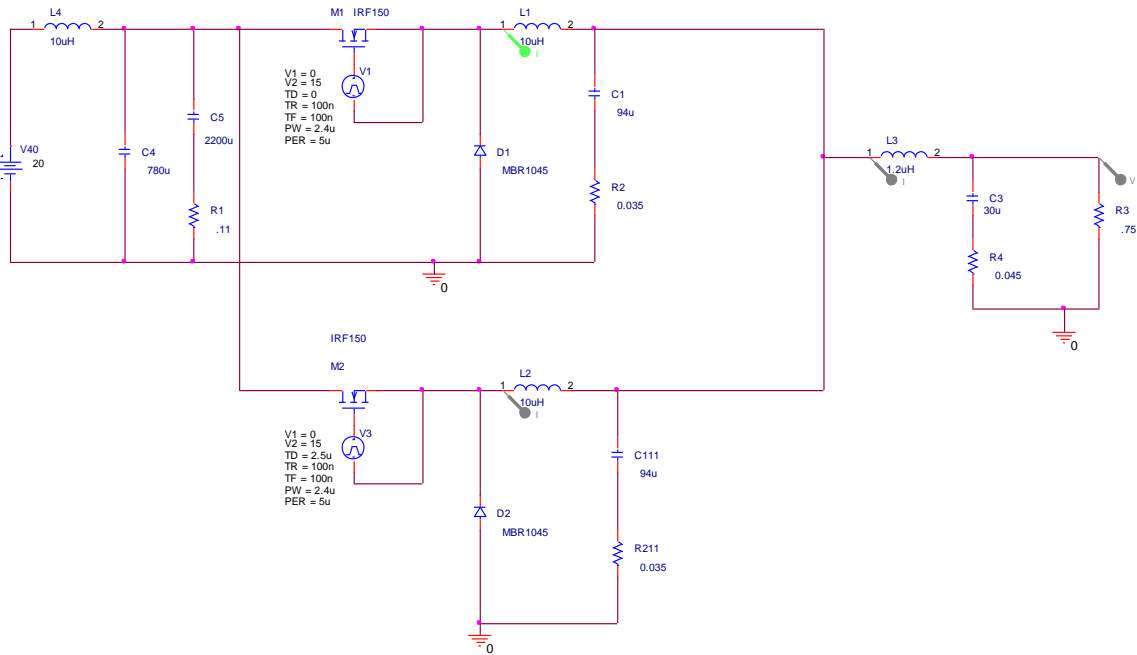


Figure 2. Simulation model for transient analysis

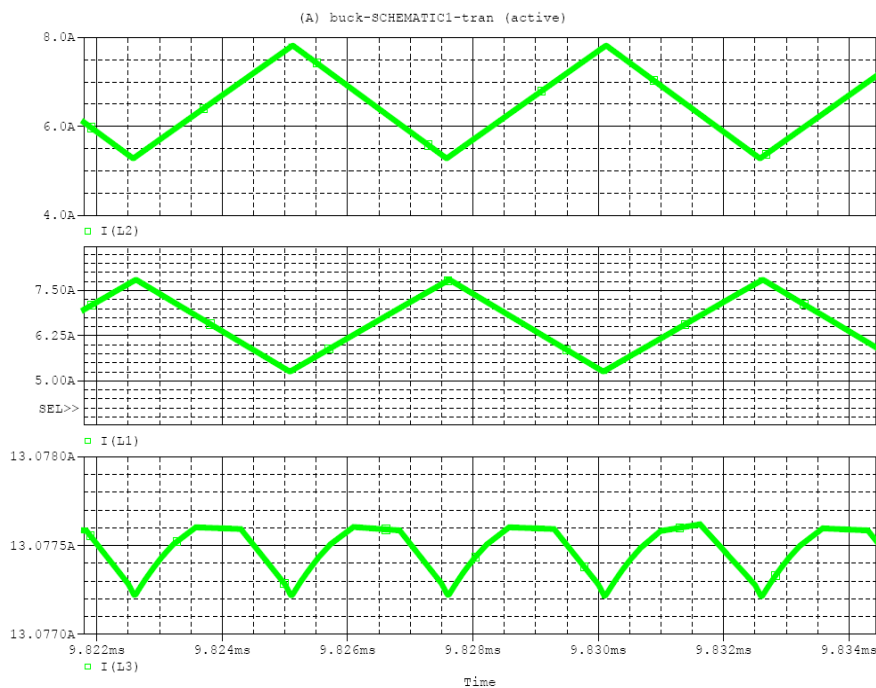


Figure 3. Ripple current cancellation

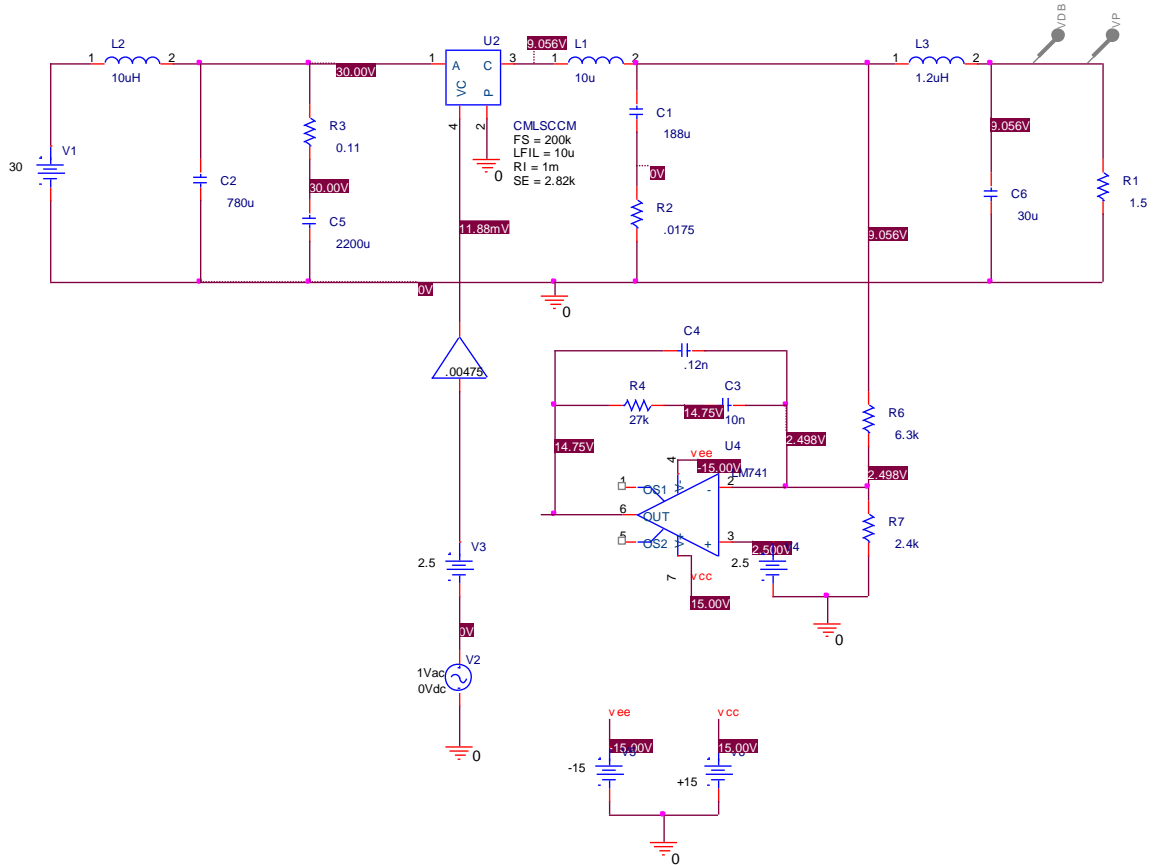


Figure 4. Simulation model for open-loop analysis

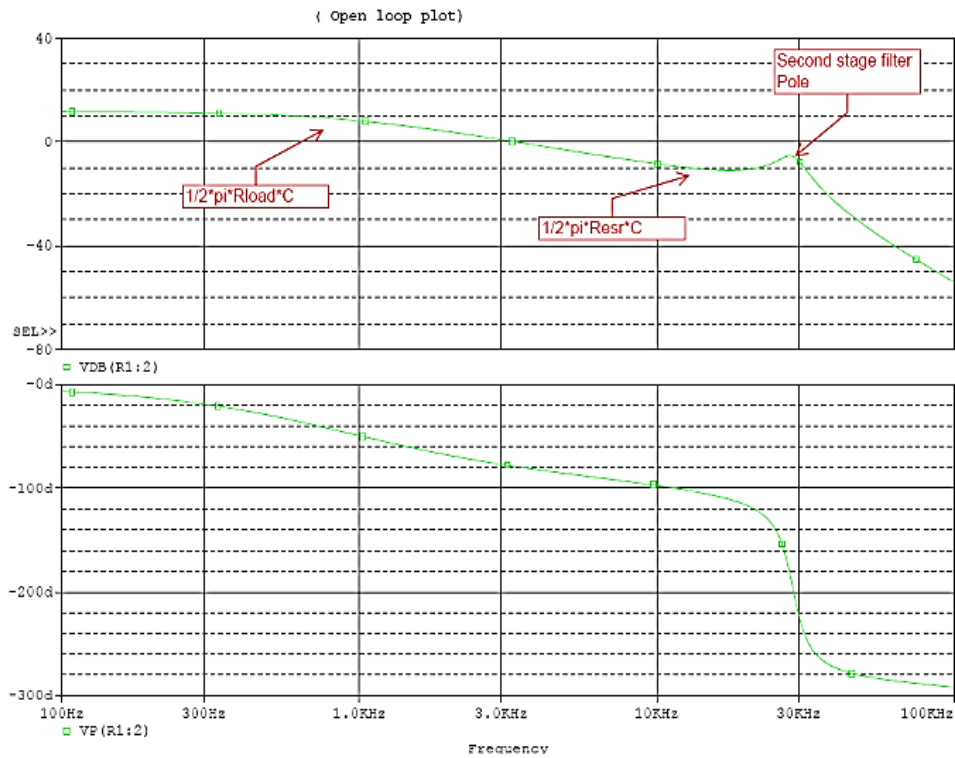


Figure 5. Open-loop frequency response

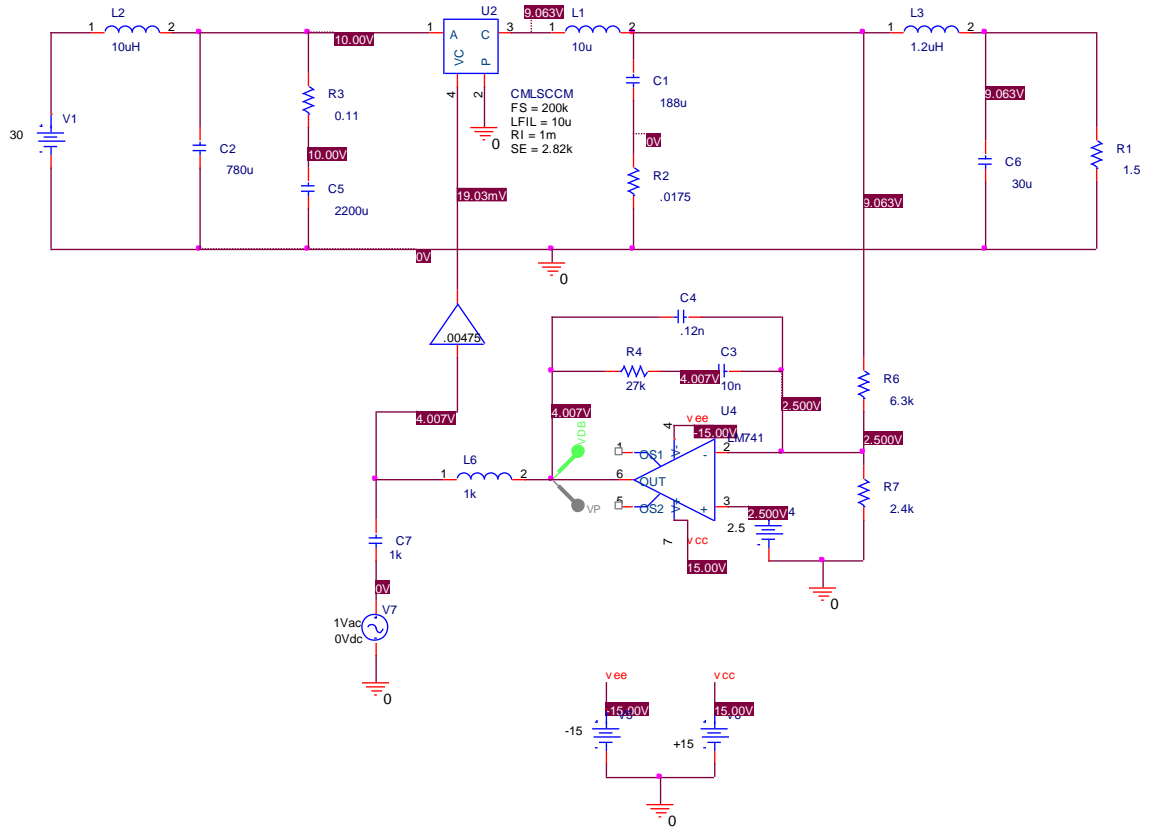


Figure 6. Simulation model for closed-loop analysis

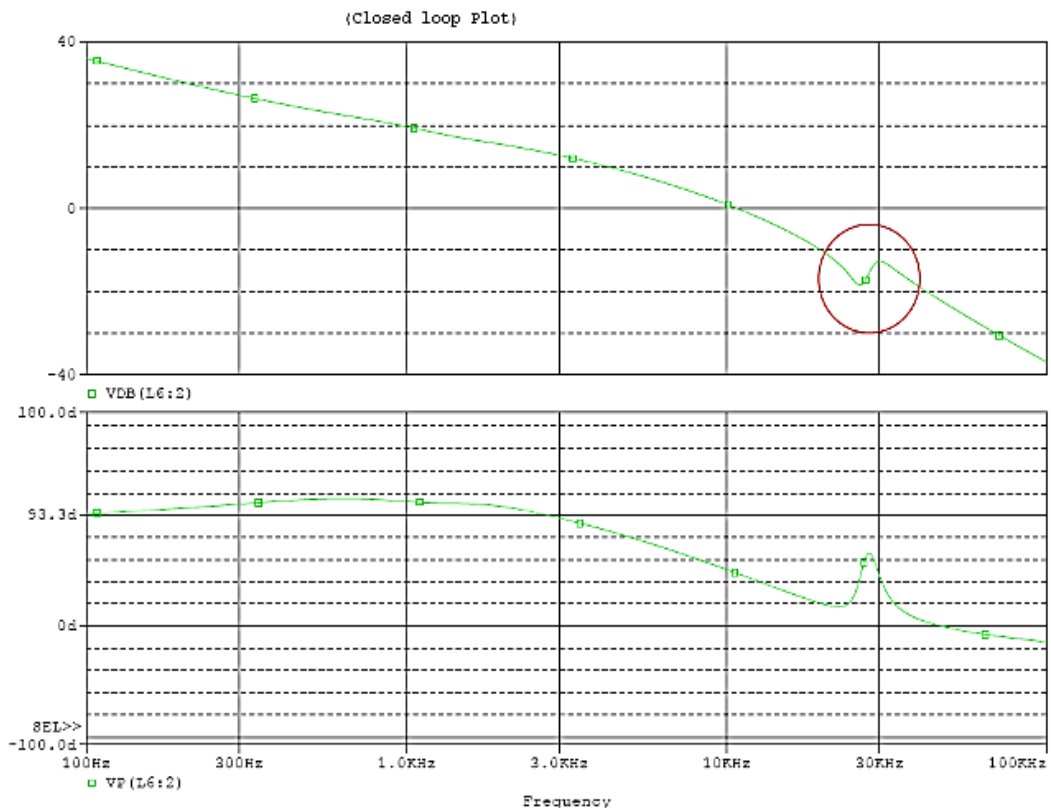


Figure 7. Closed-loop frequency response

### 3. EXPERIMENTAL RESULTS

Every DC-DC converter needs to have appropriate regulation for proper functioning [24]. To illustrate the proposed multiphase buck converter's transient behavior, the system has been designed and built with the specification such as 9 V, 12 A, 200 KHz. A prototype with two main converter power stages and a single output capacitor was created and tested [25]. Figure 8 shows an experimental lab set-up made for the testing of two-phase multiphase buck converter. Figure 9 shows the PWM gate pulses to MOSFET switches in both stages of buck converters. Figure 10 shows the output pulses from the PWM controller and the output from the current transformer. To experimentally verify the ripple cancellation due to two-phases in the buck converter, checked ripple in a single-phase converter. A single-phase buck converter with a 500 mV output voltage ripple is shown in Figure 11. The output ripple voltage was lowered to 2 mV by using the proposed two-phase interleaved buck converter, as shown in Figure 12. Figure 13 exhibits the closed loop buck converter bode plot, which indicates that the desired bandwidth is 10 Kz with a phase margin of 85°, proving that the system is stable.

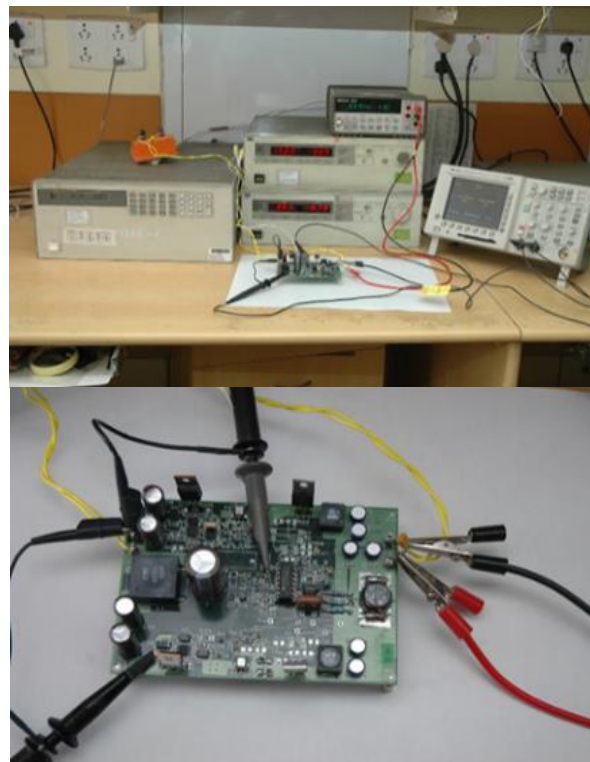


Figure 8. Experimental lab set up for two-phase buck converter

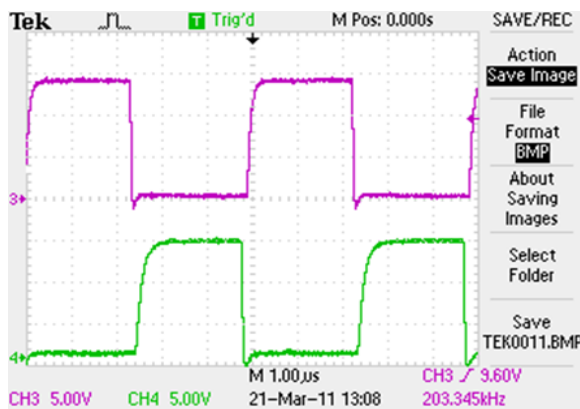


Figure 9. PWM gate pulses for two-phase converter

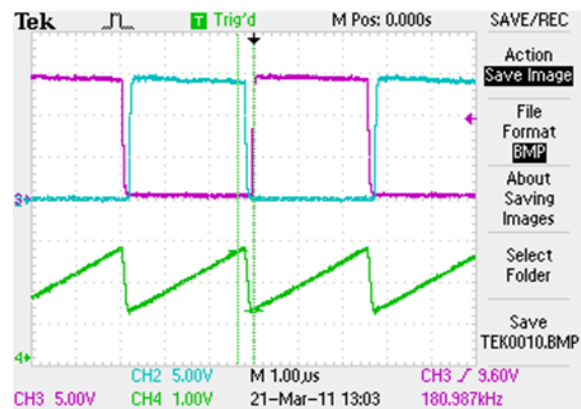


Figure 10. PWM output pulses and CT output



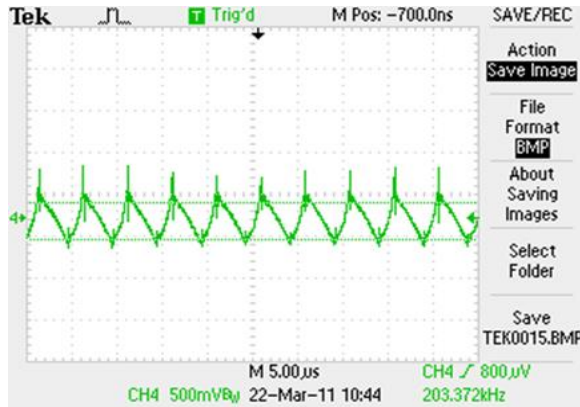


Figure 11. Output ripple of a single-phase converter

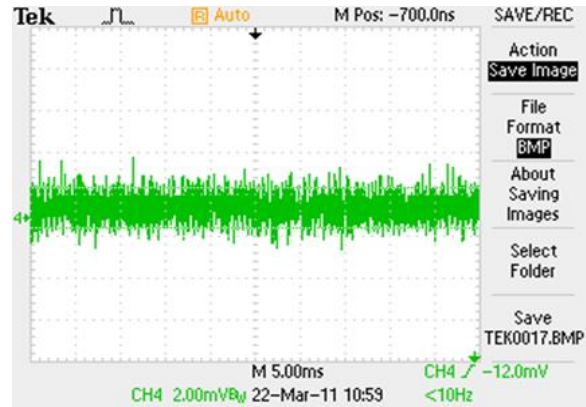


Figure 12. Output ripple from a multiphase converter

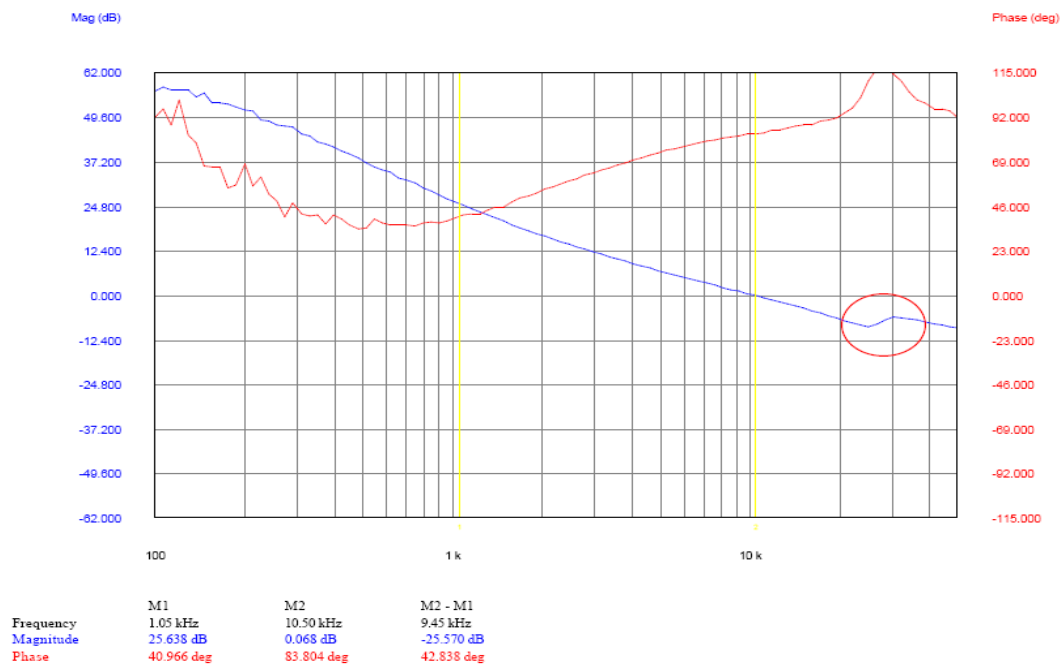


Figure 13. Closed-loop response of 30 V input 12 A output (multiphase)

#### 4. CONCLUSION

This paper demonstrates a multiphase buck converter and its time domain and frequency domain analysis. Converter circuit design is done as per specification and the designed circuit is first analyzed theoretically. The circuit was simulated in Orcad and the simulated results are validated by developing hardware. Reduction in ripple current at the output, which is due to the ripple cancellation effect, is proved from the hardware results. For a better comparison and to prove the results further, the ripple was measured from a single-phase converter and a two-phase converter separately. From the measured values, it is evident that the lowest ripple current belongs to a two-phase buck converter rather than a single phase, and the reduction is from 500 mV to 2 mV. The frequency response analyzer’s closed-loop analysis proves converter stability. The measured result reveals that the ripple voltage decreases to the lowest possible level. As a result, this converter has proven to be an excellent option for advanced microcontrollers.





#### REFERENCES

- [1] X. Zhou, P. L. Wong, P. Xu, F. C. Lee, and A. Q. Huang, “Investigation of candidate VRM topologies for future microprocessors,” *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 1172–1182, Nov. 2000, doi: 10.1109/63.892832.
- [2] J. Sun, Y. Qiu, M. Xu, and F. C. Lee, “High-frequency dynamic current sharing analyses for multiphase buck VRs,” *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2424–2431, Nov. 2007, doi: 10.1109/TPEL.2007.909303.




- [3] J. Gordillo and C. Aguilar, "A simple sensorless current sharing technique for multiphase DC–DC buck converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 3480–3489, 2016, doi: 10.1109/TPEL.2016.2592240.
- [4] N. M. Radaydeh and M. R. D. Al-Mothafar, "Small-signal modeling of current-mode controlled modular DC-DC converters using the state-space algebraic approach," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 10, no. 1, pp. 139–150, 2020, doi: 10.11591/ijece.v10i1.pp139-150.
- [5] R. G. Retegui, M. Benedetti, M. Funes, P. Antoszczuk, and D. Carrica, "Current control for high-dynamic high-power multiphase buck converters," *IEEE transactions on power electronics*, vol. 27, no. 2, pp. 614–618, 2011, doi: 10.1109/TPEL.2011.2158658.
- [6] O. Garcia, P. Zumel, A. De Castro, and A. Cobos, "Automotive DC-DC bidirectional converter made with many interleaved buck stages," *IEEE Transactions on Power Electronics*, vol. 21, no. 3, pp. 578–586, 2006, doi: 10.1109/TPEL.2006.872379.
- [7] P. Cervellini, P. Antoszczuk, R. G. Retegui, and M. Funes, "Current ripple amplitude measurement in multiphase power converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 6684–6688, 2017, doi: 10.1109/TPEL.2017.2686784.
- [8] M. Singh and A. Fayed, "Imbalanced high-current multi-phase buck converters for high-performance CPUs," in *2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2019, pp. 929–932, doi: 10.1109/MWSCAS.2019.8885141.
- [9] O. Garcia, P. Zumel, A. De Castro, and J. A. Cobos, "Effect of the tolerances in multi-phase dc-dc converters," in *2005 IEEE 36th Power Electronics Specialists Conference*, 2005, pp. 1452–1457, doi: 10.1109/PESC.2005.1581821.
- [10] Z. Lukic, S. M. Ahsanuzzaman, and A. Prodic, "Self-tuning sensorless digital current-mode controller with accurate current sharing for multiphase dc-dc converters," United States patent application US 12/498, 132, 2010.
- [11] O. Garcia, P. Zumel, A. de Castro, P. Alou, and J. A. Cobos, "Current self-balance mechanism in multiphase buck converter," *IEEE Transactions on Power Electronics*, vol. 24, no. 6, pp. 1600–1606, 2009, doi: 10.1109/PESC.2008.4591999.
- [12] Z. Wang and H. Li, "Three-phase bidirectional DC-DC converter with enhanced current sharing capability," in *2010 IEEE Energy Conversion Congress and Exposition*, 2010, pp. 1116–1122, doi: 10.1109/ECCE.2010.5617850.
- [13] M. Schuck and R. C. N. Pilawa-Podgurski, "Ripple minimization through harmonic elimination in asymmetric interleaved multiphase DC–DC converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 7202–7214, 2015, doi: 10.1109/TPEL.2015.2393812.
- [14] H. Liu, D. Zhang, and D. Wang, "Design considerations for output capacitance under inductance mismatches in multiphase buck converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5004–5015, 2016, doi: 10.1109/TPEL.2016.2605700.
- [15] M. P. Varghese, A. Manjunatha, and C. N. Raghu, "An inventive approach of stability for voltage regulator modules with high frequency multiphase buck converters," in *2012 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, 2012, pp. 1–6, doi: 10.1109/PEDES.2012.6484260.
- [16] D. Golovakha and R. Kasper, "Optimization of a multiphase interleaved buck converter based on electromagnetic processes in its elements," in *2018 IEEE International Telecommunications Energy Conference (INTELEC)*, 2018, pp. 1–8, doi: 10.1109/INTLEC.2018.8612321.
- [17] M. Ishwarya and R. Dhanalakshmi, "Investigations on multiphase modified interleaved buck converters for high step down voltage," in *2017 International Conference on Innovative Mechanisms for Industry Applications (ICIMIA)*, 2017, pp. 491–496, doi: 10.1109/ICIMIA.2017.7975663.
- [18] M. S. Vemuri and U. R. Tida, "Design and optimization of magnetic-core solenoid inductor for multi-phase buck converter," in *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2020, pp. 933–936, doi: 10.1109/MWSCAS48704.2020.9184471.
- [19] W. Hu, R. Yang, X. Wang, and F. Zhang, "Stability analysis of voltage controlled buck converter feed from a periodic input," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 4, pp. 3079–3089, 2020, doi: 10.1109/TIE.2020.2982116.
- [20] W. J. Gil-Gonzalez, O. D. Montoya, A. Garces, F. M. Serra, and G. Magaldi, "Output voltage regulation for dc-dc buck converters: a passivity-based PI design," in *2019 IEEE 10th Latin American Symposium on Circuits & Systems (LASCAS)*, 2019, pp. 189–192, doi: 10.1109/LASCAS.2019.8667557.
- [21] K. Hu, Y. Chen, and C. Tsai, "A digital multiphase converter with sensor-less current and thermal balance mechanism," in *2018 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2018, pp. 175–178, doi: 10.1109/ASSCC.2018.8579301.
- [22] K. Wu *et al.*, "A new multiphase buck converter with optimum-damping-control and current-balanced techniques," in *2017 International Conference on Applied System Innovation (ICASI)*, 2017, pp. 1320–1323, doi: 10.1109/ICASI.2017.7988146.
- [23] O. A. Trujillo, N. Toro-García, and F. E. Hoyos, "PID controller using rapid control prototyping techniques," *International Journal of Electrical and Computer Engineering*, vol. 9, no. 3, pp. 1645–1655, 2019, doi: 10.11591/ijece.v9i3.pp1645-1655.
- [24] D. Schweiner and M. Maliakova, "Transient analysis of buck DC-DC converter switching," in *2019 IEEE International Conference on Modern Electrical and Energy Systems (MEES)*, 2019, pp. 302–305, doi: 10.1109/MEES.2019.8896679.
- [25] V. Švikovic, J. Cortes, P. Alou, J. A. Oliver, O. García, and J. A. Cobos, "Multiphase current controlled buck converter with energy recycling output impedance correction circuit (OICC): adaptive voltage positioning (AVP) and dynamic voltage scaling (DVS) application," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 2877–2884, doi: 10.1109/APEC.2015.7104759.

## BIOGRAPHIES OF AUTHORS






**Mini Puthenpurakkal Varghese**     received AMIE in Electronics and communication engineering from the Institution of Engineers India in 2005 and M. tech in Computer applications in industrial drives from MS Ramaiah Institute of Technology, Bangalore, India, in 2011. She joined the Department of Electrical and Electronics Engineering, Sri Krishna Institute of Engineering Technology, Bangalore in 2011 and currently working as an assistant professor. Her research interests include switched-mode power supplies, design and testing of power converters. She can be contacted at email: mini.jinan@gmail.com.



**Ashwathnarayana Manjunatha**    did his BE from Mysore University in 1984, ME in Power Systems from Bangalore University in 1992. PhD in power system from Dr. M.G.R Deemed University Chennai during 2011. He is currently working as Principal at Sri Krishna institute of technology, Bangalore, Karnataka. His research areas of interest are power quality, power system, renewable energy. Published 20 international and national journals, 28 international and national conferences. He is a life member of the Indian Society for Technical Education also a member of the Institute of Engineers (India). He can be contacted at email: manjuprinci@gmail.com.



**Thazhathu Veedu Snehaprabha**    received her bachelor's degree -BSc Engg from NSS college of engineering, Calicut University, Kerala and master's degree -ME in Power systems from UVCE, Bangalore. She did her Ph.D. in Power electronics and Electrical Drives from JNTUH Hyderabad. She got 39 years of teaching experience. She currently holds the position of Director, Dept. student affairs at Presidency University, Bangalore. Her main research interests include Power Electronics and Electrical drives, Electric Vehicles. She has published many national and international journals, also presented papers in many conferences. She can be contacted at email: snehaprabha07@gmail.com.