International Journal of Electrical and Computer Engineering (IJECE)
Vol. 12, No. 4, August 2022, pp. 3477~3484
ISSN: 2088-8708, DOI: 10.11591/ijece.v12i4.pp3477-3484

Analysis and simulation of even-level quasi-Z-source inverter

Niltala Sai Shanmukha Akshath[1], Avugaddi Naresh[1], Matcha Nikesh kumar[1], Mayur Barman[1], Durgesh Nandan[2], Tripuathi Abhilash[3]
[1]Department of Electrical and Electronics Engineering, Aditya Engineering College, Surampalem, India
[2]Department of Electronics and Telecommunication, Symbiosis Institute of Technology, Symbiosis International (Deemed University), Pune, India
[3]Accendere Knowledge Management Services Pvt. Ltd., CL Educate Ltd., New Delhi, India

Article Info

Article history:

Received Feb 19, 2021
Revised Mar 16, 2022
Accepted Mar 29, 2022

Keywords:

Duty cycle
Harmonic spectra
Multilevel inverter
Quasi Z-source
Seven-level

ABSTRACT

This research proposes a seven-level inverter with quasi-Z-source boost converters. The proposed topology employs a packed U-cell asymmetrical type multilevel inverter along with front-end quasi-Z-source networks. The quasi networks provide high gain compared to a conventional boost converter. This topology is the most suitable for photovoltaic multi-string applications. The proposed topology has the potential to supply both the alternating current (AC) and direct current (DC) type load. The inverter structure has a lower number of active switches which helps in the reduction of losses and improvement in efficiency. In this paper, the operation principle of a quasi-network and inverter circuit are explained in detail. In addition, the simulation results for various modulation indices are presented. In the MATLAB/Simulink environment, the architecture is proposed by using gated sinusoidal "Pulse width modulation".

Corresponding Author:

Tirupathi Abhilash
Accendere Knowledge Management Services Pvt. Ltd., CL Educate Ltd.
New Delhi, India
Email: abhilash.tripuathi@accendere.co.in

1. INTRODUCTION

Latest developments have seen considerable rise in the utilization of Z-sources based converters in possible solutions such as environmentally ecofriendly fuel cell-based generations/photovoltaic (PV) to fulfil expanding energy demands, flexible alternating current (AC) transmission systems (FACTs), energy storage, electric and electric vehicles as well as in wind energy conversions [1]. In comparison by the direct current (DC-DC) two-stage conversions, the effectiveness of single-stage conversion improves as a result of this. The Z-source inverters (ZSI) alleviate the failure of outdated current source inverters and voltage supply by using a network of two inductors and two condensers in the shape of a Z [2]. This impedance network introduction eliminates inverters failure due to the lack of dead band in the absence of the leg switches and thus reduces the waveform distance. By changing the duty cycle D0, the output voltage is controlled phase switches or all phases to be activated over the cycle duration.

A review of various strategies is presented [3]. To achieve the appropriate output tension, traditional pulse-width modulation (PWM) methods are modified to include a zero-status shoot-through without changing the active circumstances. The optimal positioning of the screw is, however, obligatory as it takes a prominent place in the evaluation of the current ripple, number of switch switches, minimization of switching loss and softness. In this aspect, a new control system [4] is investigated, which uses zero voltage switching (ZVS) to effectively reduce commutations for simple control and enhanced efficiency. A better control system is being investigated in the same area [5]. Both legs are used to shoot, reducing the current stress

between the switches. The higher as well as lower frequencies of the switch's fs and 2fs are different, which increases the loss. The technique is modified in this paper to allow all switches to operate at the same frequency (s) to reduce the loss of switching. In comparison to ZSIs, the benefits of constant input current, reduced capacitor voltage stress, and smaller C2 make quasi Zsource inverters (qZSI) highly attractive for renewable applications. Multi-level inverters (MLIs) for low-power applications have recently gained the benefits of low dv/dt, minimal button stress, improved voltage and current profiles, and reduced filter size [6]. H-bridges in cascade (CHB), neutrally point clamped (NPC), and flying condensers are three prominent topologies utilized in industrial applications (FCs). CHB is the most suitable of these due to its adaptability, lack of clamping diodes, and lack of FC-voltage balance issues. Switch counts, condenser reduction, diodes, condenser equilibrium, simplicity of control, and the quantity of DC sources have all been studied in MLIs [7]. Although MLIs provide a number of advantages, one of the most significant drawbacks is the low output voltage gain. In order to achieve improved voltage control and output quality, MLIs must be properly upgraded with appropriate power conditioners [8]–[14]. The power conditioner for MLI integration is a Z source-based converter.

The recent growth in the adoption of Z-Source converters has revolutionized renewable energy system including power electronic application, hybrid cars, uninterruptable power supplies, and distributed energy [15]. Inverter capitalizes on the problems that traditional current source and voltage source inverters [16]. This reduces wave form distortions and improves dependability. It reduces DC power consumption when combined with a buck-boost circuit, resulting in a more efficient single-stage. In order to maximize the amplitude of the shoot-through voltage, the service series is boosted by the output voltage. The beam-through can be obtained by turning on the switches for DT. The different methods for shoot-through control are described in the literature [17], [18]. In general, the Z-source converters are more common with conversions from DC to alternating current (AC) as well as AC to DC. Because of the numerous Z-sources topologies [19]–[22], most systems use quasi-Z inverters, which minimize the capacitor size, thus offering continuous input current, as well as having DC input, but are not common-rail devices.

In contrast, a multi-level inverter (MLI) delivers better voltage and current with lower total harmonics distortion (THD), which reduces switching losses and increases efficiency. A number of more advanced MLI topologies, including neutral point (NP) capacitor, switch count (SC) capacitor, and the cascaded chronic myeloid leukemia blast crisis (CML BC), have been employed in order to resolve the issues of switching, capacitor voltage balancing, and the difficulty of managing complexity [23]. For another important effort, MLI is also being made to comply with lower voltage distributed energy sources, which means the biggest issue with MLI is low output voltage gain, however [24], [25].

Higher voltage gains and seven-level AC output with fewer switching devices, fewer DC power supply, as well as minimum off state voltages pressure acrossed the converting device are all advantages of the proposed converter. The rest of the manuscript is laid out: under second subpart of paper explain proposed approach of inverter and operating modes, under third subpart of paper explains the modulation principle used to generate the required output voltage waveform, under fourth subpart of paper shows how the new converter design which proposed by author is validated using simulation results for various modulation indices, and section 5 finally concludes all pros and corn of this research.

2. PROPOSED INVERTER

Figure 1 represents the developed quasi of Z-source single phase seven levels created MLI using a packed u-cell structure. The z-source network is formed by the elements called inductors, diodes capacitors and an active switch. The inverter circuit consists of 6 active switching devices with bi-directional conducting capability. Impact of anti-parallel diodes, the switching device has bi-directional leading capability but only block voltages in uni-directional. In the suggested topology, three different DC source can be generated after batteries bank, PV system, or rectifiers circuits. The major contribution of this paper is the cascaded connection of packed U-cell (PUC) inverter to the quasi-Z-source. This cascaded connection gives the higher output voltage, better performance and improved harmonic profile which is shown with the simulation results.

Figures 2(a) and 2(b) represent the switching conditions through negative along with positive zeroes crossings of the output voltage. $V0=0^{+}$ is the positive zero-crossing through the output voltage. $V0=0^{-}$ is the negative zero-crossing at output voltage. To keep the temperature escalation in entire switches at the same level, both switching states are used equally.

Figure 3 shows the recommended converter, which operates to create a positive level voltage transversely the output terminal. Figure 3(a) generated V0=V1, and the power semiconductor devices insulated gate bipolar transistors (IGBTs) S5, S7, and S10 operate in this manner. As illustrated in, the

IGBTs S6, S7, and S9 operate in this manner Figure 3(b). The peak voltage of V0=V1+V2 is shown in Figure 3(c), and the IGBTs S5, S7, and S9 conducted in these operating modes.

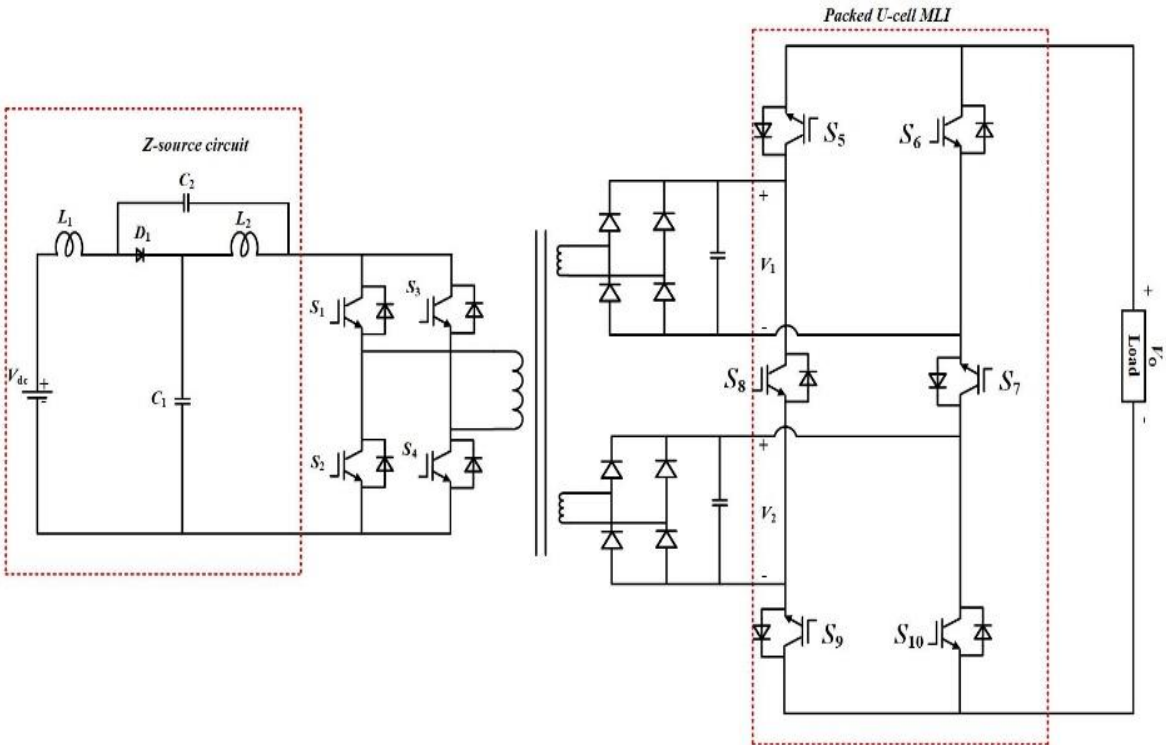


Figure 1. Proposed Z-source inverter the schematic circuit diagram

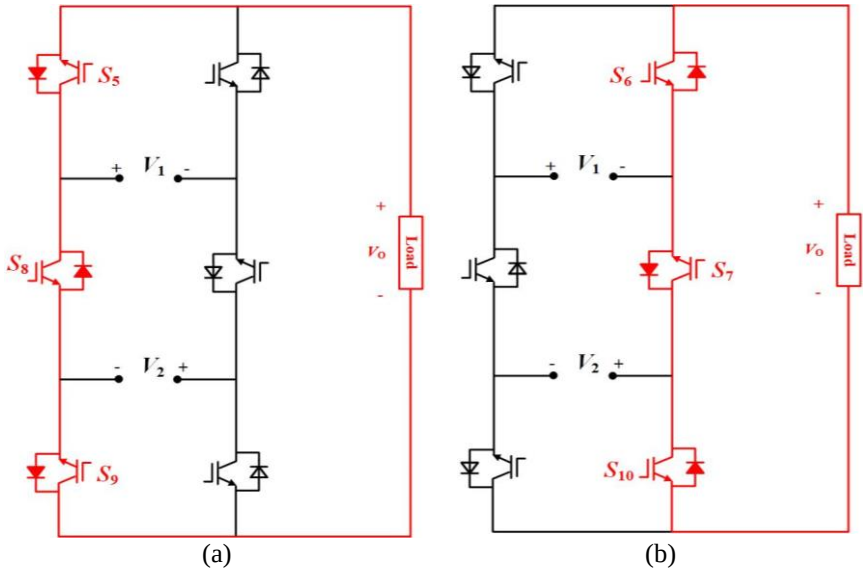
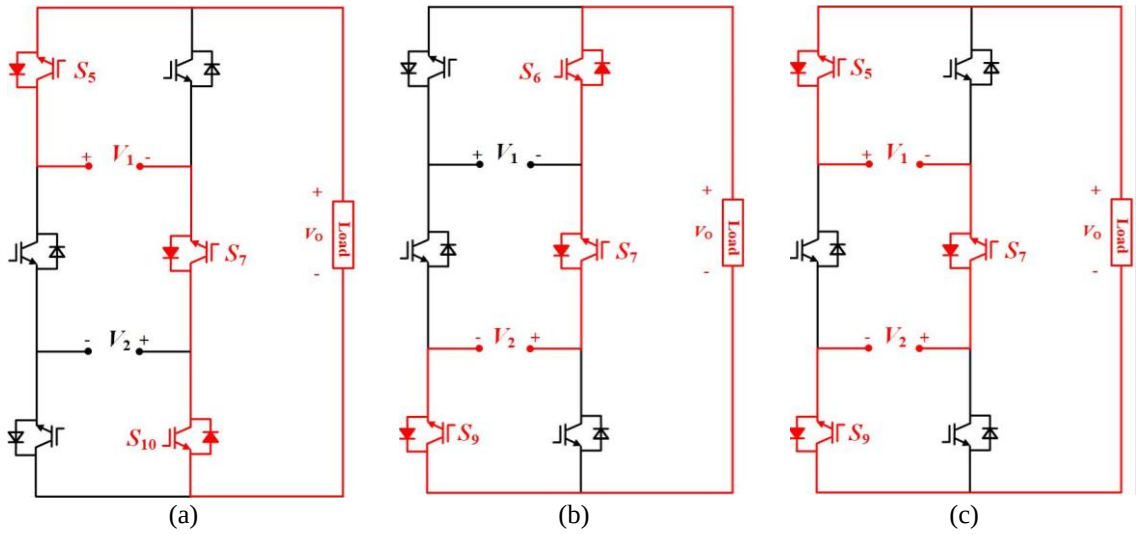


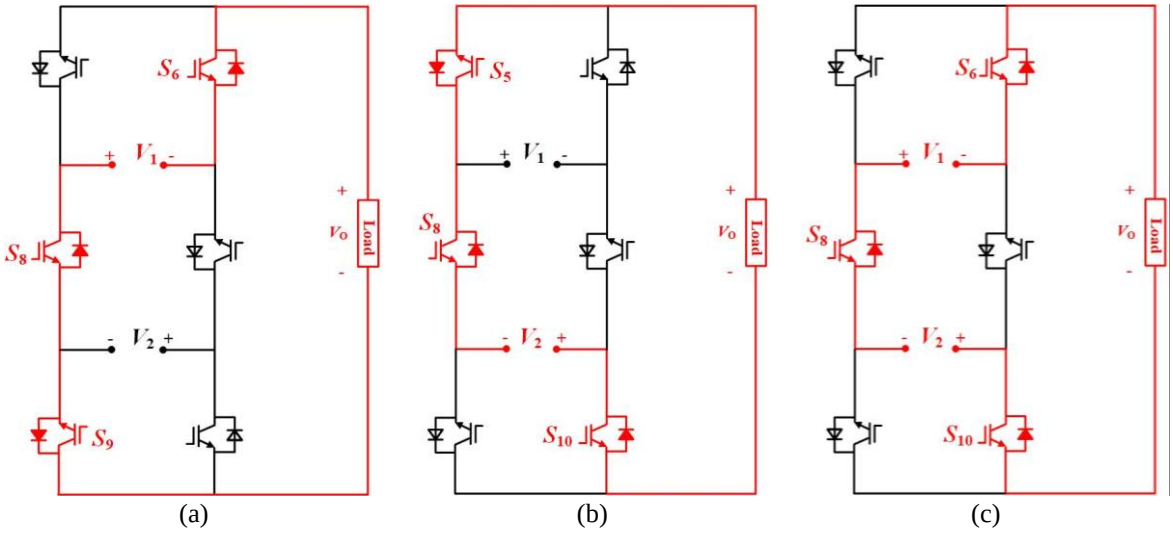
Figure 2. Zero switching states: (a) V_0=0$^+$ and (b) V_0=0$^-$

Figure 4 depicts the converter's employed mode for producing negative output voltage levels. V0=-V1 is generated in Figure 4(a), and the IGBTs S6, S8, and S9 turn on in this operating mode. The output voltage V0=-V2 is shown in Figure 4(b), and the IGBTs S5, S8, and S10 turn on during this time. The output voltage VL=-(V1+V2) is shown in Figure 4(c), and the IGBTs S6, S8, and S10 are turned on at this time.



(a) (b) (c)

Figure 3. Positive switching states (a) $V_0=V_1$, (b) $V_0=V_2$, and (c) $V_0=V_1+V_2$



(a) (b) (c)

Figure 4. Negative switching states (a) $V_L=-V_{dc}/2$, (b) VL=-3 Vdc/2, and (c) VL=-2 Vdc

3. METHOD

3.1. Modulation technique

Table 1 shows the off and on conditions of the switching devices in the planned convertors on various output voltage value to help understand the switching states. The numerals 1 and 0 in Table 1 represent the off and on state of the IGBT in the Figure 1 based results. Lower switching frequencies appear to be used by switches S7 and S8, resulting in lower switching losses. In the designed architecture, the modulation technique working for generation of gate pulse to the IGBT is depicted in Figure 5. A sine wave is placed over six trilateral waveforms. The carrier waveform is known by way of the triangle waves, whereas the reference waveform is known as the sinusoidal waves shown configuration constraints in Table 2. Respectively carrier waveform interrelates with the reference waveform at certain intermissions, as specified by the digits 1, 2, 3, 1', 2', and 3'. As a result of these connections among the carrier waves and reference, the Produced pulsations are N1-N3 and P1-P3. These pulsations are successfully used in logical gate circuit uses to produce the mandatory output voltages of seven-level. The modulation index (M.I.) regulates the amount of output stages that is explained using (1).

$$M.I.=\frac{V_{0peak}}{3\times V_{dc}} \quad (1)$$

Table 1. Switching sequences of inverter

Output Voltage Level (V_0)	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
V_1+V_2	0	0	0	0	1	0	1	0	1	0
V_2	0	0	0	0	0	1	1	0	1	0
V_1	0	0	0	0	1	0	1	0	0	1
0^+	0	0	0	0	1	0	0	1	1	0
0^-	0	0	0	0	0	1	1	0	0	1
$-V_1$	0	0	0	0	0	1	0	1	1	0
$-V_2$	0	0	0	0	1	0	0	1	0	1
$-(V_1+V_2)$	0	0	0	0	0	1	0	1	0	1

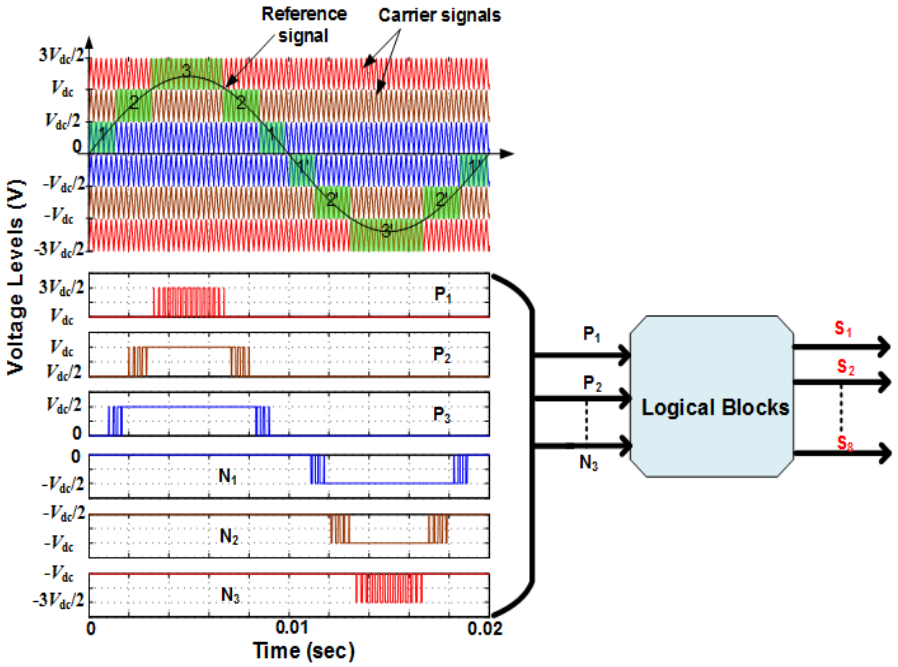


Figure 5. Sin-triangle evaluation of PWM system

Table 2. Configuration constraints

Parameters	Values
"V_{dc} (V)"	240 V
"P_{output} (W)"	730
"V_0 (V)"	230
"I_0 (A)"	3.5
"Switching frequency (f_{sw})"	4 kHz
"Fundamental frequency (f_m)"	50 Hz

4. RESULTS AND DISCUSSION

To demonstrate its performance, the proposed configuration is evaluated in a MATLAB simulation. The simulation settings are adjusted to 230 V and 50 Hz for a single-phase output voltage. Figure 6(a) shows that currents waveforms and the inverter output voltage intended for an M.I. of 0.6 and 0.9 respectively. Figure 6(a) depicts a corresponding current and the 9-level output voltage waveforms. Figure 6(b) depicts a seven-level output voltage waveforms and the comparable load currents. Lowering M.I. lowers the output voltage's peak value, which is self-evident (V0 peak). For various values of M.I., the fast Fourier transform spectrum of the inverter's output voltages is revealed in Figure 7(a) as well as Figure 7(b). V0 peak is seen to be 361 V, at the condition of the inverter is modulation value is 0.9 and the THD is 16.6%. As demonstrated in, a M.I. is invertional proportional of THD as a result of a decreasing in the amount of output voltage level.

Figures 8(a) and 8(b) represented the harmonic spectrum of the output current waveform. The rate of I0 peak is 6.4 A at an inflection of 0.9, and the THD is about 0.5%. The I0 peak value reduces in the same way as the voltage decreases when the MI decreases. The THD is coarsely 0.6%, besides the I0 peak value is 5 A.

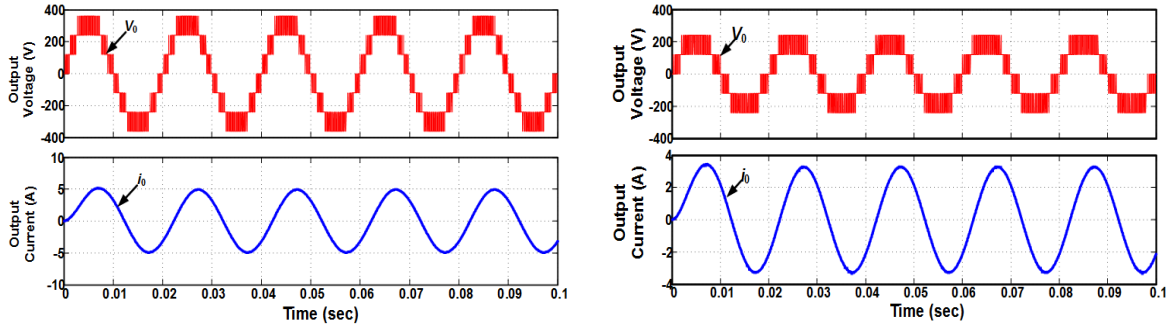


Figure 6. MATLAB based results at (a) *MI=0.9* and (b) *MI=0.6*

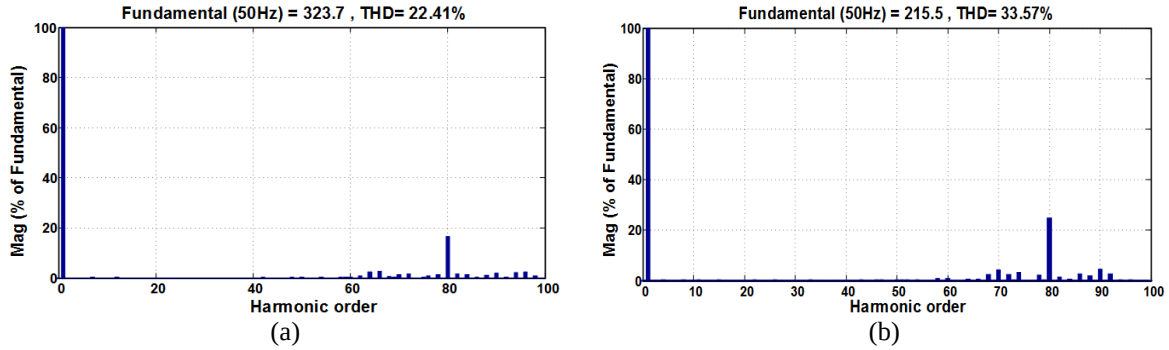


Figure 7. Fast Fourier transform analysis of (a) V_0 for (MI=0.9) and (b) V_0 for (MI=0.6)

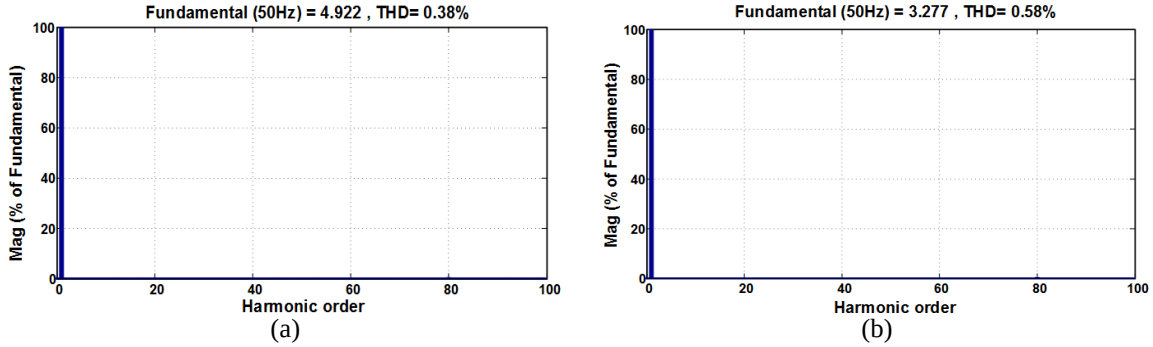


Figure 8. Fast Fourier transform analysis of (a) I_0 for (MI=0.9) and (b) I_0 for (MI=0.6)

5. CONCLUSION

Presented research work gives a comprehensive investigation of the seven-level operational methods of the proposed quasi-Z-sources constructed multi-level inverter (MLI) with a concentrated constituent amount. The proposed network topology is a two-stage circuit that provides independent control of the output variables. The modulation technique for generating inverter switch firing pulses has been refined. The simulation results are shown for a variety of M.I. values and power ratings. The output parameters were subjected to a fast fourier transform (FFT) analysis, and the percent THD of the current waveforms was found to be within the IEEE 1547 grid standard's restrictions.

REFERENCES

[1] N. Moghadasi, A. Esmaeli, S. Soleymani, and B. Mozafari, "Quasi-Z-source matrix converters to be used in PMSG-based WECS: Modeling, control, and comparison," *International Transactions on Electrical Energy Systems*, vol. 28, no. 6, Jun. 2018, doi: 10.1002/etep.2544.

[2] F. Z. Peng, "Z-source inverters," in *Wiley Encyclopedia of Electrical and Electronics Engineering*, Hoboken, NJ, USA: John Wiley & Sons, Inc., 2017, pp. 1–11.
[3] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, G. E. Town, and S. Yang, "Impedance-source networks for electric power conversion part II: review of control and modulation techniques," *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 1887–1906, Apr. 2015, doi: 10.1109/TPEL.2014.2329859.
[4] S.-C. Wang, Y.-H. Liu, Y.-S. Cheng, and B.-R. Peng, "A novel modulation technique with interleaved-and-shifted shoot-through state placement for quasi-Z-source inverters," *International Journal of Circuit Theory and Applications*, vol. 46, no. 2, pp. 343–363, Feb. 2018, doi: 10.1002/cta.2390.
[5] Y. P. Siwakoti and G. Town, "Improved modulation technique for voltage fed quasi-Z-source DC/DC converter," in *2014 IEEE Applied Power Electronics Conference and Exposition-APEC 2014*, Mar. 2014, pp. 1973–1978, doi: 10.1109/APEC.2014.6803577.
[6] J. Anderson and F. Z. Peng, "Four quasi-Z-source inverters," in *2008 IEEE Power Electronics Specialists Conference*, Jun. 2008, pp. 2743–2749, doi: 10.1109/PESC.2008.4592360.
[7] B. Ge, F. Z. Peng, and Y. Li, "Multilevel converter/inverter topologies and applications," in *Power Electronics for Renewable Energy Systems, Transportation and Industrial Applications*, Chichester, UK: John Wiley & Sons, Ltd, 2014, pp. 422–462.
[8] P. C. Loh, F. Gao, F. Blaabjerg, S. Y. C. Feng, and K. N. J. Soon, "Pulsewidth-modulated Z-source neutral-point-clamped inverter," *IEEE Transactions on Industry Applications*, vol. 43, no. 5, pp. 1295–1308, 2007, doi: 10.1109/TIA.2007.904422.
[9] P. C. Loh, S. W. Lim, F. Gao, and F. Blaabjerg, "Three-level Z-source inverters using a single LC impedance network," *IEEE Transactions on Power Electronics*, vol. 22, no. 2, pp. 706–711, Mar. 2007, doi: 10.1109/TPEL.2007.892433.
[10] F. Gao, P. C. Loh, F. Blaabjerg, and R. Teodorescu, "Modulation schemes of multi-phase three-level Z-source inverters," in *2007 IEEE Power Electronics Specialists Conference*, 2007, pp. 1905–1911, doi: 10.1109/PESC.2007.4342293.
[11] R. Strzelecki, M. Adamowicz, and D. Wojciechowski, "Buck-boost inverters with symmetrical passive four-terminal networks," in *2007 Compatibility in Power Electronics*, May 2007, pp. 1–9, doi: 10.1109/CPE.2007.4296565.
[12] T. Li and Q. Cheng, "Structure analysis and sliding mode control of new dual quasi-Z-source inverter in microgrid," *International Transactions on Electrical Energy Systems*, vol. 29, no. 1, Jan. 2019, doi: 10.1002/etep.2662.
[13] O. Husev, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov, and S. Stepenko, "Single phase three-level neutral-point-clamped quasi-Z-source inverter," *IET Power Electronics*, vol. 8, no. 1, pp. 1–10, Jan. 2015, doi: 10.1049/iet-pel.2013.0904.
[14] W. Mo, P. C. Loh, D. Li, and F. Blaabjerg, "Trans-Z-source neutral point clamped inverter," in *6th IET International Conference on Power Electronics, Machines and Drives (PEMD 2012)*, 2012, pp. A112–A112, doi: 10.1049/cp.2012.0236.
[15] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, and G. E. Town, "Impedance-source networks for electric power conversion part I: A topological review," *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 699–716, Feb. 2015, doi: 10.1109/TPEL.2014.2313746.
[16] F. Z. Peng, "Z-source inverter," *IEEE Transactions on Industry Applications*, vol. 39, no. 2, pp. 504–510, Mar. 2003, doi: 10.1109/TIA.2003.808920.
[17] F. Z. Peng, "Z-source networks for power conversion," in *2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition*, Feb. 2008, pp. 1258–1265, doi: 10.1109/APEC.2008.4522884.
[18] P. C. Loh, D. M. Vilathgamuwa, Y. S. Lai, G. T. Chua, and Y. Li, "Pulse-width modulation of Z-source inverters," *IEEE Transactions on Power Electronics*, vol. 20, no. 6, pp. 1346–1355, Nov. 2005, doi: 10.1109/TPEL.2005.857543.
[19] M.-K. Nguyen, Y.-C. Lim, and Y.-G. Kim, "TZ-source inverters," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 12, pp. 5686–5695, Dec. 2013, doi: 10.1109/TIE.2012.2229678.
[20] P. C. Loh, F. Gao, and F. Blaabjerg, "Embedded EZ-source inverters," *IEEE Transactions on Industry Applications*, vol. 46, no. 1, pp. 256–267, 2010, doi: 10.1109/TIA.2009.2036508.
[21] W. Mo, P. C. Loh, and F. Blaabjerg, "Asymmetrical Γ-Source Inverters," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 2, pp. 637–647, Feb. 2014, doi: 10.1109/TIE.2013.2253066.
[22] A. Tirupathi, K. Annamalai, and S. Veeramraju Tirumala, "A new structure of three-phase five-level inverter with nested two-level cells," *International Journal of Circuit Theory and Applications*, vol. 47, no. 9, pp. 1435–1445, Sep. 2019, doi: 10.1002/cta.2648.
[23] A. Tirupathi, K. Annamalai, and S. Veeramraju Tirumala, "A new hybrid flying capacitor-based single-phase nine-level inverter," *International Transactions on Electrical Energy Systems*, vol. 29, no. 12, Dec. 2019, doi: 10.1002/2050-7038.12139.
[24] L. S. H. Priya, K. Rajesh, U. Satya Sai Polaraju, and N. Rajesh, "Simulation and analysis of seven-level voltage source inverter," in *Advances in Intelligent Systems and Computing*, Springer Singapore, 2021, pp. 111–120.
[25] S. R. Pulikanti, G. Konstantinou, and V. G. Agelidis, "Hybrid seven-level cascaded active neutral-point-clamped-based multilevel converter under SHE-PWM," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 11, pp. 4794–4804, Nov. 2013, doi: 10.1109/TIE.2012.2218551.

BIOGRAPHIES OF AUTHORS

Niltala Sai shanmukha Akshath is U. G. student of the B. Tech. program in electrical and electronic engineering branch from Aditya Engineering College, Surrampalem, East Godavari District, Andhra Pradesh, India. His research interests include renewable energy, and power electronics. He can be contacted at email: 18a91a0233@aec.edu.in.

Avugaddi Naresh is U. G. student of the B. Tech. program in electrical and electronic engineering branch from Aditya Engineering College, Surrampalem, East Godavari District, Andhra Pradesh, India. His research interests include renewable energy, and power electronics. He can be contacted at email: 18a91a0202@aec.edu.in.

Matcha Nikesh kumar is U. G. student of the B. Tech. program in electrical and electronic engineering branch from Aditya Engineering College, Surrampalem, East Godavari District, Andhra Pradesh, India. His research interests include renewable energy, and power electronics. He can be contacted at email: 19a95a0214@aec.edu.in.

Mayur Barman received the M. Tech degrees in electrical engineering from Tezpur University, Assam, India, and the Ph.D. degree in electrical engineering from NIT Slicher, Assam, India 2019. He has been an Assistant professor of electrical and electronic engineering with Aditya Engineering College, since 2019. His research interests include to power system demand analysis, and Power electronics. He can be contacted at email: barman.mayur@yahoo.com.

Durgesh Nandan did his Doctor of Philosophy (Ph.D.) from Department of E.C.E., Jaypee University of Engineering and Technology, Guna, Madhya Pradesh, India in year 2018 with the specialization in VLSI. He found various prestigious awards like JSS fellowship, Young Personality of the Year Award (below 40 years)" and I2OR Preeminent Researcher Award 2019". He awarded IEEE senior membership in 2020. He is inventor/Co-inventor of 4 Indian patent. He is the author or a co-author of 2 books. His research interest's extent in number of areas like computer arithmetic, VLSI architecture for signal processing applications, Speech Processing, Hardware architecture of real time big data/AI applications, and Internet on Things. He can be contacted at email: durgeshnandano51@gmail.com.

Tripuathi Abhilash received the B. Tech. and M. Tech. degrees in electrical engineering in 2009 and 2012, respectively, and the Ph.D. degree in electrical engineering according from National Institute of Technology, Warangal, India, in 2020. He has been a Research Mentor of electrical engineering with AKMS, since 2020. He has authored or coauthored more than 20 refereed journal and conference papers. His research interests include the applications of power electronics, and control. He can be contacted at email: abhilash.tripuathi@accendere.co.in.