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Field-programmable gate array design of image encryption and decryption using Chua's chaotic masking

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ABSTRACT

This article presents a simple and efficient masking technique based on Chua chaotic system synchronization. It includes feeding the masked signal back to the master system and using it to drive the slave system for synchronization purposes. The proposed system is implemented in a field programmable gate array (FPGA) device using the Xilinx system generator tool. To achieve synchronization, the Pecora-Carroll identical cascading synchronization approach was used. The transmitted signal should be mixed or masked with a chaotic carrier and can be processed by the receiver without any distortion or loss. For different images, the security analysis is performed using the histogram, correlation coefficient, and entropy. In addition, FPGA hardware co-simulation based Xilinx Artix7 xc7a100t-1csg324 was used to check the reality of the encryption and decryption of the images.

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1. INTRODUCTION

Communication systems such as mobile and internet networks have increasingly developed in recent years, and the area of information transmission has been expanded. This region, however, faces additional challenges in the saving and exchange of media messages by means of illegal eavesdropping. Multimedia communications such as photographs and videos should also be encrypted to avoid unauthorized attacks to ensure secure transmission over the Internet. Traditional forms of encryption have some disadvantages in high stream data encryption and are less efficient in securing photos using encryption schemes. To guarantee secure Internet data transmission, images must be encrypted with high protection and low complexity in an efficient way [1]. The application of chaotic cryptographic to the security of images has been proposed as a way to resolve a variety of security issues, as chaotic systems have a number of advantages over random systems, including their sensitivity to initial conditions and parameter settings, and their aperiodic signal nature makes them an excellent choice for encryption systems [2].

This article contributed to the use of chaotic systems in the process of information security, rather than conventional methods of encryption, and the approach used was simpler, more effective, and produced good results as compared to other complex methods of image hiding such as. In the paper [3], a chaotic block image permutation and XOR operation are performed to achieve image encryption. The chaotic masking scheme based on embedded message synchronization is introduced in [4]. An effective and high security communication system based on two levels of encryption based on chaotic systems was proposed in [5]. Merah *et al.* [6] present a novel stream cipher based on chaotic synchronization. Suggest an image encryption model that combines chaotic maps such as logistic, sine, and tent chaotic systems [7].

Applying chaos to cryptography did not gain much attention until the discovery of chaotic synchronization, which contributed to a turning point in the application of chaos dynamics to information security. From Pecora and Carroll's work [8], a wide range of research efforts has focused on the study of chaos synchronization. It is applied in a variety of fields, including secure communication, biological systems, ecological systems, and physical systems [9]. Much attention was given to the control and synchronization of Chua systems by researchers. Chua system have recently been synchronized with active control [10], adaptive control [11], sliding control [12], fuzzy control [13], and backstepping control methods [14].

The digital implementation of this system on an field programmable gate array (FPGA) system is ideal because it eliminates part drift and has high power and throughput capability [15]. FPGAs are the primary tool for implementing high-performance systems, especially in image processing applications and digital signal processing systems. Additionally, FPGAs can perform signal processing at a high rate of efficiency [16]. The Xilinx system generator (XSG) extends the capabilities of the FPGA and offers important tools for developing image encryption models.

This paper is arranged as follows. In section 2, a Chua circuit design using XSG was illustrated; the concept of the Pecora-Carroll (PC) cascaded synchronization method and its implementation using XSG is given in section 3. In section 4, we explain the chaotic masking with feedback and the purpose of this procedure. In section 5, the FPGA platform of image encryption using chaotic masking with feedback is performed. Section 6 shows the randomness measures of the system proposed. The efficiency and security review of the proposed model is presented in section 7. Next, section 8, which co-simulates image encryption by FPGA hardware. Finally, section 9 presents the conclusion of this paper.

2. CHUA'S CIRCUIT DESIGN

The Circuit of Chua has a simple structure and easily generates chaotic dynamics with sufficient parameters. Thus, several researchers have been interested in this circuit. For the implementation of the chaotic system Chua, we use the Xilinx system generator (XSG) method in this section. The relevance of the Chua circuit has recently made possible the birth of a big family of multi-scroll oscillators and techniques to control the chaos [17]. Chua's circuit has found many applications in physics, communication, and control, mechanics, as well as chemistry, economics, and medicine [18]. Chua's circuit has also been used as a chaotic noise generator. Because of this property, it has found many applications in cryptography and steganography [19]. The as nonlinear (1), (2) describe this chaotic system:

$$\mathrm{X}^{\cdot} = \mathrm{A}\,(\mathrm{Y} - \mathrm{X} - \mathrm{F}(\mathrm{X})$$

$$\mathrm{y}^{\cdot} = \mathrm{x} - \mathrm{y} + \mathrm{z}$$

$$\mathrm{Z}^{\cdot} = -\mathrm{BY} \tag{1}$$

where $f(x)$

$$f\,(x) = m1x + 1/2(m0 - m1)\,(|x + b1| - |x - b1\,|) \tag{2}$$

where α and β are the parameters of the system and $f(x)$ piecewise linear (PWL) function, m_0 and m_1 are the negative slopes, and b1 is the breakpoint. Figure 1 shows XY phase portrait and 3D plot of the Chua attractor using fixed-point data format (Fix 32_16). The initial values x_0=-0.3, y_0= 0.1, and z_0= 0.2, and system parameters are α =9, β = 100/7, m_0=-3 and m_1 =-0.3, b1=0.1, with step size dt = 0.01**.**

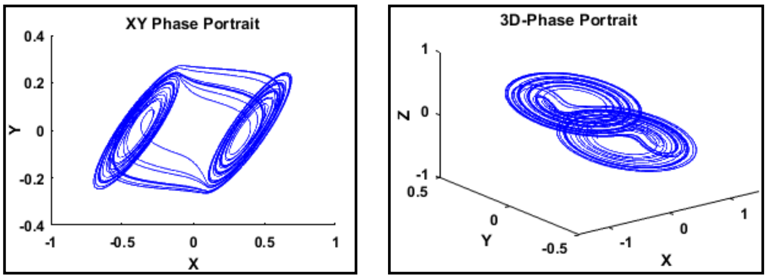


Figure 1. XY and XYZ phase portrait plot

3. PC CASCADED SYNCHRONIZATION OF CHUA'S CHAOTIC SYSTEM

This method describes the two systems with chaotic dynamics coupled to each other. One of them is the transmitter system, also called the drive (master) and the two receivers named the response (slave). The response subsystems used here are the YZ response subsystem and XZ response subsystems. The Chua cascaded synchronization system is implemented using the Xilinx system generator model shown in Figure 2.

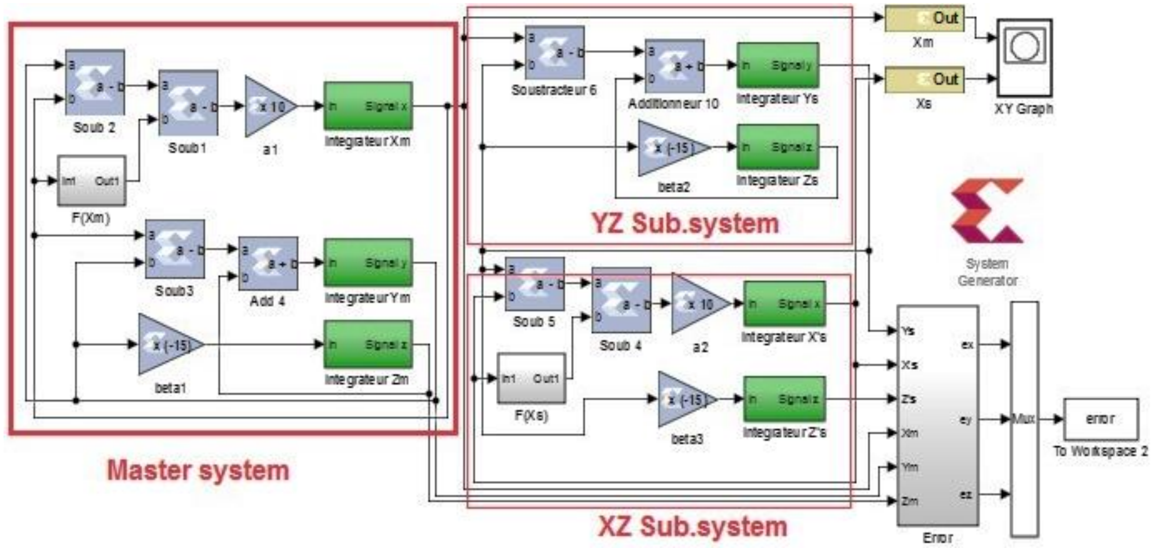


Figure 2. PC cascaded synchronization of chua system using XSG

The master as (3)

$$\begin{aligned} xm^{\cdot} &= \alpha\,(ym - xm - f\,(x)) \\ ym^{\cdot} &= xm - ym + zm \\ zm^{\cdot} &= -\beta ym \end{aligned} \tag{3}$$

YZ response subsystem (4)

$$\begin{aligned} ys^{\cdot} &= xm - ys + zs \\ zs^{\cdot} &= -\beta ys \end{aligned} \tag{4}$$

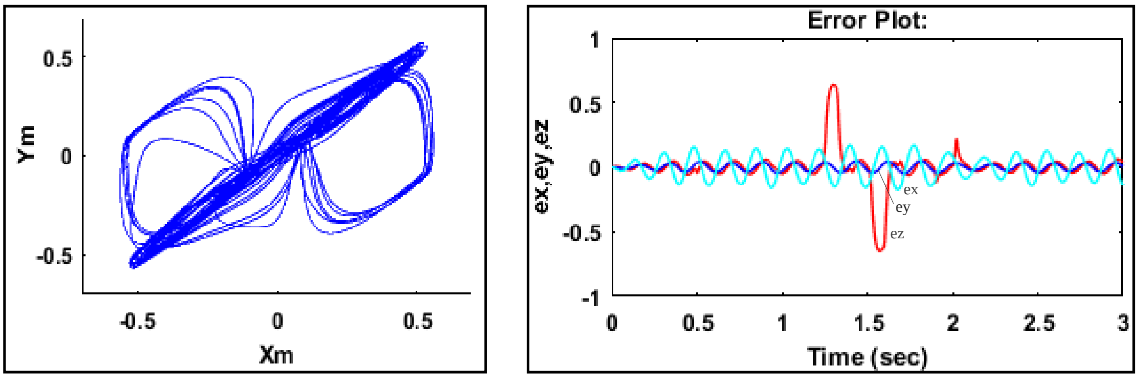
XZ response subsystem (5)

$$\begin{aligned} x's^{\cdot} &= \alpha\,(ys - x's - f\,(x')) \\ z's^{\cdot} &= -\beta ys \end{aligned} \tag{5}$$

The differences between master and slave are known as the synchronizing errors and the errors must converge to zero when the synchronization occurs.

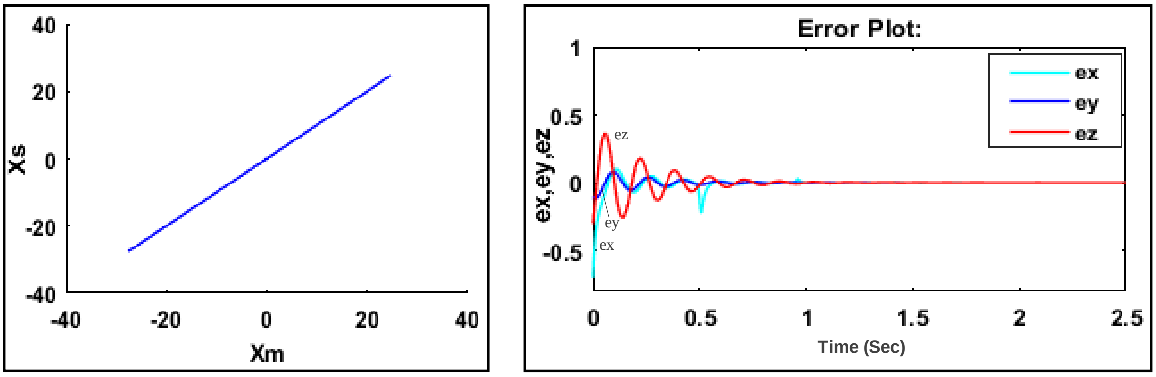
$$\begin{aligned} ex &= x's - xm \\ ey &= ys - ym \\ ez &= z's - zm \end{aligned} \tag{6}$$

The phase portrait and error signal in case of unsynchronized are shown in Figures 3(a) and 3(b) respectively, here, the value of α and β of the drive system and the response systems are different. Figures 4(a) and 4(b) show the phase portrait and error signal in case of synchronization between the drive and the response system. In this case, the initial value of the two subsystems is different, but the value of α and β is the same for both drive and response systems. The system parameters are defined in Table 1. Simulation results show that the two subsystems are well synchronized. The design was implemented on an Artix7 xc7a100t-1csg324 FPGA device and the resource utilization was estimated as shown in Table 2.



(a) (b)

Figure 3. PC synchronization in the case of mismatched parameters (a) phase portrait and (b) error signal in case of unsynchronized



(a) (b)

Figure 4. PC synchronization in the case of matched parameters (a) phase portrait describes the xm versus xs and (b) error signal in case of synchronization

Table 1. Cascaded synchronization system parameters

		Synchronization Initial value	α & β	Unsynchronized Initial value	α & β	Slops & breakpoint
Drive system		x_0=0.3 y_0=0 z_0=0.1			α=10 β=15	m0=-2.5
Response systems	YZ Response	y_0=0.1 z_0=0.4	α=10 β=15	x_0=0.3 y_0=0 z_0=0.1	α=9 β=100/7	m1=-0.3
	XZ Response	x_0= 1 z_0=0.4				b1=0.1

Table 2. FPGA utilization summary of PC cascaded synchronization

Resource type	Available	Utilization
LUT	63400	1446
Slice Registers (FF)	126800	224
Bonded IOB (IO)	210	161
BUFGCTRL (BUFG)	32	1
DSP	240	40
Minimum period Ts (ns)	40	
Worst negative slack (WNS)	0.060	
Maximum Frequency (MHz)	25.04	
Power(W)	0.153	

4. CHAOTIC MASKING WITH FEEDBACK

There are different techniques for uses the chaotic signal in secure communications: chaotic parameter modulation, chaotic shift keying, on-off key, and chaotic masking. The chaotic masking can be viewed as one of the earliest and easiest techniques in chaotic secure communications, which is based on the PC synchronization concept and mostly used for analog signal transmission. Additionally, it is quickly implemented in electronic circuits, which is why it is used in this proposed scheme [20]. As shown in Figure 5 the general block diagram of chaotic masking, the information signal $m(t)$ is added to the wideband chaotic signal $Xm(t)$, followed by transmitting the combined (masked) signal $s(t)$.

$$s(t) = Xm(t) + m(t) \tag{7}$$

To successfully remove the mask, both master and slave chaotic signals need to be synchronized, PC synchronization is one of the most powerful synchronization schemes to do this [5]. The image $m(t)$ is precisely retrieved on the receiver side by subtracting the regenerated signal *Xs(t)* from the received signal $s(t)$ with the assumption that the system is free of noise. The recovered signal (image) is.

$$\hat{m}(t) = s(t) - Xs\,(t) = [Xm(t) + m(t)] - Xs(t) = m(t) + ex\,(t) \tag{8}$$

where

$$e_x(t) = Xm(t) - Xs(t) \tag{9}$$

$e_x(t)$ it is triggered by the fact that the presence of an information signal causes the $Xm(t)$ does not to have the same reply at the receiver. Therefore, $e_x(t)$ causes the synchronization mechanism to be disrupted. To ignore the effect of the signal information sent to the receiver on the synchronization process, the information signal is the feedback to the chaotic transmitter [21].

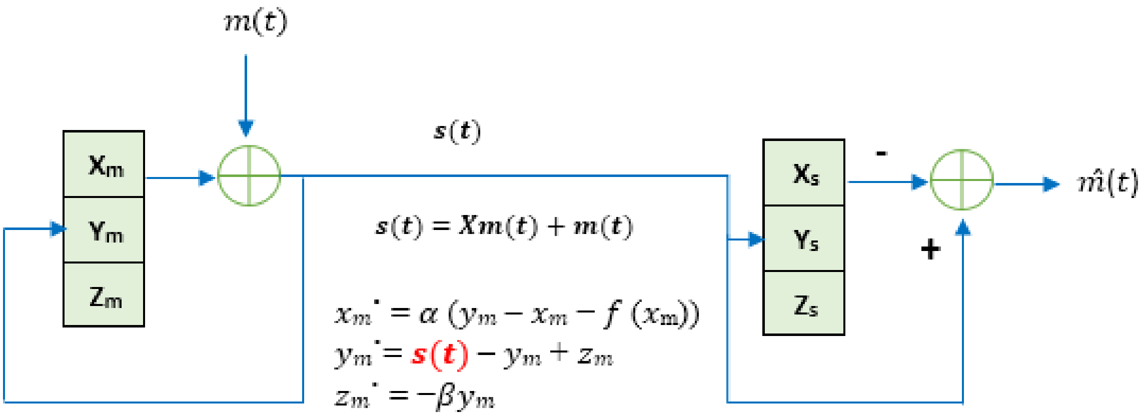

$m(t)$
$s(t)$
Xm
Ym
Zm
Xs
Ys
Zs
-
+
$\hat{m}(t)$
$s(t) = Xm(t) + m(t)$
$x_m^{\cdot} = \alpha\,(y_m - x_m - f\,(x_m))$
$y_m^{\cdot} = s(t) - y_m + z_m$
$z_m^{\cdot} = -\beta y_m$

Figure 5. Chaotic masking with feedback and recovering information based on the Chua system

5. XSG DESIGN OF IMAGE ENCRYPTION AND DECRYPTION

The XSG block diagram for encrypting and decrypting the image is shown in Figure 6. XSG input and output gateway functions are used to convert between the blocks of MATLAB/Simulink and XSG. The original color image is divided into different red, green, and blue images. This image's data type is unint8. In the first step of encryption, a pre-processing block is used to transform the original images I (Lr*Lc) dimension (where Lr is row numbers and Lc is column numbers) into serial samples. The Pre-processing block is used to transform matrix I to 8-bit serial samples (Unit8). Figure 7 displays the pre-processing blocks. The gateway-in transforms the serial sample format to an unsigned fixed point format with WL=8 and FL=0 with sample period 0.001. Then masked with the $Xm(t)$ signal produced by the Chua chaotic system to obtain the encrypted image. In the decryption process, the $Xs(t)$ response signal is subtracted from the masked signal $S(t)$. The post-processing blocks are used to transform the serial.sample into the original size (Lr×Lc) to recover the original image of the same dimension. Figure 8 displays the post-processing blocks. For all chaotic structures, like master and slave, it is implemented using a fixed-point representation with WL=32 bits and FL=16 bits. The initial values for the master system are (α= 9, β=100/7, m0=-3, m1=-0.3, b1=0.1, x0=-0.2, y0=0, z0=0.2) and for the slave system are (α= 9, β=100/7, m0=-3, m1=-0.3, b1=0.1, x0= 0.7, y0= 0.1, z0=0.6). After 70 ns (simulation time), the original image, encrypted image, and recovered image are shown in Figures 9(a) to 9(c) respectively.

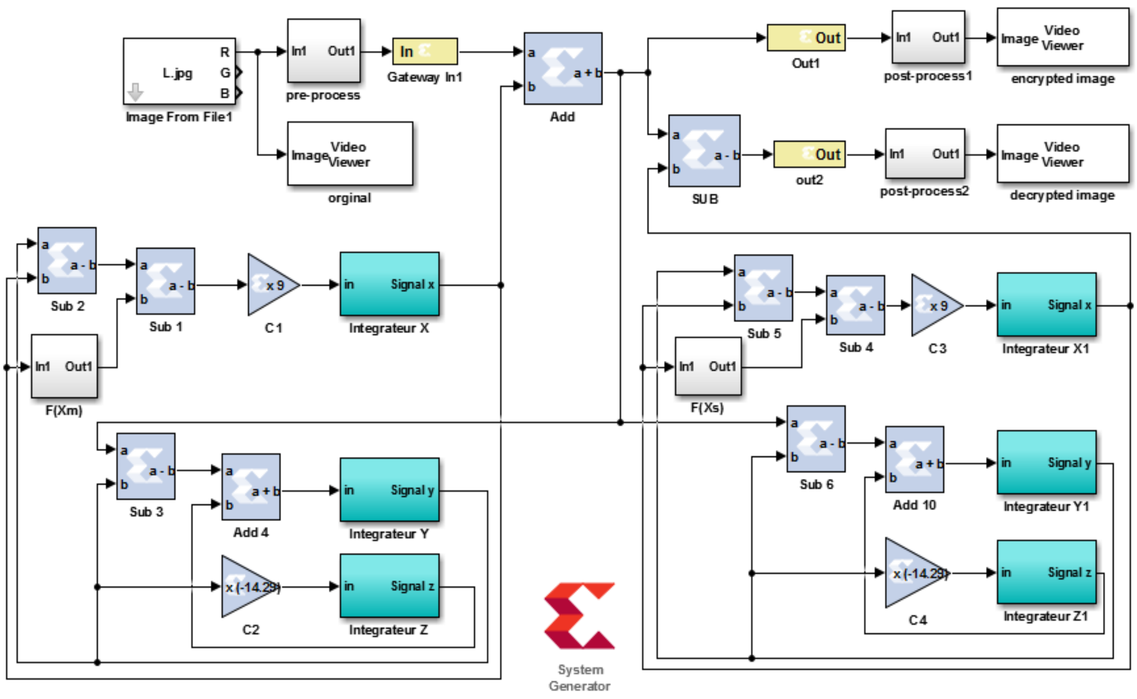


Figure 6. XSG of image encryption and decryption

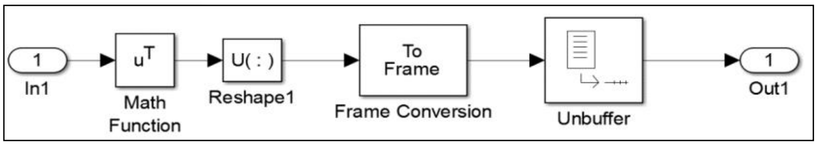


Figure 7. Pre-processing blocks

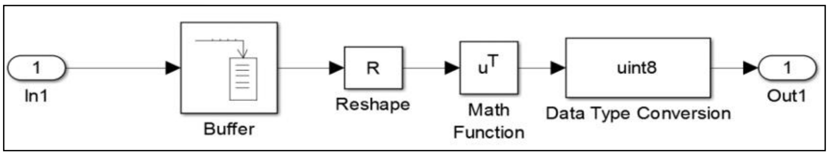


Figure 8. Post-processing blocks

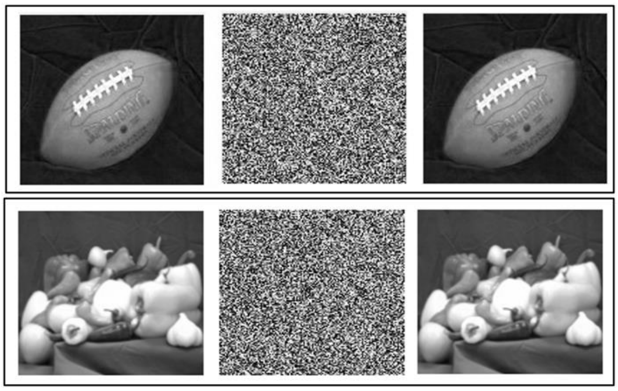

(a) (b) (c)

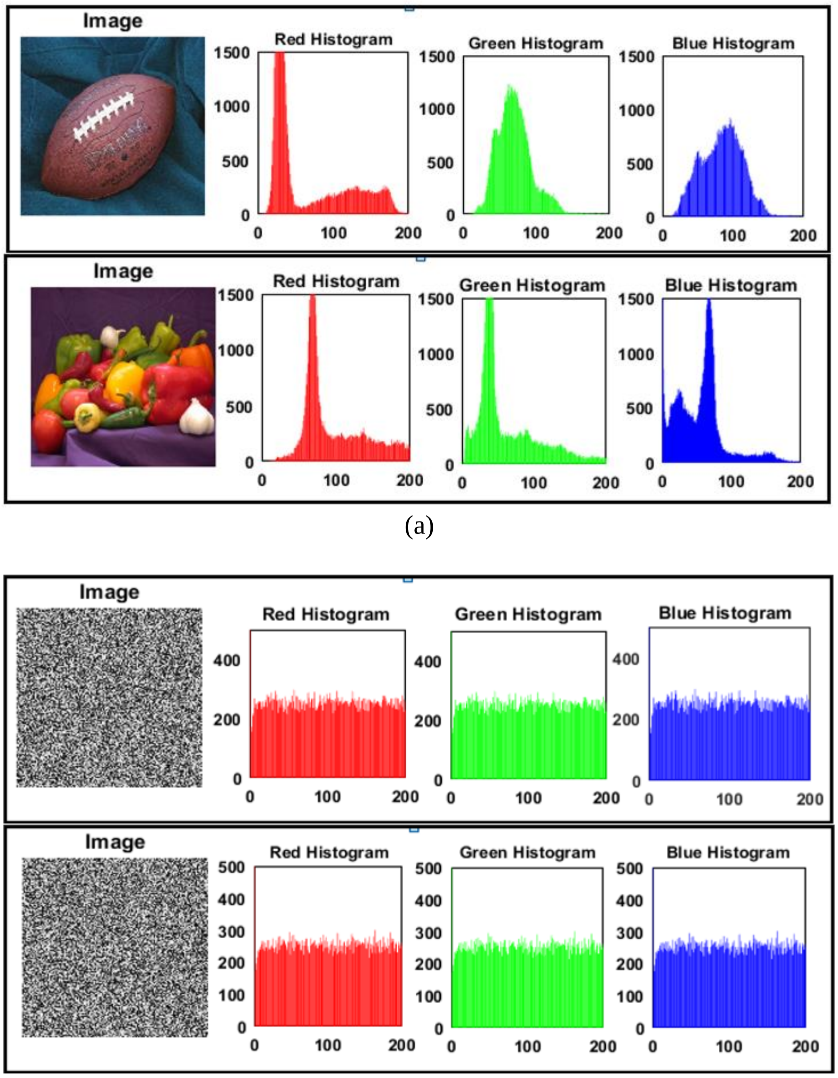
Figure 9. Results (a) original images, (b) encrypted images, and (c) decrypted images

6. STATISTICAL ANALYSIS

There are several analyses of the design's efficiency and security, including histogram, CCA, information entropy, keyspace, and a differential analysis attack. A different color image is used for analysis. Experiments are performed and data is analyzed using MATLAB environments.

6.1. Analysis of histogram

The image histogram shows the distribution of pixels by plotting the number of pixels at each level of color intensity [22]. In Figures 10(a) and 10(b), a comparison of the distribution histograms of original images and ciphered images was shown. It appears that the compression and encrypted image histograms (for R, G, B-channels) are greatly different from the original image histograms (for R, G, B-channels) and do not include any clues that could be used for any statistical analysis of the encrypted image. So, the algorithm can effectively resist statistical attacks. The original and cipher images have completely different pixel distribution at each level of intensity [23].



(a)

(b)

Figure 10. Histogram of three-channel (a) original images and (b) ciphered images

6.2. Correlation coefficient analysis (CCA)

A correlation factor is another significant factor in the study of the cryptosystem. The correlation between the pixels of the original image is strong, while the correlation between the pixels of the encrypted image is very low. An algorithm for image encryption would have succeeded if all its attributes were hidden and the encrypted image was entirely unrelated and random. If the coefficient of correlation is =1, the two images are the same. Therefore, the encryption failed in these cases. When the value =-1, the encrypted image is opposite to the plain image. The (9) is used to measure the correlation coefficient of any two-pixel color values at the same position in the original and cipher images [24].

$$Corr(x, y) = \frac{E[(x-\mu_x)(y-\mu_y)]}{\sigma_x \sigma_y} \tag{9}$$

Where μx and μy represent mean values of x and y, σx and σy are the standard deviations of x and y, and $E[\cdot]$ is the expectation function [25]. Table 3 displays experimental correlation pixels for pictures of football, and peppers with sizes 256*256.

Table 3. Correlation coefficient calculation of encrypted image with different channels

Image name	Channel		
	Red	Green	Blue
peppers	-7.6527*10^{-4}	-0.0020	0.0050
football	0.0013	0.0015	-7.3397*10^{-4}

6.3. Entropy analysis

The content of an information signal is called entropy. It determines the redundancies of the characteristic randomness [26]. The entropy of the signal information expressed as:

$$Entrp(s) = \sum_{n=0}^{2^N-1} P(si) \times \log_2 \left(\frac{1}{P(si)}\right) bits \tag{10}$$

where (si) the probability that a pixel occurs in an image, N is the length of the binary number of a pixel (usually N=8 for a gray image). An important property of the cryptosystem is it is sufficient to resist entropy attacks; the ideal entropy value of the encrypted images is 8 bits/pixel [27]. Table 4 show the Information Entropy results of two images with the size of 256×256 for different channels.

Table 4. Entropy calculation of ciphered images

Image name	channel		
	Red	Green	Blue
peppers	7.9906	7.9903	7.9908
football	7.9896	7.9905	7.9898

7. DIFFERENTIAL ATTACK ANALYSIS

It is the analysis of how variations in the input information will affect the resulting output variation to obtain the secret key. The sensitivity of a cipher picture should be high before the original image or secret key is slightly changed. As in (11) and (12), UACI and NPCR measures as shown in Table 5 are used to determine the effect on the cipher image of the change of 1 bit/pixel in the original image [28], [29].

$$UACI(C1, C2) = \frac{1}{W \times H}\left[\sum_{i,j} \frac{|c1(i,j) - c2(i,j)|}{255}\right] \times 100\% \tag{11}$$

Where W and H are the width and height of the image, respectively, C1 and C2 are encrypted representations of a plain image and a modified image.

$$NPCR(1, C2) = \frac{\sum_{i,j} D(i,j)}{W \times H} \times 100\% \tag{12}$$

Where

$$D(i,j) = \begin{cases} 0, & if\ c1(i,j) = c2(i,j) \\ 1, & otherwise \end{cases} \tag{13}$$

Table 5. NPCR and UACI test calculation for different channels

Image name	channel	NPCR	UACI
peppers	Red	99.608	34.10
	Green	99.600	33.98
	Blue	99.585	33.90
football	Red	99.621	32.31
	Green	99.612	32.28
	Blue	99.633	32.45

8. HARDWARE CO- SIMULATION OF IMAGE ENCRYPTION AND DECRYPTION

The proposed model is formulated using the FPGA board Artix7 xc7a100t-1csg324. The summary of system resource utilization for the encryption and decryption method using chaotic masking with feedback is shown in Table 6. The image encryption and decryption process are co-simulated with FPGA hardware. When JTAG is connected, serial image signal data is transmitted via a USB JTAG port to FPGA. Then serial samples were returned to the PC using the MATLAB/Simulink viewer to test the image, as shown in Figure 11. The encrypted image has proved to be the same for system generators and co-simulation, demonstrating that the actual time for the proposed encrypted image works correctly and is compatible with the configuration expected.

Table 6. FPGA utilization summary for image encryption and decryption

Resource type	Available	Utilization
LUT	63400	1563
Slice registers (FF)	126800	192
Bonded IOB(IO)	210	89
BUFGCTRL(BUFG)	32	1
DSP	240	36
Minimum period Ts (ns)	41	
Worst negative slack (WNS)	0.444	
Maximum frequency (MHz)	24.66	
Power (W)	0.128	

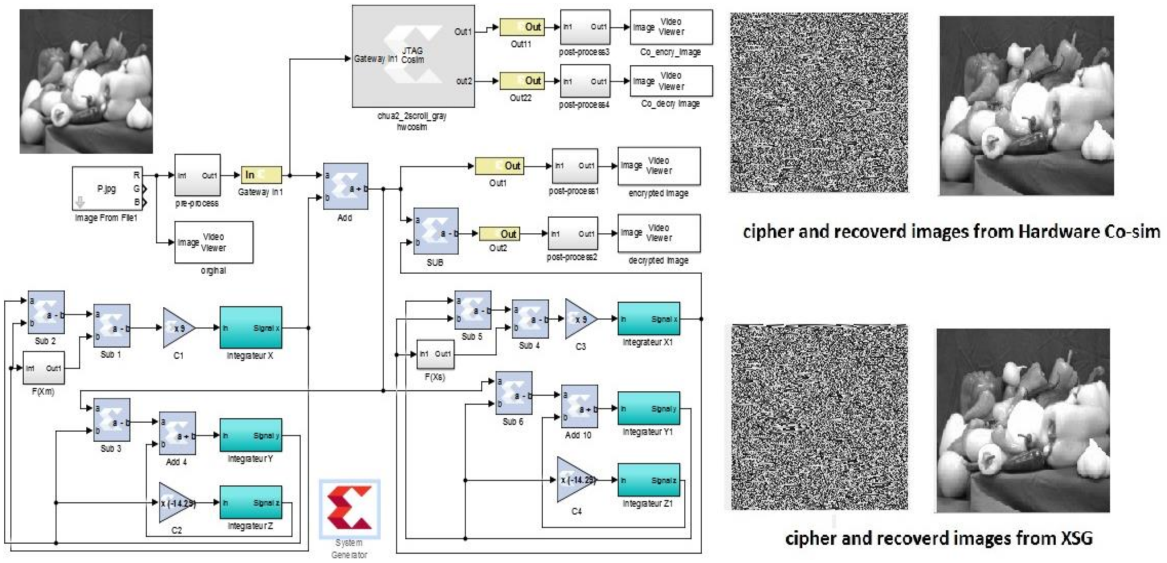


Figure 11. Hardware co-simulation results

9. CONCLUSION

In this research, Chua's chaotic attractor was synchronized based on the PC cascading method. such a chaotic synchronization phenomenon can serve as a basis for secure communication. Applying protection to transmitted images is critical, as the communication channel is open and susceptible to attack. To protect this channel, this article implements an image encryption algorithm based on chaotic masking with feedback. This method, which is based on chaotic signals, was considered the simplest in terms of secure communication because it produced an optimal analysis result that can resist various attacks and provides an extremely high level of protection that can be used to transmit images over insecure networks. The design has been implemented in an efficient way by using the XSG tool. The proposed method's synthesis results indicate that its maximum frequency is approximately 24.66 MHz. In conclusion, the real-time evaluation of the system proposed was co-simulated using the FPGA Xilinx Artix7 xc7a100t-1csg324 kit and resource utilization has been measured.

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