Design new voltage balancing control series connected for HV-IGBT`s

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ABSTRACT

The insulated gate bipolar transistors (IGBTs) are widely used in various applications as they require low gate drive power and gate voltage. This paper proposes an active gain circuit to maintain voltage stability of seriesconnected IGBTs for high voltage applications. The novel gate driver circuit with closed-loops control amplifies the gate signal while restricting the IGBT emitter voltage below a predetermined level. With the proposed circuit, serial-connected IGBTs can replace high-voltage IGBTs (HV-IGBTs) for high-voltage applications through the active control of the gate signal time delay. Closed-loop controls function is to charged current to the gate to restrict the IGBT emitter voltage to a predetermined level. This paper also presents the experiment on the gate driver capability based on a seriesconnected IGBTs with three IGBTs and a snubber circuit. The experimental results show a voltage offset with active control with a wide variation in load and imbalance conditions. Lastly, the experimental results are validated with the simulation results, where the simulation results agree with the experimental results.

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1. INTRODUCTION

In today's modern era, the demand for high-power converters has multiplied. Thus, researchers focus on the research and development of high-power converters, especially on the analysis between the semiconductor device voltage and system requirements [1]. Although the maximum collector conveyor for high voltage insulated gate bipolar transistor (HV-IGBT) reaches 6500 V, it cannot be integrated with some high-voltage power converters. The main issue of the serial-connected IGBTs is the voltage offset during the dynamic switching process [2]. The dynamic voltage offset methods for the serial-connected IGBTs can be categorized as passive control and active control. The unbalanced energy stored in the equivalent capacitors in the series related to IGBTs is essential due to voltage imbalance [3, 4]. The studies in [5] demonstrated the potential hazard for the IGBT and Power MOs devices in controlling the voltage slope and collector voltage independently, by manipulating the profile at the entrance. The reduction of conversion power losses has proven by the technique used in [6]. However, high-speed semiconductors with high voltage insulation capacity have been adapted into several applications by the industry. Hence, as a solution to the problem, a series of IGBT switch joints is one of the solutions. The IGBT switches can be connected in series, but this

connection exhibits some technical issues as highlighted in [7-9]. For example, due to different conversion features of the IGBT's, the voltage shared between the serial switches, in dynamic and static conditions, is different [10]. As a result, the switch voltage will be higher than the rated voltage, which can cause severe damage to the IGBTs. Therefore, to overcome the problem, a proper design for the IGBT gate driver is required. The need for the IGBT high voltage driver can be summarized as it is an important aspect of the project [11-13].

The serial-connected IGBT results in a power switch with improved switching performance and higher voltage rating [14]. However, it is challenging to maintain the same voltage among the existing components dynamic and in dynamic transient state [15]. There are many ways to ensure the voltage balance of the IGBTs in the series connection circuit. Based on active-use control voltage in [16], it limits the current-voltage and turn off time to control dynamic voltage sharing during transitions. In fact, the series connection of IGBT presents a structural voltage unbalance. The complex control methods implement on the circuit, the stress on the switch is compensate and lead to unequal gate driver signals to adjust voltage balance [17]. But for this paper, IGBTs will used as an experiment to do research. Therefore, the serial-connected power devices are essential for constructing power converters with high efficiency at smaller size. To address the over-voltage issues of the serial-connected IGBT, a passive voltage balancing technique is typically used [18]. For knowledge, the passive control can cause excessive power losses in the snubber circuit and delay in transient switching for stresses can be balanced in serial-connected devices [19]. In the series connection of gate turn off (GTO), pulse width modulation (PWM) may result in loss and conversion features that slow down the device inverters.

Based on previous work, the voltage conversion is usually occurred in 0.3-0.5s and the function of this intended is to stabilize the conventional voltage with a non-existent passive method [20, 21]. Transient equivalents will affect the voltage across the IGBT, which connected in series, where the transient obtained when a high rating of IGBT used, which through creating an active voltage balance [22]. Therefore, the controlled voltage must act fast, as it is to avoid any loss or reduce the frequency to change the system [23]. To equate the pressure present on the device connected in a series of steady-state voltage for the rigid condition must be adopted. To maintain the to voltage stability, the resistor can be integrated with the serialconnected IGBTs as a voltage sensor [24]. The power flows across the power switch must be restricted as high power can lead to large transient overvoltage [25]. The gate drivers able to control induced drop inductance levels in an external circuit caused it to rely on the turn off overshoot and to avoid overshoots in the turn-on assisted by steady-state voltage divisions. To withstand more voltages when switching where the device must act to be more likely, in the meantime, to withstand higher voltages during activation of slow devices [26]. In this paper, the new proposed serial-connected IGBT is evaluated in both hardware experiment and simulation. For experimentally tested gate driver capability based on an IGBT circuit connection in series using three IGBTs plus a snubber circuit. The experimental results show a voltage offset with active control with a wide variation in load and imbalance conditions. Finally, simulation test and experiment results will prove the validity of the circuit.

2. RESEARCH METHOD

The common dispersion of the device parameters, which causes voltage instability in steady-state, can be caused slightly different leakage current while switching time difference may cause intolerable transients overvoltage [27]. Among these two fundamental approaches dependence on the offset or shrink any form of differential speed switching between working on a load section as well as a series-connected device by impedance equalization, snubber network and Clamping circuit [28].

Figure 1 shows the proposed circuit for the active voltage balancing control circuit. When overvoltage in steady-state static, the circuit will force the voltage to amplify to make sure the gate start works and turn on the device when a device with small delay would cause overvoltage of steady-state applied to IGBT. However, in the voltage balancing circuit, there is a non-inverting circuit where, based on the parameter obtained, the output voltage must be regulated to the approximate output. For the simulation and hardware experiment, the output voltage is equivalent to what is desire as shown in (1).

$$V_{OUT} = \frac{\left(R_I + R_f\right)V_{ce,fb} - R_f V_{ref}}{R_i} \tag{1}$$

The IGBT voltage $V_{ce,fb}$ is a sense by using a potential divider across the collector-emitter junction, and this voltage compared with the reference voltage. When $V_{ce,fb}$ is greater than the V_{ref} due to overvoltage,

which is convert into positive gate current with appropriate feedback gain. The positive current is applied to the gate when an overvoltage across the IGBT. The IGBT collector-emitter voltage will decrease by the additional positive charge on the gate. In summary, one of the main reasons of IGBT dynamic voltage overruns is shown in Table 1.



Figure 1. The proposed active voltage balancing control scheme

Variable	Dynamic voltage	Influence factor
Turning-on	$t_{dan} \ d_v$	R _{gon} , C _{ge} , C _{ge} R _{gon} , C _{ge}
Turning-off	$d_t \ t_{doff}$	R_{gon}, C_{ge} R_{off}, C_{ge}, C_{ge}
	$\frac{d_v}{d_t}$	R_{off}, C_{ge} R_{off}, C_{ge}

Table 1. Factor affecting the dynamic-balancing process of IGBTs

The signal is generated from the PWM pulse, where it produces a 0% to 100% duty cycle using VHDL by a field-programmable gate arrays. To generate a PWM signal, a frequency comparator is required. The comparator compares two input data. The first data obtained is generated using the PWM counter, while the second data is generated via the top counter to use the push button.

Based on Figure 2, the PWM production technique is produced through a block diagram where many methods can be used when using FPGA to obtain PWM. For this project, the PWM is generated using a block diagram as it does not require coding. The pulse width modulation produced by the circuit as shown in Figure 2, as shown in Figure 3, is delivered to the gate driver to control the duty cycle.

Two causes of voltage imbalance are considered. One of these is the voltage imbalance caused by the external capacitor and the other is the voltage imbalance caused by the gate signal delay. For an imbalance caused by delays, switching transients and turning off transients is considered separately because of their different characteristics. Figure 4 shows a circuit for the gate driver. for example, the original circuit of the gate driver in such form when translated into MATLAB drawing. The gate driver circuit needs to be replaced by a pulse as a gate driver. The circuit supplies the PWM control signal to three IGBTs. No matter what the real concept is to provide pulses to IGBTs through voltage balancing also intended to compensate for the balance voltage to allow for the desired output. PWM is required by the IGBT for its operation. However, it cannot be connected directly to the circuit because it requires a gate driver as a tool to charge PWM directly to the IGBT section. In this MATLAB section, PWM is generated manually where the sine wave signal and comparator are integrated.



Figure 2. PWM using a block diagram



Figure 3. Output waveform after giving the PWM



The output is divided into two parts, which are load and IGBT. This project focus on the stability of the voltage output generated through the IGBT for V_{ce} where the voltage output stability can be seen here, and this is the objective of the project to solve the problem through the existing method. The serial-connected IGBT circuit needs to be improved, including control delay, gate driver and voltage balancing because discharged emissions are unbalanced products that can affect other applications.

Therefore, the voltage offset circuit is essential, and each circuit should be adequately examined to ensure the desired output can be achieved. When the HV-IGBTs are connected in series, the voltage imbalance occurs due to the transmitter variance of the manufacturer which cuts the current. In other word, differences between state equivalent resistance, which can be defined as R, leads to an external imbalance voltage. Therefore, the general method for balancing the static state voltage is to connect the resistor. Figure 5 is one of the IGBT circuits connected to the serial connection and is included with the pulse without inserting the voltage balancing circuit.



Figure 5. Series connection of IGBTs circuit without voltage balancing

3. RESULTS AND DISCUSSION

The function voltage balancing is to control the circuit by controlling the duty cycle using a gate driver. The circuits of serial-connected IGBTs using three IGBTs are constructed in simulation and hardware to validate the effectiveness of the proposed method, where the voltage source Vs is 1.1 kv as shown in Figure 6. By referring to output voltage collect-emitter, the rotational delays do not result in a steady-voltage imbalance, small delays during conduction can increase the voltage across the suspended IGBT. High voltage thrust was not observed with a delay of less than 0.3us as each IGBT was not fully saturated. The delayed gate driver signal generates a temporary voltage surge across the device. Although this does not create a steady voltage imbalance, the device still suffers from the loss of power and local warming in. However, the simulation results as shown in Figure 7 is the same as the only difference is that in this figure is when it is focused on more outcomes when switching on a gate IGBT.



Figure 6. Complete design of voltage balancing control circuit for series-connected HV-IGBT

The result of the simulation in MATLAB is validated in hardware experiment. The output seen in Figure 8 is comparable with the simulation result with some noise because of hardware implementation. Technically, the output is observed to have the imbalance voltage without the snubber circuit. Then, the value obtained is based on the measured voltage on the collector and emitter, which is known as V_{ref} . With the input supply voltage of 11KV and V_{ref} of 3.7 V, the output voltage is around 4.38 V. Voltage imbalance of series IGBTs can be divided into three stages in the overall trimming and trimming process. The main reason for the voltage imbalance is the mismatch between ton and the lower decline d_v/d_t . The voltage imbalance caused by different snubber capacitor values with an inductive load. Without active control, the device can experience overvoltage near the device voltage rating because of the high d_v/d_t during turn-off transient. Since the balance barrier is not used, the tensile imbalance during the rotational transition results in a steady-state voltage imbalance.







Unbalanced voltage reduction in serial-connected power device, with capacitance addition out and resistor in power part, together with the use of conversion postponement still had in the past solution that is

most common. Nevertheless, since snubber technique produced higher power loss, it is essential to seek for an optimum driving strategy that can ensure a balance that is enough voltage partnership between power device connected series is topic that intriguing in-field high power conversion. For information on Figure 9 for output obtained is the result of switching voltage balancing differs from the output that has been exhibited in the previous researcher [3].

Figure 10 shows significant differences in output when measured on oscilloscopes. For the 1st part, the pf the output voltage is in a state of equilibrium. The new circuit the Snubber circuit that acts to support the stability of the voltage were added. Hence, discussions that can be done are the voltage generated from the output measured through the emitter collector's feet, indicating that the voltage is balanced. As explained in the previous section, the V_{ref} of 370 V has been reduced to V_{ref} =3.7 V and Vin=1.1 kV also reduced to Vin=11 V. The result shows all parameter values decreased aimed at security aspects and cost to have components is very expensive. However, as a study, the result is produced to analyze every resulting output. From the findings, there are so many losses that arise, and this will be improved for the future.



Figure 9. Output voltage imbalance measure by a digital oscilloscope

Figure 10. Output voltage balancing by digital oscilloscope

4. CONCLUSION

Active voltage offset control for various HV-IGBT connections in the series proposed in this work. The new voltage balancing method for IGBTs series Microcontroller is suggested in this work. The Microcontroller can generates control signals using the future that high-level voltage is applied to the gate, but the transmitter voltage will fall. The high-level voltage can produced when the overvoltage occurs, so the number of signals, control signals and original conversion signals acts as door driver inputs. This paper demonstrates that practical can use the continuous IGBT series in high voltage applications with the following advantages. The electronic system of power can be compact, precise control can be achieved, harmonic can be much and losses can be reduced.

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