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Switched capacitor based multi-level boost inverter for smart grid applications

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ABSTRACT

To link DC power sources to an AC grid, converters are needed. Inverters are the power electronic devices, which are used for this purpose. Conventional inverters employ harmonic filters and transformers that are lossy and expensive. Multilevel inverters (MLIs) are an alternative to conventional ones, proposing reduced total harmonic distortion (THD), increased range of control, and inductor-less design. They generate a stepped waveform, with close similarity to a sine wave. Many distributed sources may be employed in a smart grid. If those sources have minimal THD, the filtering process could be reduced at the point of common coupling. This paper presents two switched capacitor based MLIs, proposing boost capability and low THD. Inverters have inherent charge balancing capability, which eliminates the need for auxiliary circuits and voltage sensors. Inverters switches are modulated using phase opposition disposition pulse-width modulation (PODPWM) method that ease the balancing of the voltage and decrease the losses of switching. Designs were verified by simulation and the output waveforms were introduced.

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1. INTRODUCTION

Recently, industries have needed equipments with higher power. To convert and control that power, power electronics are essential. These devices are nowadays the most important component in extracting power from renewable sources. During conversion of AC to DC or vice versa, efficiency plays an important role in high powered applications. Power electronics enables highly efficient conversion of power, reducing losses expended as heat and in turn, size of the devices.

To convert DC voltages to AC waveform, inverters, which are power electronics modules, are needed. The output frequency maybe constant or variable depending on the application. The waveform that closely resembles a sinewave with least content of harmonic and it increases with increase in deviation of the output voltage waveform from this wave. In certain applications, that might lead to large losses and generate pulsating torques, such as, with the application to an AC motor [1]-[2].

THD is a measure of the harmonics that are present in a waveform. These harmonics are integral multiples of the fundamental frequency. Harmonics mitigation is crucial as they distort the output waveform

and produce losses in the system. Due to the presence of several distributed sources in smart grid, handling the harmonics at the point of common coupling (PCC) becomes an issue. MLIs are lucrative power conversion alternative as they are simple to control and are useful for low harmonics power injection.

In order to reduce these harmonics, passive filters have been widely available. However, the main issue with these filters is that the size of the inductor and capacitor is too large to be feasible and efficient for lower order harmonics at a fundamental frequency. Power electronics provide the means to convert electric power generated into that required by the load. They are a crucial component in the power system which forms the power grid of a country. Multilevel inverters produce a stepped waveform, which is like to a sine wave. The required stepped waveform could be determined by applying one of PWM methods. The principle aim of a multilevel inverter is to produce a waveform that resembles a pure sine wave as much as possible [3].

Cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitors (FCs) are considered the three classical multilevel inverter topologies. The first type introduces a good performance and could achieve higher levels of voltage with high power quality [4], [5]. Traditional multilevel inverters require many auxiliary circuit devices to balance the capacitors charge [6], [7]. They do not have a boost function as the the output voltage magnitude could not be greater than the scalar superimposition of the DC link voltages [8]. Current trends in multilevel inverters are alternative topologies for CHBs with less switches number and improved THD reduction. In addition, other properties, such as, new applications, improvement of the efficiency, fault tolerant operation, and optimized control methods gain attention. Easy modules replacement in fault cases would be due to high modularity degree feature of the converters, which means that each inverter is a module with the same control scheme and circuit topology.

Qualitative improvement is done by reducing THD by increased number of levels and improved PWM strategy in this work, two improved configurations of switched capacitor-based step-up Multilevel inverters are proposed. Quantitative and qualitative aspects of the multilevel inverter (MLI) are improved, along with analysis of THD of the output voltage under different modulation index and control strategies. Quantitative improvement is done by reducing the number of semiconductor switches and diodes [9]-[15].

Electronic power conditioning and control of the production and distribution of electricity are important aspects of the smart grid. Thus, some techniques such as load forecasting have been developed to cope up with the increase in demand of electric power. Targeting PHEV powertrains optimization, a plethora of energy management strategies (EMSs) have been proposed [16]. Varying in complexity and accuracy, these algorithms offer different solutions according to the need of the given system.A preliminary study of various topologies and working of multilevel inverters was done. General considerations, important topologies such as cascaded H-Bridge inverters, diode clamped inverters and switched-capacitor inverters were studied. Relevant control methods such as Phase disposition PWM, Phase opposition disposition PWM were considered. The circuit simulation was done using MATLAB/Simulink. The SIMSCAPE power systems toolbox enables simulation of complex PWM modulation techniques with relative ease. FFT analysis can be done on the output waveform for computing THD. The author in [17] presented a DC-DC boost converter which utilizes switched capacitors as the storage element unlike inductors in conventional boost converters. It also has self-balanced voltage of capacitors and is modular.

Barzegarkhoo *et al.* [18] proposed a novel switched capacitor-based inverter with reduced number of circuit devices along with detailed analysis of cascaded topologies. The main structure of introduced converter was the capability of producing nine-level output voltage using the same two capacitors paralleled to a DC voltage source with variable loads.

Multilevel inverters consisting of cascade of one or more units is done in [19]-[21]. In [19], it was presented a new family of cascaded multilevel inverters (CMLIs) that could produce a significant number of levels of the output voltage with minimum associated switching devices. Mohammed *et al.* [20] introduced a power inverter topology that generates 15 voltage levels by 4 DC-links and 8 power switches. In [21], a cascaded asymmetric multilevel inverter was introduced (25 output levels.) It had a minimum number of switches (10 switches) and could be employed in AC applications using solar energy. The circuit layout was optimized.

Another topology is presented in [22] to consider the cost and size. A 15-level inverter was proposed. A 71-level inverter and an m-level inverter were proposed considering the basic unit development. Comparing the inverter with conventional MLIs, the inverter was capable of generating higher number of output levels using lower number of power electronic devices and DC voltage sources. A topology suggested by Hsieh *et al.* [23] requires additional circuitry to facilitate charge balancing of capacitors. It produced seven-level ac output voltage with the proper gate signals' design. THD was reduced by using a low-pass filter. In [24], a topology consisting of modified H-bridge is proposed by Kamaldeep *et al.* Eight switches were needed to produce 15-level single phase output voltage. That was simple, with smaller size and cost effective.

A study of different PWM techniques employed in inverters is presented in [25] by Ilhami *et al.* to match inverter topology and the best control scheme. Kishore *et al.* has presented a study in [26] where performance improvement by implementing different PWM techniques. The PWM strategies include phase disposition PWM (PDPWM), alternate phase opposition disposition PWM (APODPWM), and PODPWM. It aimed to present two novel designs of switched capacitor-based inverters which have voltage boost capability and self-charge balancing of capacitors. First, the configuration proposed in the base paper is simulated and the expected output waveform and characteristics are verified. Then, a novel configuration is presented wherein the same 19-level voltage waveform is obtained using 2 DC voltage sources and 4 capacitors with only 10 power switches. The relevant switches are modulated on a new PDPWM technique which reduces switching losses considerably. Reduced complexity is also a feature of the proposed inverter. A second novel configuration based on the above design is presented, wherein a 17-level voltage waveform is obtained using 2 DC voltage sources and 2 capacitors with 9 power switches and also uses a similar PDPWM technique. The first novel module focuses on producing the same performance and output characteristics as the base model, while reducing the number of components and power losses. The second novel module aims at producing nearly the same output, but also drastically reducing the number of components, thereby decreasing the cost of the inverter. It also thus increases its reliability. The circuits are verified under resistive loading conditions using MATLAB/Simulink.

2. INVERTER CIRCUITS AND OPERATIONS

Multilevel inverters with novel switched capacitor-based designs have been proposed by various authors [27]-[29]. These designs focus on reliability while reducing the costs of the components and power losses. A switched capacitor based 19-level inverter has been presented in [30] and has been analyzed and simulated first. The circuit proposed in the base paper is shown in Figure 1. The inverter can produce 19-levels of output voltage stepped waveform is as in Figure 2 while operating at a low switching frequency [30]. The main features of switched capacitor-based circuits are; Boosting capability of the output voltage. Requiring only 4 electrolytic capacitors and 2 voltage sources to produce high number of voltage levels. Use of only 12 power switches and 10 gate drivers working at low switching frequency.

Employing HPWM technique would Lessen total switching loss. Switched capacitor inverters offer many features such as high reliability, reduction in cost, easy swapping of components. However, the main disadvantage is that they require delicate voltage or charge balancing to be done. This can be done in open loop by natural charge balancing every cycle by providing suitable switching and current flow paths. It can also be done closed loop or by using a RLC filter tuned at the switching frequency in parallel with the load. However, this increases the cost and depreciates the dynamic response of the circuit. The PDPWM technique is considered the best method to be employed for a capacitor based MLI as it offers self-balancing property when applied to an ideal and symmetrical circuit. The SC cell unit can produce 9 levels (4 positive, 4 negative and one zero level) using 2 passive diodes, 2 integrated capacitors, and 9 power switches. With series- parallel capacitors conversion along with the DC source (2 V_{dc}), positive levels 0, 2 V_{dc}, 4 V_{dc}, 6 V_{dc} and 8 V_{dc} and the corresponding negative levels would be generated. The voltage across C_1 and C_2 is 2 V_{dc} and 4 V_{dc}, respectively. The diodes are used to counteract the effect of the parasitic body diode present in the power switches and enable the reverse flow of load current.

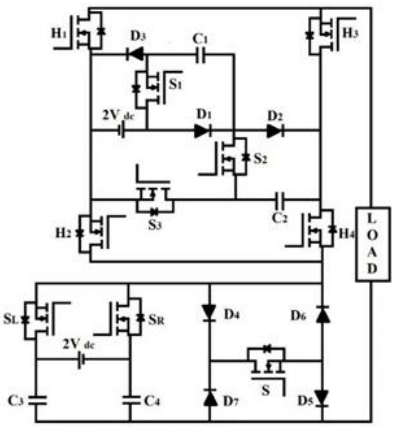

Figure 1. Proposed novel topology-1 (NT-1) circuit

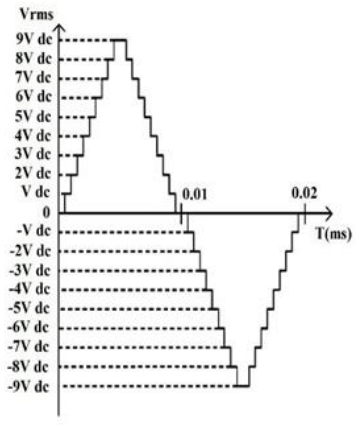

Figure 2. NT-1 overall theoretical waveform

The FCB cell unit produces three levels (1 positive, 1 negative and one zero level) using two capacitors, four diodes and 3 power switches. Similar to the series-parallel switching in the SC cell, the FCB cell also produces levels 0, V_{dc} and -V_{dc}. The backward load current would be undertaken with the power diodes. That current is due to inductive loads, which could cause voltage blocking. The modulation index was chosen as 0.95. As the proposed method would generate a 19-level output voltage, using 18 carrier waveforms would enlarge the system complexity. Switching loss value could be decreased with HPWM methodology, which has the fundamental and high switching frequencies in the hybridized MLVSIs. The circuit has been simulated in MATLAB and the output voltage waveform has been presented in Figure 3. The circuit uses series-parallel switching of capacitors using power semiconductor switches and diodes to produce multilevel stepped waveform. Zero voltage level can be achieved using either of the redundant states by turning ON the switches T_1, S and T_2 or T_1', S and T_2'. Also, S_{p1} is turned ON to charge the capacitor C_1 to 2 V_{dc}. The working of the SC cell is described as follows: The first output voltage-positive and negative - levels (±2 V_{dc}) determined by using only the DC source 2 V_{dc} without any of the capacitors in the load path. Also, S_{p1} is kept ON facilitating charging of the capacitor C_1, while C_2 remains disconnected. For the second output voltage -positive and negative- levels (±4 V_{dc}), the voltage across of the DC source is added to the voltage of C_1 that has been previously charged to V_{dc}. By turning OFF S_{p1} and turning ON S_{s1}, C_1 is now discharging. The net voltage across the load is now the addition of DC source V_{dc} and voltage 2 V_{dc} accumulated in C_1, i.e., 4 V_{dc}. Also, in this interval, by turning ON S_{p3}, power diode D_2 becomes forward biased and C_2 now gets charged to 4 V_{dc}. The third output voltage - positive and negative -levels (±6 V_{dc}) are created by series connection of the stored voltage in C_2 and the DC voltage source value through the series switch S_{s2}. This is achieved by turning ON the switch S_{s2}. Also, S_{p1} is turned ON to charge C_1 again to 2 V_{dc}.

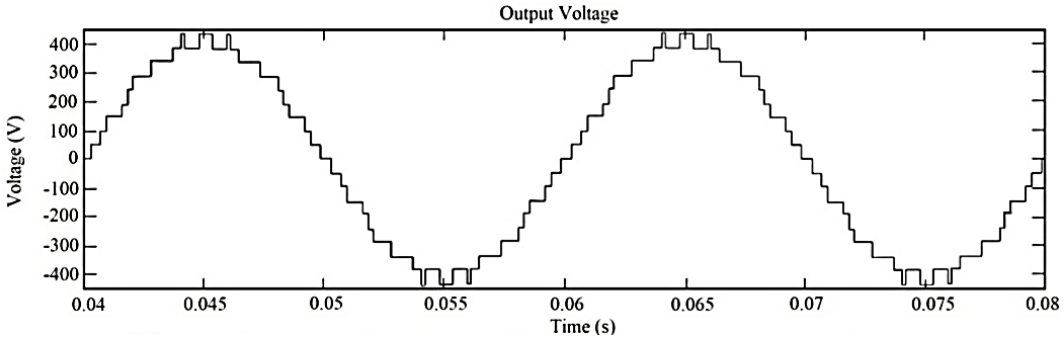

Figure 3. Overall output voltage of design proposed in base paper

Eventually, in the fourth output voltage levels - positive and negative -(±8 V_{dc}), the capacitors must be series with the supply via S_{s1} and S_{s2}. This is done by turning ON the switches S_{s1} and S_{s2}, discharging both the capacitors and the required voltage level is attained. The FCB cell produces 3 level waveform of amplitude V_{dc}, which when superimposed with the output of the SC cell output waveform using suitable modulation technique, a 19-level waveform is finally obtained. Figure 1 shows the introduced topology circuit, which has two distinct switched capacitor-based cells, floating capacitor (FC) and switched capacitor (SC) cells, which produce the required 19-level output waveform. A DC voltage sourcealong with two capacitors are employed in each cell and would be switched properly to generate the 9-level and 3-level waveforms. The FC cell operates at higher switching frequency while SC cell is at low one. FC cell generates a three-level waveform (a positive level, a negative level and a zero level), but SC cell generates a nine-level waveform (4 positive levels, 4 negative levels and a zero level). If both types are connected in series, that would allow a stepped sine wave to be generated by the inverter, with a peak amplitude of nine times the DC voltage source. That could be conducted using 10 MOSFET switches, 3 diodes, and 4 capacitors. Voltage boosting would be guaranteed by the diodes and the capacitor of the network. Series-parallel switching of the capacitor network through the semiconductor switches would balance the capacitors voltage, allowing uniform charging and discharging cycles. The circuit could operate with minimized switching frequency and small switching losses when using phase disposition PWM (PDPWM) technique.

A schematic of the SC circuit is shown in Figure 4. When turning ON the switches H_1 and H_2 or H_3 and H_4, a level of zero voltage could be gained. D_1 would be forward biased and charge C_1 to 2 V_{dc}.

The first positive and negative voltage levels (±2 V_{dc}) is obtained by using only the DC source 2 V_{dc} without any of the capacitors in the load path. C_1 keeps its voltage at 2 V_{dc} by the connection to the voltage source. When S_1 is ON, the voltage of the source added with C_1 voltage give the second positive and negative voltage levels (±4 V_{dc}). When S_3 turns ON, D_3 would be forward biased and charge C_2 to 4 V_{dc}. When S_2 is ON, the voltage of the source added with C_2 voltage give the third positive and negative voltage levels (±6 V_{dc}). C_1 charges to 2 V_{dc} as D_1 becomes forward biased. When S_1 and S_2 are both turned ON, the voltage of the source added with C_1 and C_2 voltages give the fourth positive and negative voltage levels (±8 V_{dc}).

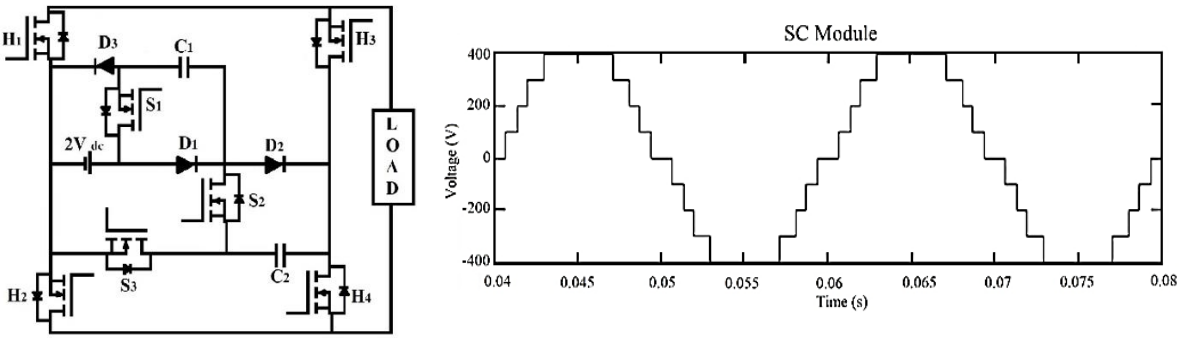

Figure 4. SC cell of NT-1 circuit and output waveform

The floating capacitor circuit is shown in Figure 5. Switch S, diodes D_4, D_5, D_6 and D_7, ease bidirectional current flow. C_3 and C_4 have been located to ease their charging to voltage V_{dc} simultaneously, with opposing polarity.Capacitors get discharged to the load when either of the switches S_L or S_R are closed, contributing to the output waveform. Capacitors do not add to the upper cell when switch S is ON. Hence, the voltage source is never directly connected to the load and is used only to charge the two capacitors. During the positive half cycle, only capacitor C_3 is used and during the negative cycle, only capacitor C_4 is used. Without any external circuitry, voltage balancing of capacitors is obtained using switches S_L and S_R in tandem with S.

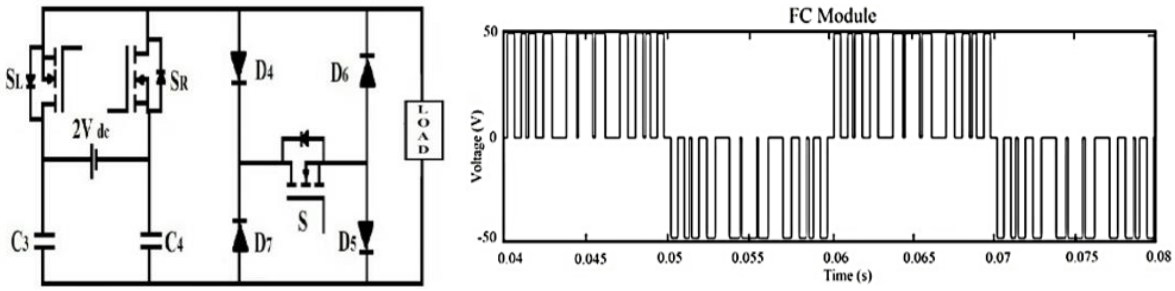

Figure 5. FC cell of NT-1circuit and output waveform

The converter circuit consists of 9 switches, 3 diodes, 2 capacitors and 2 DC voltage sources. This work discusses a symmetric configuration, where both voltage sources have the same magnitude of voltages. The 2 capacitors act as storage elements and are charged and discharged multiple times within the same cycle. Each switch is switched ON and OFF to yield different output voltage at each stage, producing multilevel voltage waveform. This multilevel waveform, when fed to an H-Bridge produces multilevel AC voltage of reduced THD. Each charging stage consists from 2 modes; Switch S_4 is ON and Switch S_5 is OFF and Switch S_5 is ON and Switch S_4 isOFF.

In mode 1, only voltage source is present in the charging circuit. In mode 2, both the voltage sources are present in the charging circuit. It is assumed that each voltage source is of magnitude 100 V. Hence,

capacitor C_1 gets charged to a voltage of 100 V and 200 V, while capacitor C_2 gets charged to voltage of 200 V and 400 V during the operation of the circuit. Thus, at each stage, different output voltages are obtained by series-parallel switching of the voltage sources with the capacitors facilitated by the power semiconductor diodes and switches. Figure 6 shows a schematic of the proposed power circuit.

Both capacitors are self-charge balanced during each cycle without the need for external circuits to discharge the charges during each cycle. This is achieved by series-parallel switching of capacitor network realized using phase disposition pulse width modulation (PDPWM). This facilitates complex gate signals which can switch ON and OFF the switches multiple times during a cycle, giving rise to charging and discharging paths and redundancies.

The circuit works by alternatively switching ON and OFF switches S_4 and S_5 complementary to each other. Turning ON the switches H_1 and H_2 or H_3 and H_4, zero voltage level could be obtained. D_1 would be forward biased and charges C_1 to V_{dc}. The first positive and negative voltage levels ($\pm V_{dc}$) are determined by using only one DC source V_{dc} without any of the capacitors in the load path. That could be done by switching ON S_4. Then, by turning ON S_5 and turning OFF S_4, D_3 gets forward biased and C_1 gets charged to 2 V_{dc} by being connected to the voltage sources in series to each other and the second positive and negative voltages ($\pm 2 V_{dc}$) are maintained.

When S_1 is ON, the voltage of the source added with C_1 voltage give the third positive and negative voltage levels ($\pm 3 V_{dc}$). The fourth levels - positive and negative - ($\pm 4 V_{dc}$) are determined by switching ON S_5 and adding the second voltage source. When S_3 turns ON, D_2 would be forward biased and charge C_2 to $2V_{dc}$. If S_2 is ON, the voltage of the source added with C_2 voltage give the fifth and sixth positive and negative voltage levels ($\pm 5 V_{dc}$) and ($\pm 6 V_{dc}$). C_1 charges to V_{dc} as D_1 would be forward biased and C_2 keeps voltage of $2V_{dc}$. When S_1 and S_2 are ON, the voltage of the source, added to C_1 and C_2 voltages give the seventh and eighth positive and negative voltage levels ($\pm 7 V_{dc}$) and ($\pm 8 V_{dc}$). Figure 7 illustrates the 17-level stepped waveform.

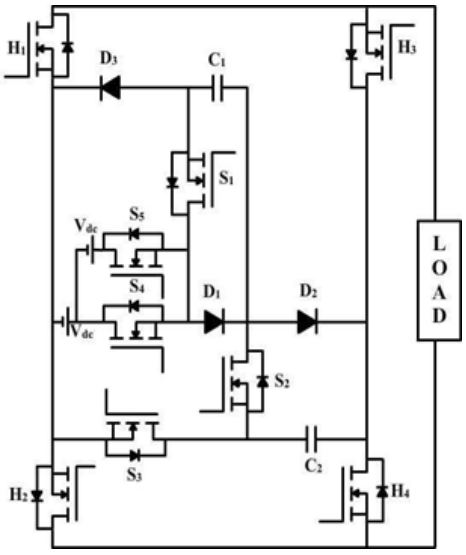

Figure 6. Proposed novel topology-2 (NT-2) circuit

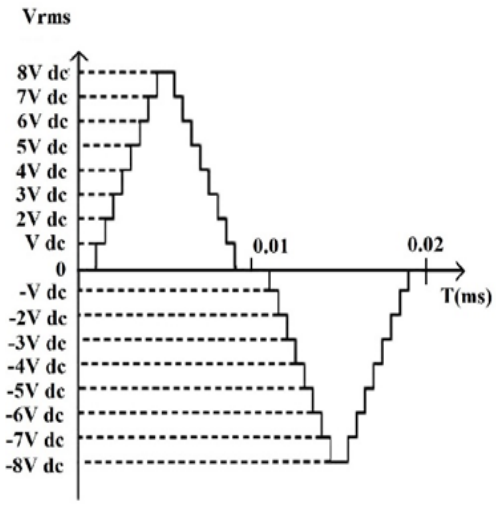

Figure 7. NT-2 overall theoretical waveform

3. PROPOSED PWM STRATEGY

The switching pulses for the switches in both of the above proposed topologies are obtained by comparison of reference sine waveform which resembles the desired output voltage with carriers. The technique used here is called phase disposition PWM (PDPWM), wherein, the absolute function of a reference sine waveform is compared to 9 level shifted triangle carrier waveforms in the first novel topology and 8 level shifted triangular carrier waveforms in the second novel topology. The reference sine wave is chosen to have an amplitude of 9 or 8 and each of the triangle carrier waves have an amplitude of 1 each. The reference sine wave is defined as

$$V_{ref} = Arsinwt \quad (1)$$

The next equation is to compute the modulation index:

$$m = \frac{Ar}{n.Ac} \quad (2)$$

Where A_C is the amplitude of each carrier wave, n is the number of triangular carrier waves and A_r is the amplitude of the reference sine wave. A_r is chosen as 9 and 8 in the first topology and second topology respectively and A_C is chosen as 1. Thus, the modulation index is calculated as 1. This allows the maximum number of levels to be obtained and the THD to be minimized in this particular case. Also, a commander coefficient (CM) is defined to be used to select positive or negative halves of the reference wave over a single cycle.

$$CM = \frac{1+sgn(V_{ref})}{2} \quad (3)$$

If CM is selected to be 1, the comparison between V_{ref} and each carrier waveform will be done in the first half-cycle of the reference waveform; hence the positive output voltage levels are made, whereas by setting CM on zero, the second half-cycle of the reference waveform is involved in the comparative process and as a result the negative steps of the output voltage are built. In the novel topology 1, the number of switches in the SC cell have been reduced and the switching mechanism in the FCB cell has been changed such that only two of the switches operate at high frequency at a given time, hence reducing both switching and conduction losses. In the novel topology 2, the FC cell has been removed and two new switches have been added to the SC cell to enable selection of either of the two voltage sources. These selecting switches work at high frequency complementary to each other while the other switches operate at low switching frequency.

4. RESULTS AND DISCUSSION

4.1. Simulation of novel topology 1

The proposed 19-level SCMLI was simulated using MATLAB/Simulink. The Simscape Power Systems toolbox was used for simulation. The Tustin/Backward Euler solver was utilized. The objective of this work is to minimize THD for a 200 ohm purely resistive load foe both the topologies. The FFT Analyzer was used to compute the output current and voltage waveforms THD. The output parameters, and circuit design parameters of the inverter are shown in Tables 1 and 2. FFT analysis was performed on the load current and the result obtained is shown in Figure 8. THD of the load current was found to be 5.80 %. The third harmonic component of the output current was found to be 0.47%.

4.2. Simulation of novel topology 2

The proposed 17-level SCMLI was simulated using MATLAB/Simulink r2018a. The SIMSCAPE Power Systems toolbox was used for simulation. The Tustin/Backward Euler solver was utilized. The objective of this work is to minimize THD for a 200 ohm purely resistive load foe both the topologies. The FFT Analyzer was used to compute output current and voltage waveforms THD. The output parameters and circuit design parameters of the inverter are shown in Tables 3 and 4.

Table 1. Output parameters of NT1

Parameter	Value
Vrms	302.9 V
Irms	1.59 A
Output Power	481.6 W

Table 2. Design parameters of NT1

Parameter	Value
Input DC Voltage Source in FC Cell	100 V
Input DC Voltage Source in SC Cell	100 V
Design Power	500 W
C1	2000 µF
C2	3000 µF
C3	1000 µF
C4	1000 µF

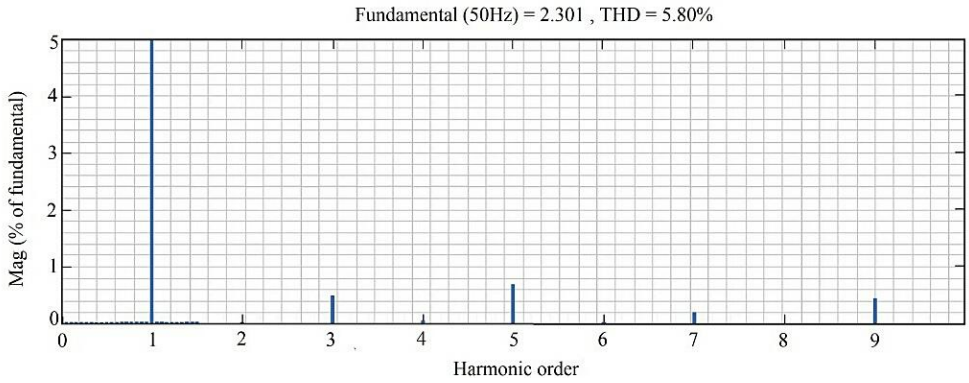

Figure 8. THD characteristics of output current of NT-1

Table 3. Output parameters of NT2

Parameter	Value
Vrms	527.0 V
Irms	2.635 A
Output Power	1388.6 W

Table 4. Design parameters of NT2

Parameter	Value
Input DC Voltage Source in FC Cell	100 V
Input DC Voltage Source in SC Cell	100 V
Design Power	1400 W
C1	2000 µF
C2	3000 µF

Figure 9 illustrates FFT analysis results, which applied on the load current. Load current THD=6.41% and the output current third harmonic component=1.71%. The modulation index of both the above topologies can be changed according to the needs of the load. As discussed earlier, PDPWM strategy is used for modulation of the above topologies with 9 and 8 carriers respectively.

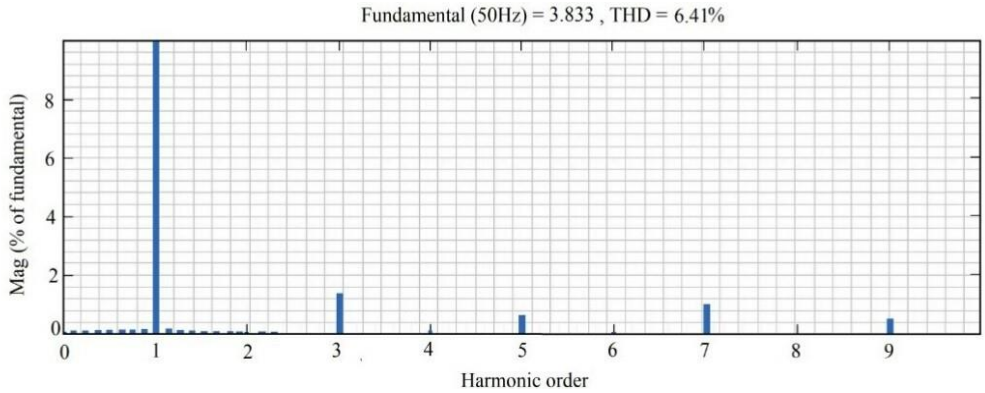

Figure 9. THD characteristics of outpu current of NT-2

5. CONCLUSION

In this work, a switched capacitor based single phase multi-level inverter with reduced number of devices is first simulated. Then, two novel designs based on the simulated model is proposed, wherein the models focus on reducing losses and costs while increasing reliability. A literature survey of the different topologies of multi-level inverters and new PWM techniques was presented. The carrier based PDPWM

technique was used for generating switching pulses. The output waveforms for voltage and current were recorded for a resistive load. Simulation was done in MATLAB/Simulink environment using the SIMSCAPE power systems toolbox. FFT analysis for output voltage and current was done and the THD was noted.

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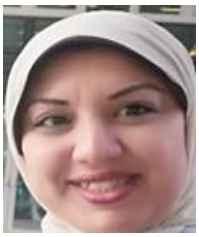

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