International Journal of Electrical and Computer Engineering (IJECE)
Vol. 12, No. 1, February 2022, pp. 201~207
ISSN: 2088-8708, DOI: 10.11591/ijece.v12i1.pp201-207

The impact of channel fin width on electrical characteristics of Si-FinFET

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Article Info

Article history:

Received Sep 3, 2020
Revised Jul 23, 2021
Accepted Aug 11, 2021

Keywords:

Channel fin width
FinFET
MOSFET
Subthreshold swing
Temperature

ABSTRACT

This paper studies the impact of fin width of channel on temperature and electrical characteristics of fin field-effect transistor (FinFET). The simulation tool multi-gate field effect transistor (MuGFET) has been used to examine the FinFET characteristics. Transfer characteristics with various temperatures and channel fin width (W_F=5, 10, 20, 40, and 80 nm) are at first simulated in this study. The results show that the increasing of environmental temperature tends to increase threshold voltage, while the subthreshold swing (SS) and drain-induced barrier lowering (DIBL) rise with rising working temperature. Also, the threshold voltage decreases with increasing channel fin width of transistor, while the SS and DIBL increase with increasing channel fin width of transistor, at minimum channel fin width, the SS is very near to the best and ideal then its value grows and going far from the ideal value with increasing channel fin width. So, according to these conditions, the minimum value as possible of fin width is the preferable one for FinFET with better electrical characteristics.

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1. INTRODUCTION

The scaling down of conventional metal oxide semiconductor field effect transistor (MOSFET) has become harder because it has serious effects of short channel on the characteristics of transistor when it is minimized lower than 32 nm [1], the minimization width and length of channel of MOSFET guide to a bad characteristics and increasing average consumed power. The main reason of these bad performances is related to the implementing the MOSFET inside the Si wafer, so, the main idea to improve the performances of transistor is free the MOSFET and isolate its structure on the surface of Si wafer. Much silicon on insulator silicon on insulator (SOI) structure have been invented to isolate transistor from silicon bulk like silicon nanowire transistor, carbon nanotube transistor, fin field-effect transistor (FinFET) structure. One of those new innovated structures is the FinFET as shown in Figure 1 [2]. The FinFET structure has free from many serious defies related with the continual scaling down structure of planer MOSFET [3]-[5].

The first FinFET like structure has been fabricated by Hashimoto *et al.* [6], the research of Hashimoto *et al.* reports a new double-gate SOI structure MOSFET structure [6]. In the last decade, many researchers direct their attention to the FinFET because of good performances in Nano-dimensional range and to overcome the short channel effect problems of conventional planar MOSFET [7]-[11]. The excellent short-channel behavior of FinFET results increase attention from semiconductor industries as well as the researchers [12].

The sensor for subsumed electronic applications is the sensor of temperature based on semiconductor devices [13]. Temperature sensors based on MOSFET could be designed on the fundamental of the effect of working temperature on the I-V characteristics of the MOSFET [14]-[15]. While the bipolar junction transistor possible to use as a sensor of temperature by use it as a diode by connecting its base and collector together. In a similar way, a MOSFET could be used in diode mode by connecting the drain or source with gate to use it as a temperature sensor Figure 2.

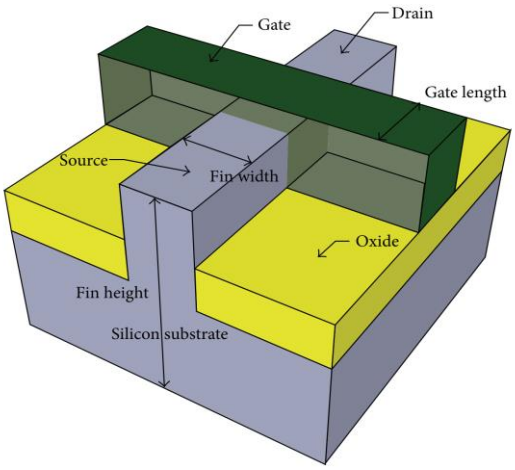

Figure 1. FinFET structure [2]

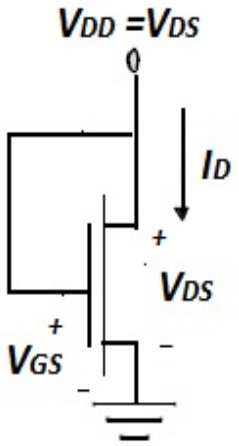

Figure 2. Diode mode of MOSFET to use it as a sensor of temperature (V_g=V_d=V_{DD})

The Nano-dimensional electronic devices such as diodes, transistors, capacitors, and resistors, have newly become marketable in the industry of electronics because of their so tiny applicable circuits. The characteristics of these Nano devices, which may correspond to enormous novel applications [16]-[20], will likely build on the Nano-dimensional feature of such devices. The new versions of chips with these comparatively novel and Nano-dimensional transistors may be further considered when new future research findings are achieved. Also, the new designs and structures of MOSFET with Nano-dimensions are included in novel technologies and consequently require more investigation and improvements to overcome the limitations of normal MOSFET structure when its dimensions going down to Nano range.

Simulation of nano-devices in nano-electronic has extra importance in understanding those new nano-devices' merits. So, simulation tools are used in this research for realization and valuation of the FinFET sensitivity with temperature. The simulation tools have an ability to support the research fields for more characterization the Nano-dimensional devices [21]. As well, simulation tools can define the nano-device failure, in addition, retrenchment the costs of fabrication of these nano-devices in the Nano dimensions field [22], [23].

2. RESEARCH METHOD

In this study, multi-gate field effect transistor (MuGFET) is used as the simulation tool to explore the fin field-effect transistor (FinFET) characteristics. The I_d-V_g characteristics of FinFET under different environmental situations and with different parameters are examined. The impact of fin width of the gate on the characteristics of temperature has been studied depending on the output characteristics of the FinFET. The simulation tool MuGFET [24] has been used in this research.

MuGFET simulator depends mainly on PADRE or PROPHET for simulation, PADRE or PROPHET was invented at Bell Laboratories. The partial differential equation profiler for one, two, or three dimension were used in the PROPHET, and PADRE simulation depends on a device-oriented for 3D or 2D transistors structure with arbitrary geometry [24]. This simulation tool has an ability to provide adequate characteristic curves of FinFET for researcher to aid him completely explain and understand the FinFET physics. Furthermore, the simulation tool gives self-consistent solutions to drift-diffusion and Poisson equations [25], also this simulation tool, when calculating FinFET characteristics, can be used to simulate the movement of transport objects. In this research, the output characteristics (I_d–V_g) of FinFET at temperature range from 250 K° to 400 K° with steps 25 K° are explored as shown in Figures 3-8 with parameters in Table 1.

Table 1. The simulated FinFET dimensions and parameters of used in this study

Parameter	Values
Length of channel (L_g)	85 nm
Length of source (L_s)	50 nm
Length of drain (L_d)	50 nm
concentration of channel (P-type)	10^{16} cm^{-3}
concentration of source (N-type)	10^{19} cm^{-3}
concentration of drain (N-type)	10^{19} cm^{-3}
Thickness of oxide (T_{ox})	2.5 nm
Fin width of gate (W_F)	5, 10, 20, 40, and 80 nm

3. RESULTS AND DISCUSSION

Figure 3 shows the effect of working temperature on the FinFET important parameters including drain-induced barrier lowering (DIBL), subthreshold swing (SS), and threshold voltage (V_T) at fin width W_F=5 nm, all measurements done with working temperature range from 250 to 400 K°. It is clear that the increasing working temperature tends to decrease V_T linearly, at 250 K° the V_T=0.65 V which the higher value and at 400 K° the V_T=0.62 V which is the lower. The slope of curve which represents the threshold voltage sensitivity with working temperature of transistor is -0.16 mV/K°. While, the best SS (at 49.7 mV/dec) and the near value to ideal SS (49.6 mV/dec) happen at lower temperature at 250 K° and then increases linearly with increasing temperature until reaching (80.09 mV/dec) at 400 K°, which is also near to the ideal SS at 79.4 mV/dec at 400 K°, so for all the range of T the SS is very close to the ideal values. The SS sensitivity to the working temperature is 0.196 mV/dec.K°. DIBL increases linearly with increasing working temperature, the minimum value is 26.9 mV/V and the maximum is 79.4 mV/V.

Figure 4 presents the impact of working temperature at W_F=10 nm on the DIBL, SS, and V_T of FinFET, the working temperature T range from 250 K° to 400 K°. This figure illustrates that the increasing working temperature results decreasing V_T linearly, the V_T decreases linearly from 0.59 V at 250 K° to 0.55 V at 400 K°. The slope of curve which represents the threshold voltage sensitivity with working temperature of transistor is -0.31 mV/K°. While, at 250 K working temperature the SS value is 49.6 mV/dec which represent the nearest value to the ideal SS at 49.6 mV/dec at 250 K°, and then with increasing working temperature up to 400 K the SS increased up to 80.99 mV/dec, this SS represents the farthest value from the ideal SS at 79.4 mV/dec at 400 K°. Also, the SS here is very close to the ideal values with all range of T. The SS sensitivity to the working temperature is 0.21 mV/dec.K°. The DIBL increases as working temperature increased but at lower values than W_F=5 nm.

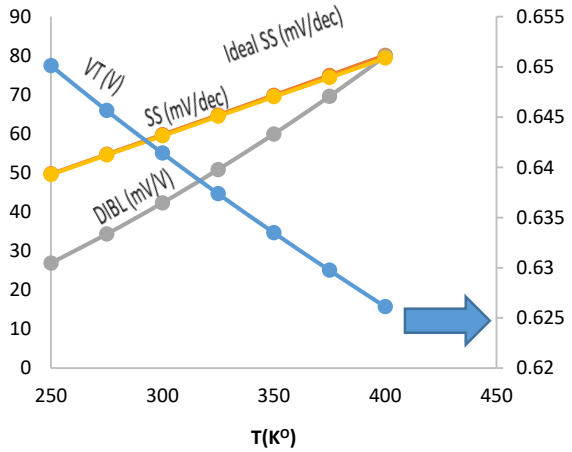

Figure 3. Temperature characteristics of V_T, SS and DIBL of the FinFET at W_F=5 nm

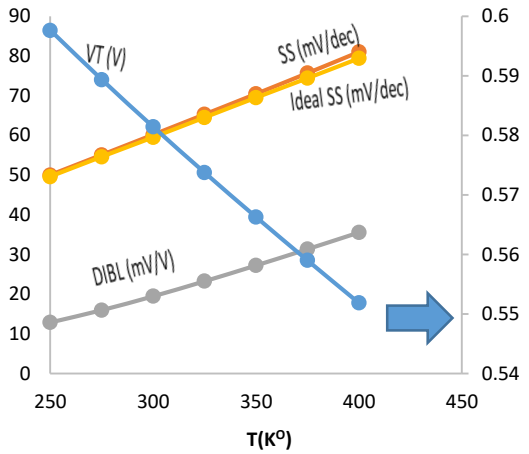

Figure 4. Temperature characteristics of V_T, SS and DIBL of the FinFET at W_F=10 nm

Figure 5 presents the impact of working temperature on the FinFET important parameters including V_T, DIBL and SS at fin width W_F=20 nm, all measurements done with working temperature range from 250 up to 400 K°. It is clear that V_T decreasing linearly with increasing working temperature, at 250 K° the V_T=0.54 V which the higher value and at 400 K° the V_T=0.49 V which is the lower. The slope of curve which represents the threshold voltage sensitivity with working temperature of transistor is -0.44 mV/K°. While, the best SS (at 51.7 mV/dec) and the near value to ideal SS (49.6 mV/dec) happen at lower

temperature at 250 K° and then increases linearly with increasing temperature until reaching (84.93 mV/dec) at 400 K°, which is far from ideal SS at 79.4 mV/dec at 400 K°, so at lower T the SS is very close to the ideal values. The SS sensitivity to the working temperature is 0.22 mV/dec.K°. DIBL increases linearly with increasing working temperature until 350 K° then decreases with increasing working temperature.

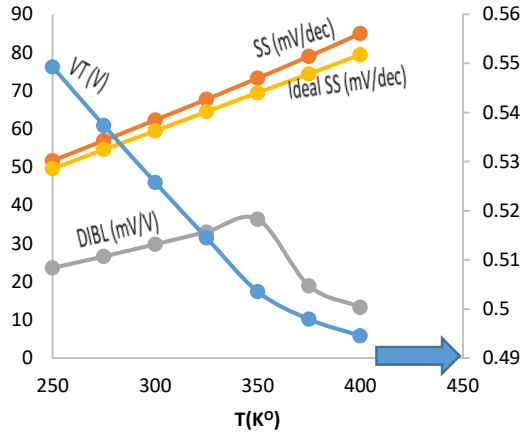

Figure 5. Temperature characteristics of V_T, SS and DIBL of the FinFET at W_F=20 nm

Figure 6 presents the impact of working temperature at W_F=40 nm on the DIBL, SS, and V_T of FinFET, the working temperature T range from 250 K° to 400 K°. This figure illustrates that the increasing of working temperature results decreasing V_T linearly, the V_T decreases linearly from 0.49 at 250 K° to 0.45 V at 400 K°. The slope of curve which represents the threshold voltage sensitivity with working temperature of transistor is -0.47 mV/K°. While, at T=250 K° the SS is at 61.99 mV/dec, this value is the nearest to the ideal SS at 49.6 mV/dec and then working temperature increases the SS increased up to 106.49 mV/dec at 400 K°, this SS value is the farthest value from the ideal SS at 79.4 mV/dec at 400 K°. Also, all values of SS here is very far from the ideal values with all range of T. The SS sensitivity to the working temperature is 0.27 mV/dec.K. The DIBL increases as working temperature increasing, DIBL increases from 26.54 up to 52.07 mV/V with the same range of T.

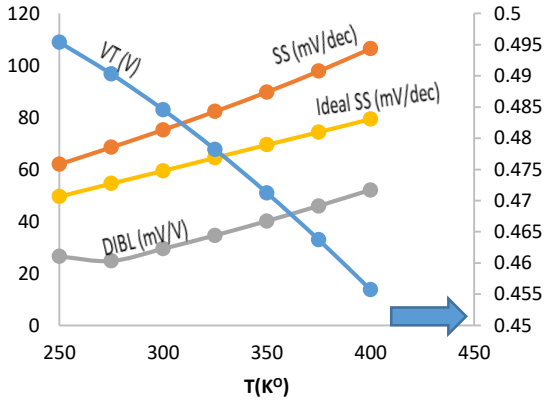

Figure 6. Temperature characteristics of V_T, SS and DIBL of the FinFET at W_F=40 nm

Figure 7 shows the effect of increasing working temperature from 250 K° to 400 K° on V_T, SS and DIBL at W_F=80 nm. It is clear that with increasing working temperature the values of V_T decreases. The slope of curve which represents the threshold voltage sensitivity with working temperature of transistor is -0.6 mV/K°. While SS and DIBL increased with increasing working temperature. This figure illustrates that for the range of temperature the values of change of the V_T from 0.38 to 0.29 V, SS from 130.66 to

253.20 mV/dec and DIBL from 230.37 to 295.89 mV/V, respectively. SS values increases with increasing temperature while the nearest value to the ideal happens at lower temperature. The SS sensitivity to the working temperature is 0.8 mV/dec.K.

Figure 8 shows the effect of fin width of FinFET on the V_T, SS, and DIBL, the FinFET channel width from 5-80 nm at 20 nm steps at working temperature T=300 K°. When the width of the channel increased, it is notice that there is a decrease in V_T and it is also notice an increase in DIBL with the W_F greater than 40 nm, the SS increases with increasing W_F, when the W_F increases from 5 nm, to 20 nm, the SS approaches the very ideal value and when the W_F increases more than 20 nm, the SS increased away the ideal value as shown in Figure 8. So, this research shows the best range for W_F is 5 to 20 nm. Figure 9 illustrates the temperature sensitivity of V_T ($\Delta V_T/\Delta T$) and SS ($SS/\Delta T$) with FinFET channel fin width (W_F). According to this figure, the lower sensitivity for both threshold voltage and subthreshold swing with better stability with working temperature happen at lower W_F.

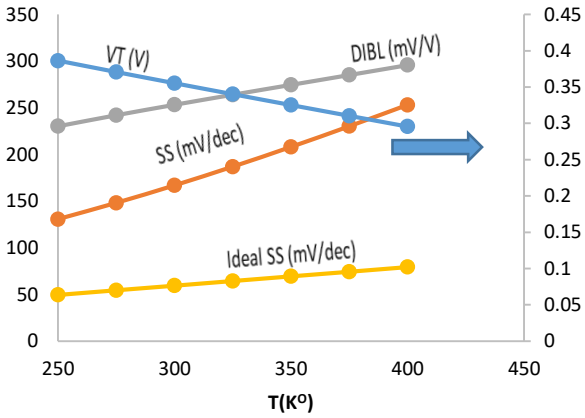

Figure 7. Temperature characteristics of V_T, SS and DIBL of the FinFET at W_F=80 nm

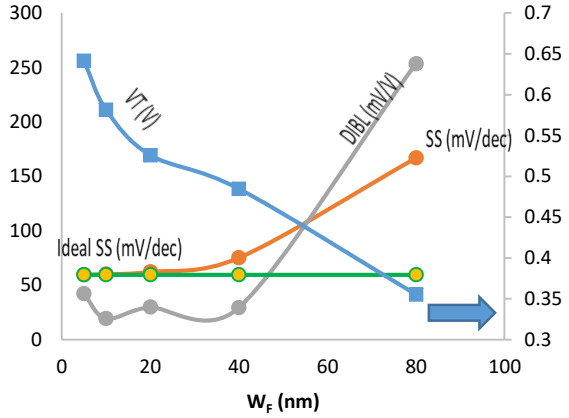

Figure 8. The V_T, SS, and DIBL with the increase of the FinFET channel fin width (W_F)

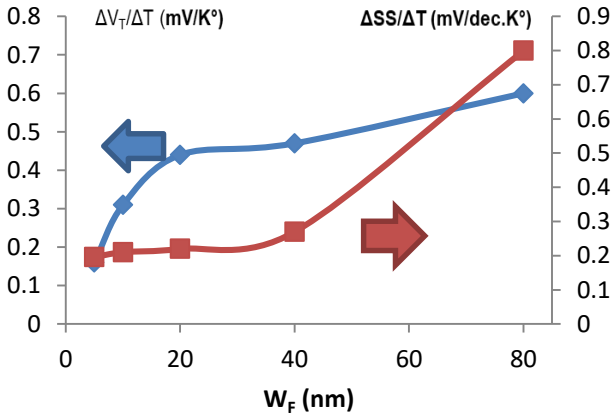

Figure 9. The temperature sensitivity of V_T and SS, with FinFET channel fin width (W_F)

4. CONCLUSION

The impact of environmental temperatures with range of 250 to 400 K° on the FinFET electrical parameters has been studied different channel fin widths (W_F=5, 10, 20, 40, and 80 nm). The results show that the V_T lowering with rising working temperature, while the increasing of working temperature tends to increase SS and DIBL. Also, the threshold voltage decreases with increasing channel fin width of transistor, while SS and DIBL increase with increasing channel fin width of transistor. The (SS is very near to the ideal value at 5 nm channel fin width then diverges and increases with increasing channel fin width. So, based on the SS and V_T temperature sensitivity, the FinFET with lower channel fin width is the best for stability with the temperatures range of 250 to 400 K°.

ACKNOWLEDGEMENTS

The authors would like to thank Tishk International University (TIU), the Ministry of Higher Education (in Malaysia) for providing financial support under Fundamental research grant No. FRGS/1/2019/TK04/UMP/02/15 (University reference RDU1901199) and Universiti Malaysia Pahang (UMP) for laboratory facilities as well as additional financial support under Internal Research grant RDU1901199.

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